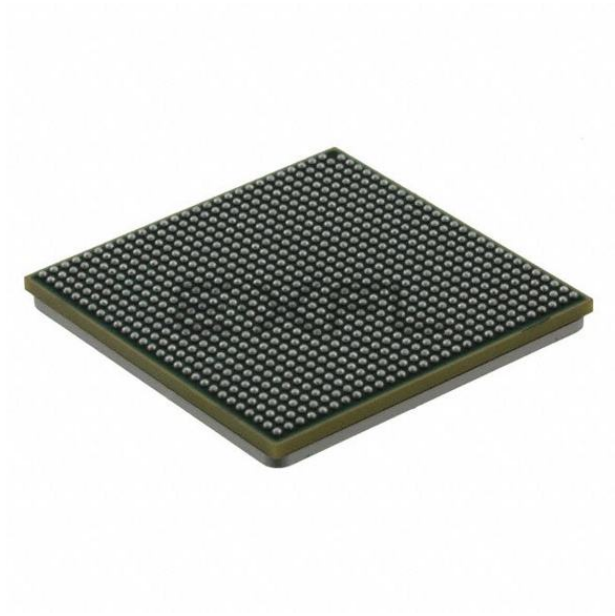

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.25GHz
Co-Processors/DSP	-
RAM Controllers	DDR2, DDR3
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	SATA 3Gbps (1)
USB	USB 2.0 (2)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 90°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/ppc8535avtath

This figure shows the major functional units within the chip.

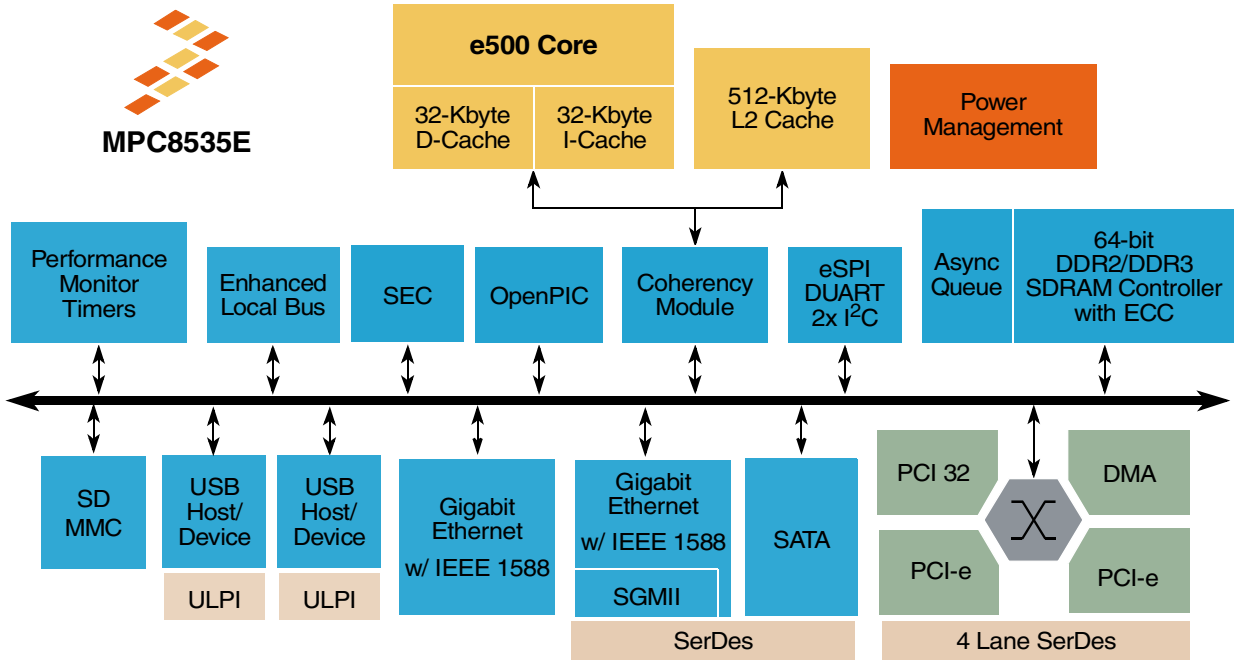


Figure 1. Chip Block Diagram

1 Pin Assignments and Reset States

NOTE

The naming convention of TSEC1 and TSEC3 is used to allow the splitting voltage rails for the eTSEC blocks and to ease the port of existing PowerQUICC III software

NOTE

The UART_SOUT[0:1] and $\overline{\text{TEST\_SEL}}$ pins must be set to a proper state during POR configuration. See Table 1 for more details.

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
LAD[0:31]	Muxed data / address	K22,L21,L22,K23,K24, L24,L25,K25,L28,L27, K28,K27,J28,H28,H27, G27,G26,F28,F26,F25, E28,E27,E26,F24,E24, C26,G24,E23,G23,F22, G22,G21	I/O	BV_{DD}	5,9,29
LDP[0:3]	Data parity	K26,G28,B27,E25	I/O	BV_{DD}	29
LA[27]	Burst address	L19	O	BV_{DD}	5,9,29
LA[28:31]	Port address	K16,K17,H17,G17	O	BV_{DD}	5,7,9,29
$\overline{\text{LCS}}$[0:4]	Chip selects	K18,G19,H19,H20,G16	O	BV_{DD}	29
$\overline{\text{LCS5}}$/$\overline{\text{DMA\_DREQ2}}$	Chips selects / DMA Request	H16	I/O	BV_{DD}	1,29
$\overline{\text{LCS6}}$/$\overline{\text{DMA\_DACK2}}$	Chips selects / DMA Ack	J16	O	BV_{DD}	1,29
$\overline{\text{LCS7}}$/$\overline{\text{DMA\_DDONE2}}$	Chips selects / DMA Done	L18	O	BV_{DD}	1,29
$\overline{\text{LWE0}}$/$\overline{\text{LBS0}}$/$\overline{\text{LFWE}}$	Write enable / Byte select	J22	O	BV_{DD}	5,9,29
$\overline{\text{LWE[1:3]}}$/$\overline{\text{LBS[1:3]}}$	Write enable / Byte select	H22,H23,H21	O	BV_{DD}	5,9,29
LBCTL	Buffer control	J25	O	BV_{DD}	5,8,9,29
LALE	Address latch enable	J26	O	BV_{DD}	5,8,9,29
LGPL0/LFCLE	UPM general purpose line 0 / FLash command latch enable	J20	O	BV_{DD}	5,9,29
LGPL1/LFALE	UPM general purpose line 1 / Flash address latch enable	K20	O	BV_{DD}	5,9,29
LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LFRE}}$	UPM general purpose line 2 / Output enable/Flash read enable	G20	O	BV_{DD}	5,8,9,29
LGPL3/$\overline{\text{LFWP}}$	UPM general purpose line 3 / Flash write protect	H18	O	BV_{DD}	5,9,29
LGPL4/$\overline{\text{LGTA}}$/LUPWAIT /LPBSE/LFRB	UPM general purpose line 4 / Target Ack/Wait/SDRAM parity byte select/Flash Ready-busy	L20	I/O	BV_{DD}	29, 35
LGPL5	UPM general purpose line 5 / Amux	K19	O	BV_{DD}	5,9,29
LCLK[0:2]	Local bus clock	H24,J24,H25	O	BV_{DD}	29
LSYNC_IN	Synchronization	D27	I	BV_{DD}	29
LSYNC_OUT	Local bus DLL	D28	O	BV_{DD}	29
DMA					
$\overline{\text{DMA\_DACK}}$[0:1] /GPIO[10:11]	DMA Acknowledge	AD6,AE10	O	OV_{DD}	—

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
Programmable Interrupt Controller					
$\overline{\text{MCP}}$	Machine check processor	Y14	I	OV_{DD}	—
$\overline{\text{UDE}}$	Unconditional debug event	AB14	I	OV_{DD}	—
IRQ[0:8]	External interrupts	AG22,AF17,AB23, AF19,AG17,AF16, AA22,Y19,AB22	I	OV_{DD}	—
IRQ[9]/$\overline{\text{DMA\_DREQ[3]}}$	External interrupt/DMA request	AE13	I	OV_{DD}	1
IRQ[10]/$\overline{\text{DMA\_DACK[3]}}$	External interrupt/DMA Ack	AD13	I/O	OV_{DD}	1
IRQ[11]/$\overline{\text{DMA\_DDONE[3]}}$	External interrupt/DMA done	AD14	I/O	OV_{DD}	1
$\overline{\text{IRQ\_OUT}}$	Interrupt output	AC17	O	OV_{DD}	2,4
Ethernet Management Interface					
EC_MDC	Management data clock	Y10	O	OV_{DD}	5,9,22
EC_MDIO	Management data In/Out	Y11	I/O	OV_{DD}	—
Gigabit Reference Clock					
EC_GTX_CLK125	Reference clock	AA6	I	LV_{DD}	31
Three-Speed Ethernet Controller (Gigabit Ethernet 1)					
TSEC1_TXD[7:0]	Transmit data	AA8,AA5,Y8,Y5,W3, W5,W4,W6	O	LV_{DD}	5,9,22
TSEC1_TX_EN	Transmit Enable	W1	O	LV_{DD}	23
TSEC1_TX_ER	Transmit Error	AB5	O	LV_{DD}	5,9
TSEC1_TX_CLK	Transmit clock In	AB4	I	LV_{DD}	—
TSEC1_GTX_CLK	Transmit clock Out	W2	O	LV_{DD}	—
TSEC1_CRS	Carrier sense	AA9	I/O	LV_{DD}	17
TSEC1_COL	Collision detect	AB6	I	LV_{DD}	—
TSEC1_RXD[7:0]	Receive data	AB3,AB7,AB8,Y6,AA2, Y3,Y1,Y2	I	LV_{DD}	—
TSEC1_RX_DV	Receive data valid	AA1	I	LV_{DD}	—
TSEC1_RX_ER	Receive data error	Y9	I	LV_{DD}	—
TSEC1_RX_CLK	Receive clock	AA3	I	LV_{DD}	—
Three-Speed Ethernet Controller (Gigabit Ethernet 3)					
TSEC3_TXD[7:0]	Transmit data	T12,V8,U8,V9,T8,T7, T5,T6	O	TV_{DD}	5,9,22
TSEC3_TX_EN	Transmit Enable	V5	O	TV_{DD}	23
TSEC3_TX_ER	Transmit Error	U9	O	TV_{DD}	5,9

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
TSEC3_TX_CLK	Transmit clock In	U10	I	TV_{DD}	—
TSEC3_GTX_CLK	Transmit clock Out	U5	O	TV_{DD}	—
TSEC3_CRS	Carrier sense	T10	I/O	TV_{DD}	17
TSEC3_COL	Collision detect	T9	I	TV_{DD}	—
TSEC3_RXD[7:0]	Receive data	U12,U13,U6,V6,V1,U3, U2,V3	I	TV_{DD}	—
TSEC3_RX_DV	Receive data valid	V2	I	TV_{DD}	—
TSEC3_RX_ER	Receive data error	T4	I	TV_{DD}	—
TSEC3_RX_CLK	Receive clock	U1	I	TV_{DD}	—
IEEE 1588					
TSEC_1588_CLK	Clock In	W9	I	LV_{DD}	29
TSEC_1588_TRIG_IN[0:1]	Trigger In	W8,W7	I	LV_{DD}	29
TSEC_1588_TRIG_OUT[0:1]	Trigger Out	U11,W10	O	LV_{DD}	5,9,29
TSEC_1588_CLK_OUT	Clock Out	V10	O	LV_{DD}	5,9,29
TSEC_1588_PULSE_OUT1	Pulse Out1	V11	O	LV_{DD}	5,9,29
TSEC_1588_PULSE_OUT2	Pulse Out2	T11	O	LV_{DD}	5,9,29
eSDHC					
SDHC_CMD	Command line	AH10	I/O	OV_{DD}	29
$\overline{\text{SDHC\_CD}}$/GPIO[4]	Card detection	AH11	I	OV_{DD}	—
SDHC_DAT[0:3]	Data line	AG12,AH12,AH13, AG11	I/O	OV_{DD}	29
SDHC_DAT[4:7] / SPI_CS[0:3]	8-bit MMC Data line / SPI chip select	AE8,AC10,AF9,AA10	I/O	OV_{DD}	29
SDHC_CLK	SD/MMC/SDIO clock	AG13	I/O	OV_{DD}	29
$\overline{\text{SDHC\_WP}}$/GPIO[5]	Card write protection	AG10	I	OV_{DD}	1, 32
eSPI					
SPI_MOSI	Master Out Slave In	AF8	I/O	OV_{DD}	29
SPI_MISO	Master In Slave Out	AD9	I	OV_{DD}	29
SPI_CLK	eSPI clock	AD8	I/O	OV_{DD}	29
SPI_CS[0:3] / SDHC_DAT[4:7]	eSPI chip select / SDHC 8-bit MMC data	AE8,AC10,AF9,AA10	I/O	OV_{DD}	29
DUART					
$\overline{\text{UART\_CTS}}$[0:1]	Clear to send	AE11,Y12	I	OV_{DD}	29
$\overline{\text{UART\_RTS}}$[0:1]	Ready to send	AB12,AD12	O	OV_{DD}	29
UART_SIN[0:1]	Receive data	AC12,AF12	I	OV_{DD}	29

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
XVDD	SerDes 1 transceiver supply	M21,N23,P20,R22,T20, U23,V21,W22,Y20, AA23	—	XV_{DD}	—
S2VDD	SerDes 2 core logic supply	R6,N7,M9	—	$S2V_{DD}$	—
X2VDD	SerDes 2 transceiver supply	R11,N12,L11	—	$X2V_{DD}$	—
VDD_CORE	Core, L2 logic supply	P13,U16,L16,M15,N14, R14,P15,N16,M13, U14,T13,L14,T15,R16, K13	—	V_{DD_CORE}	—
VDD_PLAT	Platform logic supply	T19,T17,V17,U18,R18, N18,M19,P19,P17,M17	—	V_{DD_PLAT}	—
AVDD_CORE	CPU PLL supply	AH16	—	AV_{DD_CORE}	20,28
AVDD_PLAT	Platform PLL supply	AH18	—	AV_{DD_PLAT}	20
AVDD_DDR	DDR PLL supply	AH19	—	AV_{DD_DDR}	20
AVDD_LBIU	Local Bus PLL supply	C28	—	AV_{DD_LBIU}	20
AVDD_PCI1	PCI PLL supply	AH20	—	AV_{DD_PCI1}	20
AVDD_SRDS	SerDes 1 PLL supply	W28	—	AV_{DD_SRDS}	20
AVDD_SRDS2	SerDes 2 PLL supply	T1	—	AV_{DD_SRDS2}	20
SENSEVDD_CORE	—	V15	—	V_{DD_CORE}	13
SENSEVDD_PLAT	—	W17	—	V_{DD_PLAT}	13
GND	Ground	D5,AE7,F4,D26,D23, C12,C15,E20,D8,B10, AF3,E3,J14,K21,F8,A3, F16,E12,E15,D17,L1, F21,H1,G13,G15,G18, C6,A14,A7,G25,H4, C20,J12,J15,J17,F27, M5,J27,K11,L26,K7, K8,T14,V14,M16,M18, P14,N15,N17,N19,N2, P5,P16,P18,M14,R15, R17,R19,T16,T18,L17, U15,U17,U19,V18,C27, Y13,AE26,AA19,AE21, B28,AC11,AD19,AD23, L15,AD15,AG23,AE9, A27,V7,Y7,AC5,U4,Y4, AE12,AB9,AA14,N13, R13,L13	—	—	—
XGND	SerDes 1Transceiver pad GND (xpadvss)	M20,M24,N22,P21, R23,T21,U22,V20, W23, Y21	—	—	—

2.3 Power Characteristics

The estimated power dissipation for the core complex bus (CCB) versus the core frequency for this family of PowerQUICC III chips is shown in the following table.

Table 5. Power Dissipation [5]

Power Mode	Core Frequency	CCB Frequency	DDR Frequency	V_{DD} Platform	V_{DD} Core	Junction Temperature	Core Power		Platform Power[9]		Notes
	(MHz)	(MHz)	(MHz)	(V)	(V)	(°C)	mean[7]	Max	mean[7]	Max	
Maximum (A)	600	400	400	1.0	1.0	105 /90	—	4.1/3.3	—	4.7/3.7	1, 3, 8
Thermal (W)							—	3.7/2.9	—	4.7/3.7	1, 4, 8
Typical (W)						65	1.5	—	1.5	—	1, 2
Doze (W)							1.2	1.9	1.4	1.9	1
Nap (W)							0.8	1.5	1.4	1.9	1
Sleep (W)							0.8	1.5	1.0	1.6	1
Deep Sleep (W)						35	0	0	0.6	1.1	6
Maximum (A)	800	400	400	1.0	1.0	105 / 90	—	4.5/3.7	—	4.7/3.7	1, 3, 8
Thermal (W)							—	3.9/3.1	—	4.7/3.7	1, 4, 8
Typical (W)						65	1.7	—	1.5	—	1, 2
Doze (W)							1.3	2.1	1.4	1.9	1
Nap (W)							0.8	1.5	1.4	1.9	1
Sleep (W)							0.8	1.5	1.0	1.6	1
Deep Sleep (W)						35	0	0	0.6	1.1	1,6
Maximum (A)	1000	400	400	1.0	1.0	105 / 90	—	4.8/4.0	—	4.7/3.7	1, 3, 8
Thermal (W)							—	4.1/3.3	—	4.7/3.7	1, 4, 8
Typical (W)						65	1.9	—	1.5	—	1, 2
Doze (W)							1.4	2.2	1.4	1.9	1
Nap (W)							0.8	1.6	1.4	1.9	1
Sleep (W)							0.8	1.6	1.0	1.6	1
Deep Sleep (W)						35	0	0	0.6	1.1	1, 6

A timing diagram for TBI receive appears in the following figure.

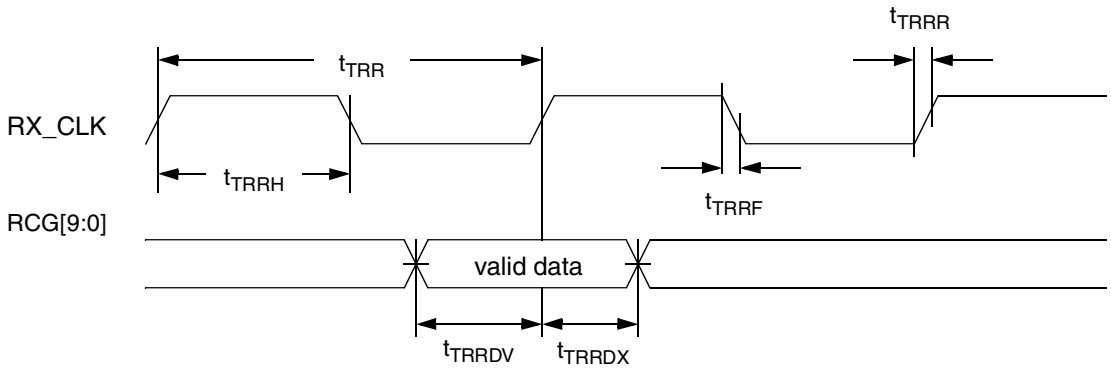


Figure 24. TBI Single-Clock Mode Receive AC Timing Diagram

2.9.2.6 RGMII and RTBI AC Timing Specifications

This table presents the RGMII and RTBI AC timing specifications.

Table 35. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 2.5 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)	t_{SKRGT_TX}	–500	0	500	ps
Data to clock input skew (at receiver) [2]	t_{SKRGT_RX}	1.0	—	2.8	ns
Clock period duration [3]	t_{RGT}	7.2	8.0	8.8	ns
Duty cycle for 1000BASE-T[4]	t_{RGTH}/t_{RGT}	45	—	55	%
Duty cycle for 10BASE-T and 100BASE-TX [3, 4]	t_{RGTH}/t_{RGT}	40	50	60	%
Rise time (20%–80%)	t_{RGTR}	—	—	0.75	ns
Fall time (20%–80%)	t_{RGTF}	—	—	0.75	ns

Notes:

1. Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns will be added to the associated clock signal.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transition to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.

This figure shows the RGMII and RTBI AC timing and multiplexing diagrams.

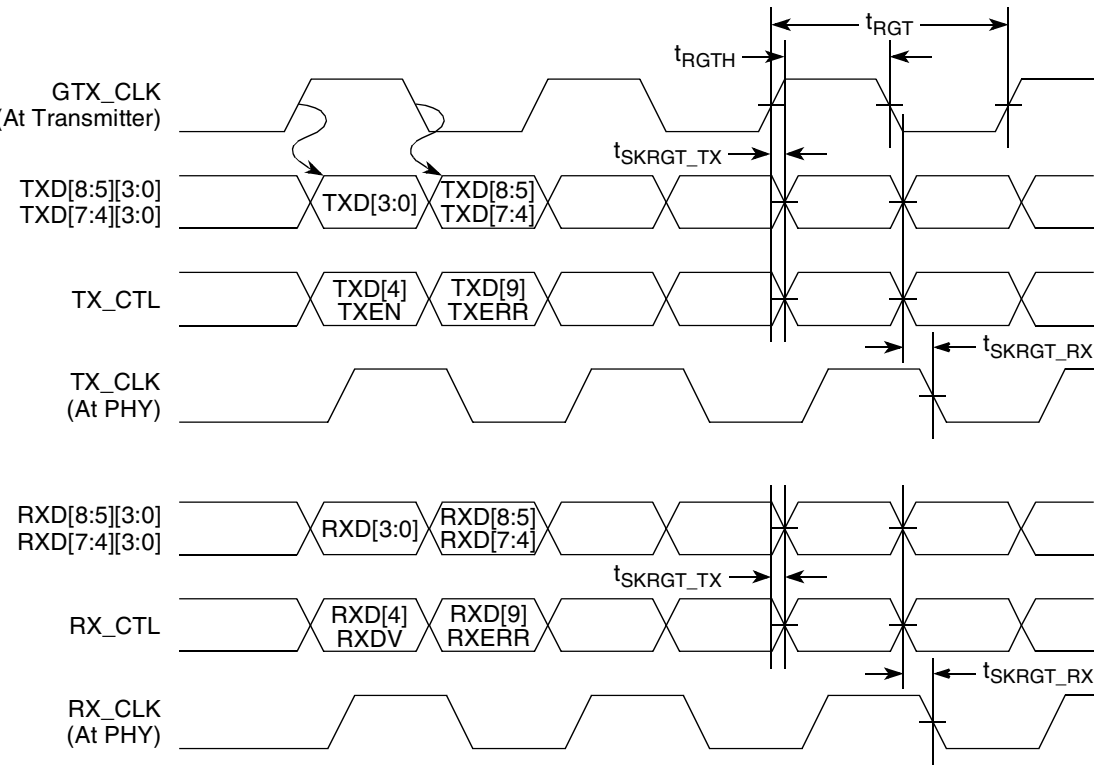


Figure 25. RGMII and RTBI AC Timing and Multiplexing Diagrams

2.9.2.7 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

2.9.2.7.1 RMII Transmit AC Timing Specifications

The RMII transmit AC timing specifications are in the following table.

Table 36. RMII Transmit AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
TSECn_TX_CLK clock period	t_{RMT}	15.0	20.0	25.0	ns
TSECn_TX_CLK duty cycle	t_{RMTH}	35	50	65	%
TSECn_TX_CLK peak-to-peak jitter	t_{RMTJ}	—	—	250	ps

Table 36. RMII Transmit AC Timing Specifications (continued)

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
Rise time TSECn_TX_CLK (20%–80%)	t_{RMTR}	1.0	—	2.0	ns
Fall time TSECn_TX_CLK (80%–20%)	t_{RMTF}	1.0	—	2.0	ns
TSECn_TX_CLK to RMII data TXD[1:0], TX_EN delay	t_{RMTDX}	2.0	—	10.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure shows the RMII transmit AC timing diagram.

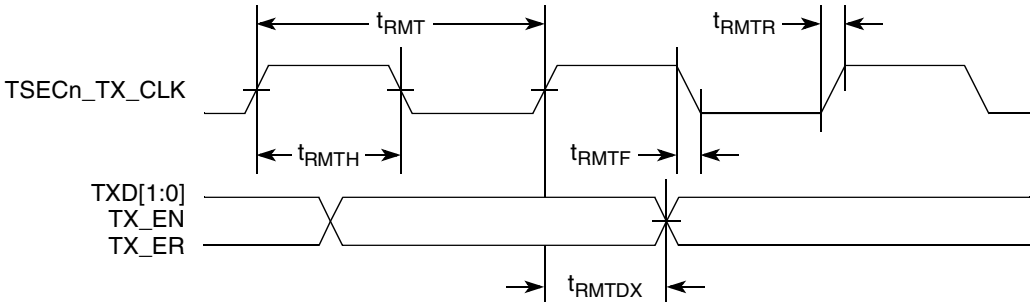


Figure 26. RMII Transmit AC Timing Diagram

2.9.2.7.2 RMII Receive AC Timing Specifications

Table 37. RMII Receive AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
TSECn_RX_CLK clock period	t_{RMR}	15.0	20.0	25.0	ns
TSECn_RX_CLK duty cycle	t_{RMRH}	35	50	65	%
TSECn_RX_CLK peak-to-peak jitter	t_{RMRJ}	—	—	250	ps
Rise time TSECn_RX_CLK (20%–80%)	t_{RMRR}	1.0	—	2.0	ns

2.12 enhanced Local Bus Controller (eLBC)

This section describes the DC and AC electrical specifications for the local bus interface of the chip.

2.12.1 Local Bus DC Electrical Characteristics

This table provides the DC electrical characteristics for the local bus interface operating at BV_{DD} = 3.3 V DC.

Table 48. Local Bus DC Electrical Characteristics (3.3 V DC)

Parameter	Symbol	Min	Max	Unit
Supply voltage 3.3V	BV_{DD}	3.13	3.47	V
High-level input voltage	V_{IH}	1.9	BV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current (BV_{IN} [1] = 0 V or BV_{IN} = BV_{DD})	I_{IN}	—	±5	μA
High-level output voltage (BV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V
Low-level output voltage (BV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V

Note:

1. The symbol BV_{IN}, in this case, represents the BV_{IN} symbol referenced in Table 1.

This table provides the DC electrical characteristics for the local bus interface operating at BV_{DD} = 2.5 V DC.

Table 49. Local Bus DC Electrical Characteristics (2.5 V DC)

Parameter	Symbol	Min	Max	Unit
Supply voltage 2.5V	BV_{DD}	2.37	2.63	V
High-level input voltage	V_{IH}	1.70	BV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.7	V
Input current (BV_{IN} [1] = 0 V or BV_{IN} = BV_{DD})	I_{IH}	—	10	μA
	I_{IL}		–15	
High-level output voltage (BV_{DD} = min, I_{OH} = –1 mA)	V_{OH}	2.0	BV_{DD} + 0.3	V
Low-level output voltage (BV_{DD} = min, I_{OL} = 1 mA)	V_{OL}	GND – 0.3	0.4	V

Note:

1. Note that the symbol BV_{IN}, in this case, represents the BV_{IN} symbol referenced in Table 1.

This table provides the DC electrical characteristics for the local bus interface operating at BV_{DD} = 1.8 V DC.

Table 50. Local Bus DC Electrical Characteristics (1.8 V DC)

Parameter	Symbol	Condition	Min	Max	Unit
Supply voltage 1.8V	BV_{DD}	—	1.71	1.89	V
High-level input voltage	V_{IH}	—	0.65*BV_{DD}	0.3+BV_{DD}	V
Low-level input voltage	V_{IL}	—	–0.3	0.35*BV_{DD}	V
Input current (BV_{IN} [1] = 0 V or BV_{IN} = BV_{DD})	I_{IN}	—	-15	10	μA
High-level output voltage	V_{OH}	I_{OH} = –100 μA	BV_{DD} – 0.2	—	V
		I_{OH} = –2 mA	BV_{DD} – 0.45	—	
Low-level output voltage	V_{OL}	I_{OH} = 100 μA	—	0.2	V
		I_{OH} = 2 mA	—	0.45	

Note:

1. Note that the symbol BV_{IN}, in this case, represents the BV_{IN} symbol referenced in Table 1.

2.12.2 Local Bus AC Electrical Specifications

This table describes the general timing parameters of the local bus interface at BV_{DD} = 3.3 V DC. For information about the frequency range of local bus see Section 2.23.1, “Clock Ranges.”

Table 51. Local Bus General Timing Parameters (BV_{DD} = 3.3 V DC)

Parameter	Symbol [1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	7.5	12	ns	2
Local bus duty cycle	t_{LBKH}/t_{LBK}	43	57	%	—
LCLK[n] skew to LCLK[m] or LSYNC_OUT	$t_{LBKSKEW}$		150	ps	7
Input setup to local bus clock (except LUPWAIT)	$t_{LBIVKH1}$	1.8	—	ns	3, 4
LUPWAIT input setup to local bus clock	$t_{LBIVKH2}$	1.7	—	ns	3, 4
Input hold from local bus clock (except LUPWAIT)	$t_{LBIXKH1}$	1.0	—	ns	3, 4
LUPWAIT input hold from local bus clock	$t_{LBIXKH2}$	1.0	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH setup and hold time)	t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKHOV1}$	—	2.3	ns	—
Local bus clock to data valid for LAD/LDP	$t_{LBKHOV2}$	—	2.4	ns	3
Local bus clock to address valid for LAD	$t_{LBKHOV3}$	—	2.3	ns	3
Local bus clock to LALE assertion	$t_{LBKHOV4}$	—	2.3	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKHOX1}$	0.7	—	ns	3

Table 54. Local Bus General Timing Parameters—PLL Bypassed (continued)

Parameter	Symbol [1]	Min	Max	Unit	Notes
Local bus clock to data valid for LAD/LDP	$t_{LBKLOV2}$	—	0.5	ns	4
Local bus clock to address valid for LAD, and LALE	$t_{LBKLOV3}$	—	0.5	ns	4
Local bus clock to LALE assertion	$t_{LBKLOV4}$	—	0.5	ns	4
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKLOX1}$	—	2.2	ns	4,8
Output hold from local bus clock for LAD/LDP	$t_{LBKLOX2}$	—	2.2	ns	4,8
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$t_{LBKLOZ1}$	—	0.1	ns	7
Local bus clock to output high impedance for LAD/LDP	$t_{LBKLOZ2}$	—	0.1	ns	7

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to local bus clock for PLL bypass mode.
3. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.
4. All signals are measured from BVDD/2 of the rising edge of local bus clock for PLL bypass mode to 0.4 x BVDD of the signal in question for 3.3-V signaling levels.
5. Input timings are measured at the pin.
6. t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is guaranteed with LBCR[AHD] = 0.
7. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
8. These timing parameters for PLL bypass mode are defined in the opposite direction of the PLL enabled output hold timing parameters.

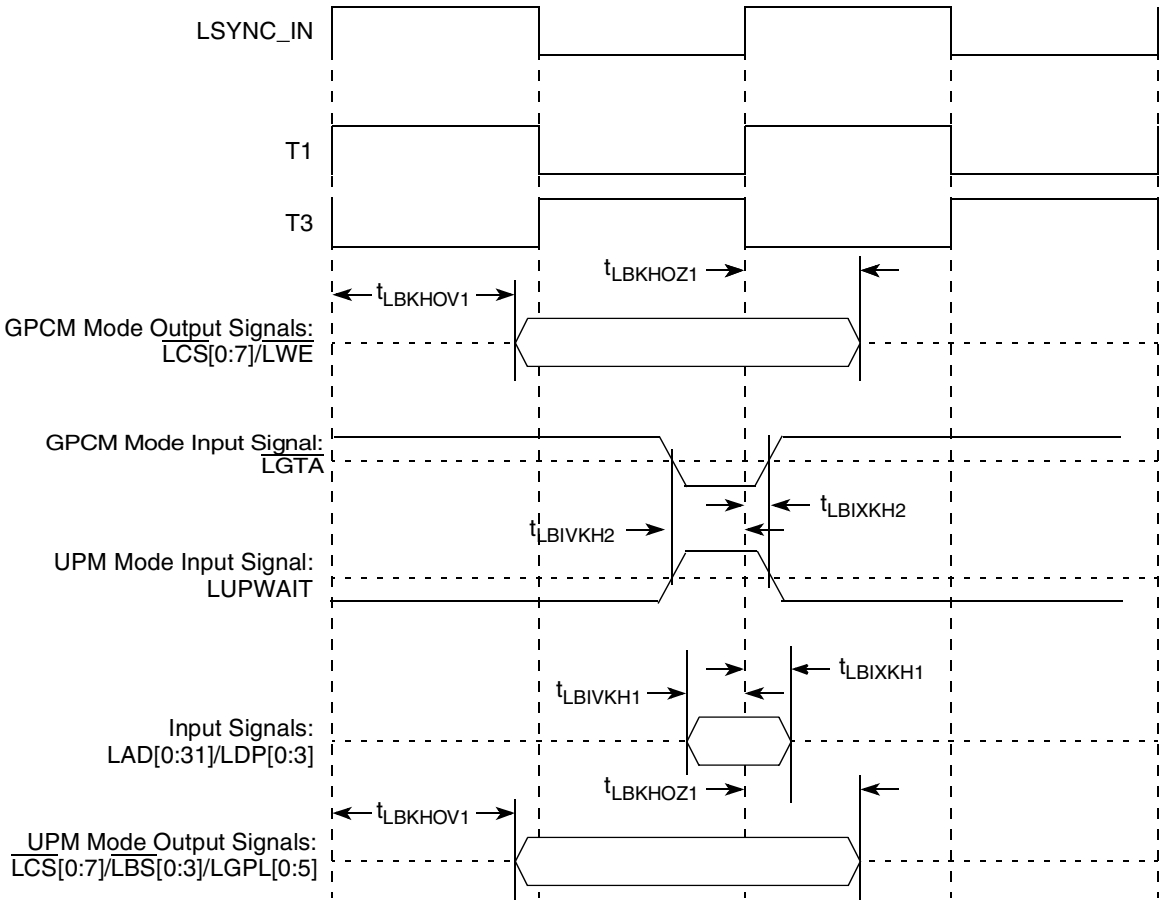


Figure 41. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4(PLL Enabled)

This figure provides the AC test load for TDO and the boundary-scan outputs.

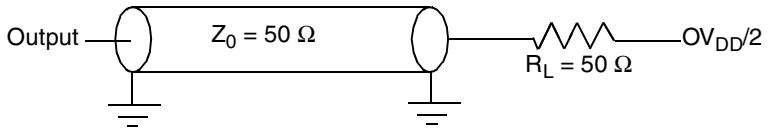


Figure 45. AC Test Load for the JTAG Interface

This figure provides the JTAG clock input timing diagram.

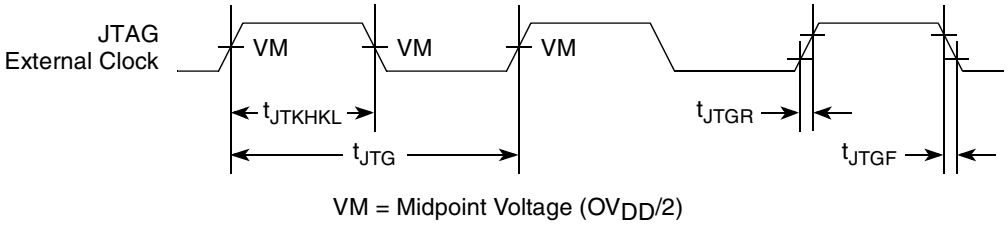


Figure 46. JTAG Clock Input Timing Diagram

This figure provides the $\overline{\text{TRST}}$ timing diagram.

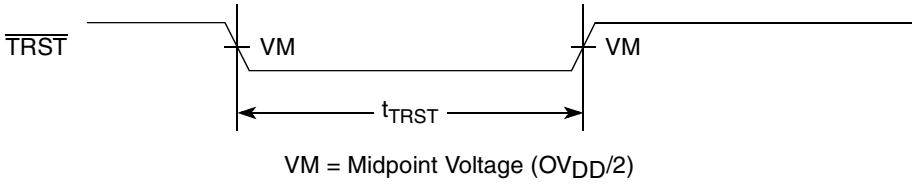


Figure 47. $\overline{\text{TRST}}$ Timing Diagram

This figure provides the boundary-scan timing diagram.

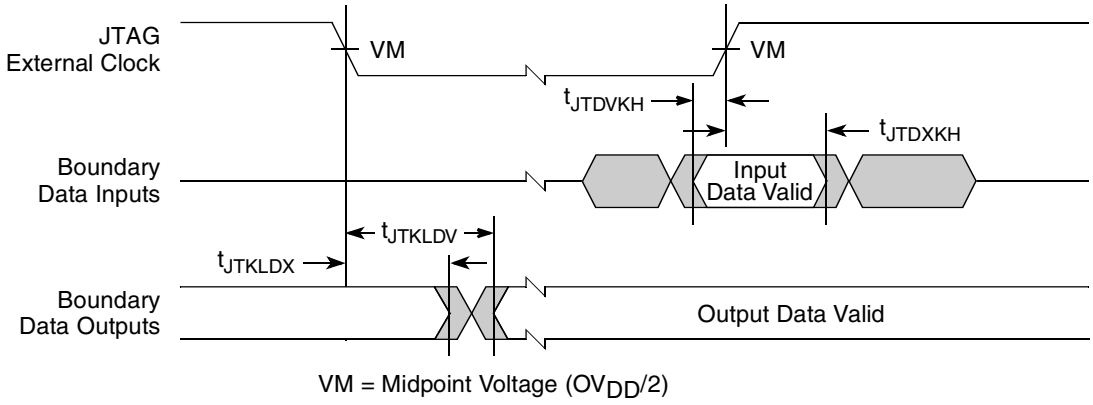


Figure 48. Boundary-Scan Timing Diagram

2.16 Serial ATA (SATA)

This section describes the DC and AC electrical specifications for the serial ATA (SATA) of the chip. Note that the external cabled applications or long backplane applications (Gen1x & Gen2x) are not supported.

Table 68. PCI AC Timing Specifications at 66 MHz (continued)

Parameter	Symbol [1]	Min	Max	Unit	Notes
$\overline{\text{HRESET}}$ high to first $\overline{\text{FRAME}}$ assertion	t_{PCRHFV}	10	—	clocks	8
Rise time (20%–80%)	t_{PCICLK}	0.6	2.1	ns	—
Failing time (20%–80%)	t_{PCICLK}	0.6	2.1	ns	—

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the SYSCLK clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.2 Local Bus Specifications*.
3. All PCI signals are measured from $OV_{DD}/2$ of the rising edge of PCI_SYNC_IN to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V PCI signaling levels.
4. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
5. Input timings are measured at the pin.
6. The timing parameter t_{SYS} indicates the minimum and maximum CLK cycle times for the various specified frequencies. The system clock period must be kept within the minimum and maximum defined ranges. For values see Section 22, “Clocking.”
7. The setup and hold time is with respect to the rising edge of $\overline{\text{HRESET}}$.
8. The timing parameter t_{PCRHFV} is a minimum of 10 clocks rather than the minimum of 5 clocks in the *PCI 2.2 Local Bus Specifications*.
9. The reset assertion timing requirement for $\overline{\text{HRESET}}$ is 100 µs.

This figure provides the AC test load for PCI.

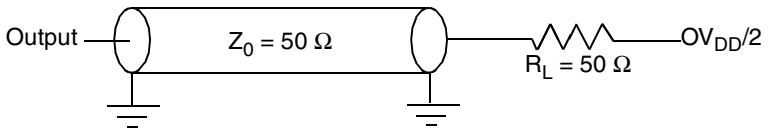


Figure 54. PCI AC Test Load

This figure shows the PCI input AC timing conditions.

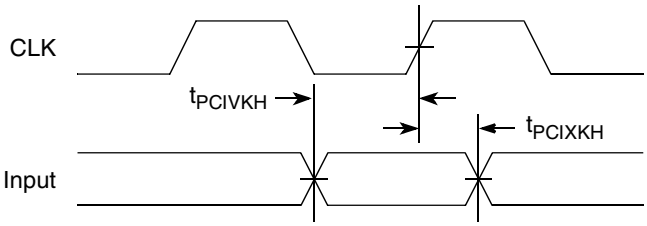


Figure 55. PCI Input AC Timing Measurement Conditions

Table 72. Differential Receiver (RX) Input Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Units	Comments
$L_{TX-SKEW}$	Total Skew	—	—	20	ns	Skew across all lanes on a Link. This includes variation in the length of SKP ordered set (for example, COM and one to five Symbols) at the RX as well as any delay differences arising from the interconnect itself.

Notes:
1. No test load is necessarily associated with this value.
2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 71 should be used as the RX device when taking measurements (also refer to the Receiver compliance eye diagram shown in Figure 70). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
3. A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the Transmitter and interconnect collected any 250 consecutive UIs. The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
4. The Receiver input impedance shall result in a differential return loss greater than or equal to 15 dB with the D+ line biased to 300 mV and the D- line biased to -300 mV and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50 ohms to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50 ohm probes - see Figure 71). Note: that the series capacitors CTX is optional for the return loss measurement.
5. Impedance during all LTSSM states. When transitioning from a Fundamental Reset to Detect (the initial state of the LTSSM) there is a 5 ms transition time before Receiver termination values must be met on all un-configured Lanes of a Port.
6. The RX DC Common Mode Impedance that exists when no power is present or Fundamental Reset is asserted. This helps ensure that the Receiver Detect circuit will not falsely assume a Receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.
7. It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

2.22 Receiver Compliance Eye Diagrams

The RX eye diagram in Figure 70 is specified using the passive compliance/test measurement load (see Figure 71) in place of any real PCI Express RX component.

Note: In general, the minimum Receiver eye diagram measured with the compliance/test measurement load (see Figure 71) will be larger than the minimum Receiver eye diagram measured over a range of systems at the input Receiver of any real PCI Express component. The degraded eye diagram at the input Receiver is due to traces internal to the package as well as silicon parasitic characteristics which cause the real PCI Express component to vary in impedance from the compliance/test measurement load. The input Receiver eye diagram is implementation specific and is not specified. RX component designer should provide additional margin to adequately compensate for the degraded minimum Receiver eye diagram (shown in Figure 70) expected at the input Receiver based on some adequate combination of system simulations and the Return Loss measured looking into the RX package and silicon. The RX eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.

The eye diagram must be valid for any 250 consecutive UIs.

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 77). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

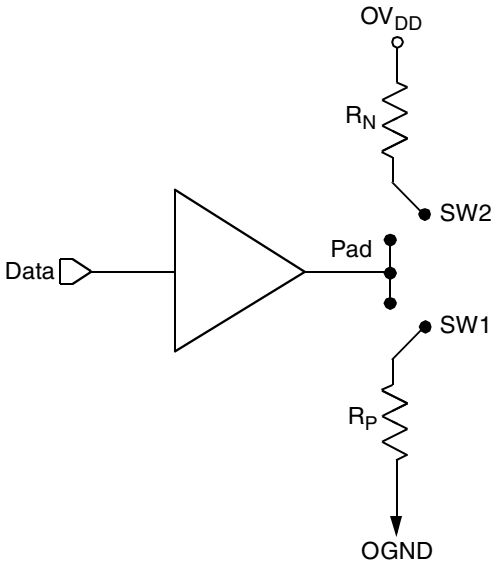


Figure 77. Driver Impedance Measurement

This table summarizes the signal impedance targets. The driver impedances are targeted at minimum V_{DD}, nominal OV_{DD}, 105°C.

Table 81. Impedance Characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI	DDR DRAM	Symbol	Unit
R_N	45 Target	45 Target (cfg_pci_impd=1) 25 Target (cfg_pci_impd=0)	18 Target (full strength mode) 36 Target (full strength mode)	Z_0	Ω
R_P	45 Target	45 Target (cfg_pci_impd=1) 25 Target (cfg_pci_impd=0)	18 Target (full strength mode) 36 Target (full strength mode)	Z_0	Ω

Note: Nominal supply voltages. See Table 1.

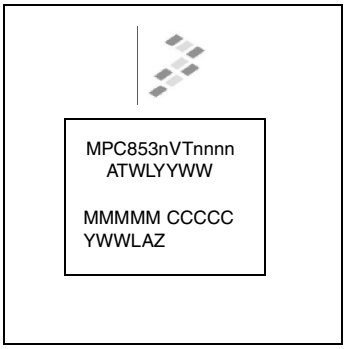
3.9 Configuration Pin Muxing

The chip provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{HRESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Most of these sampled configuration pins are equipped with an on-chip gated resistor of approximately 20 kΩ. This value should permit the 4.7-kΩ resistor to pull the configuration pin to a valid logic low level. The pull-up resistor is enabled only during $\overline{\text{HRESET}}$ (and for platform /system clocks after $\overline{\text{HRESET}}$ deassertion to ensure capture of the reset value). When the input receiver is disabled the pull-up is also, thus allowing functional operation of the pin as an output with minimal signal quality or delay disruption. The default value for all configuration bits treated this way has been encoded such that a high voltage level puts the chip into the default state and external resistors are needed only when non-default settings are required by the user.

4.2 Part Marking

Parts are marked as in the example shown in the following figure.



FC-PBGA

Notes:

MMMMM is the 5-digit mask number.
ATWLYYWW is the traceability code.
CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.

Figure 80. Part Marking for FC-PBGA

4.3 Part Numbering

These tables list all part numbers that are offered for the chip.

Table 83. MPC8535 Part Numbers Commercial Tier

Core/Platform/ DDR (MHz)	Standard Temp Without Security	Standard Temp With Security	Notes
600/400/400	MPC8535AVTAKG(A)	MPC8535EAVTAKG(A)	—
800/400/400	MPC8535AVTANG(A)	MPC8535EAVTANG(A)	—
1000/400/400	MPC8535AVTAQG(A)	MPC8535EAVTAQG(A)	—
1250/500/500	MPC8535AVTATH(A)	MPC8535EAVTATH(A)	—
1250/500/667	MPC8535AVTATLA	MPC8535EAVTATLA	—

Table 84. MPC8535 Part Numbers Industrial Tier

Core/Platform/ DDR (MHz)	Standard Temp Without Security	Standard Temp With Security	Extended Temp Without Security	Extended Temp With Security	Notes
600/400/400	MPC8535BVTAKG(A)	MPC8535EBVTAKG(A)	MPC8535CVTAKG(A)	MPC8535ECVTAKG(A)	1
800/400/400	MPC8535BVTANG(A)	MPC8535EBVTANG(A)	MPC8535CVTANG(A)	MPC8535ECVTANG(A)	
1000/400/400	MPC8535BVTAQG(A)	MPC8535EBVTAQG(A)	MPC8535CVTAQG(A)	MPC8535ECVTAQG(A)	
1250/500/500	MPC8535BVTATH(A)	MPC8535EBVTATH(A)	MPC8535CVTATH(A)	MPC8535ECVTATH(A)	
1250/500/667	MPC8535BVTATLA	MPC8535EBVTATLA	MPC8535CVTATLA	MPC8535ECVTATLA	

Note:

1. The last letter A indicates a Rev 1.2 silicon. It would be Rev 1.0 or Rev 1.1 silicon without a letter A

5 Package Information

This section details package parameters, pin assignments, and dimensions.

5.1 Package Parameters for the FC-PBGA

The package parameters are as provided in the following list. The package type is 29 mm × 29 mm, 783 flip chip plastic ball grid array (FC-PBGA) without a lid.

Package outline	29 mm × 29 mm
Interconnects	783
Pitch	1 mm
Minimum module height	2.23 mm
Maximum module height	2.8 mm
Solder Balls	96.5Sn/3.5Ag
Ball diameter (typical)	0.6 mm

5. Capacitors may not be present on all devices
6. Caution must be taken not to short exposed metal capacitor pads on package top.
7. All dimensions are symmetric across the package center lines, unless dimensioned otherwise.

6 Product Documentation

The following documents are required for a complete description of the chip and are needed to design properly with the part.

- *MPC8536E PowerQUICC III Integrated Processor Reference Manual* (document number: MPC8536ERM)
- *e500 PowerPC Core Reference Manual* (document number: E500CORERM)

7 Document Revision History

This table provides a revision history for this hardware specification.

Table 85. Document Revision History

Revision	Date	Substantive Change(s)
5	09/2011	• Removed PVDD from Table 1, “Pinout Listing.”
4	06/2011	• In Table 1, “Pinout Listing,” updated the power supply for TSEC3 pins to TVDD. • Updated Table 56, “eSDHC AC Timing Specifications.” • In Section 4.3, “Part Numbering,” added an extra bin (1250/500/667) to support DDR3.
3	11/2010	• In Table 1, “Pinout Listing,” added the following note: “For systems that boot from Local Bus (GPCM)-controlled NOR flash or (FCM) controlled NAND flash, a pullup on LGPL4 is required...” In addition, updated footnote 26 and added footnote 29 to PCI1_AD. • Updated Table 21 • Updated Figure 25, “RGMII and RTBI AC Timing and Multiplexing Diagrams.” • In Table 44, “MII Management DC Electrical Characteristics,” changed the Voh/Vol values for MDIO/MDC. • Added Note 6 regarding USB*n*_DIR pin to Table 47, “USB General Timing Parameters6.” • In Table 64, “I2C AC Electrical Specifications,” updated footnote 2. • In Table 82, , Table 83, , Table 84, added the Revision Level A for Rev 1.2
2	09/2009	**Note:** • In Section 1, “Pin Assignments and Reset States,”updated the first sentence of the note to say, “The UART_SOUT[0:1] and TEST_SEL pins must be set to a proper state during POR configuration.” • In Table 40, “SGMII DC Receiver Electrical Characteristics,” changed LSTSAB to LSTSA and LSTSEF to LSTSE for Note 4. • Updated Die value and Bump/Underfill value in Table 84 **Note:** Updated Figure 81, “Mechanical Dimensions and Bottom Surface Nomenclature of the FC-PBGA,” and its notes.
1	09/2009	• In Table 3, “Recommended Operating Conditions,” for V_{DD_CORE}, removed 1.1 ± 55 mV. • In Table 5, “Power Dissipation 5,” remove note 5. • In Table 5, ”Power Dissipation 5,” changed an “—” to “0.”
0	08/2009	• Initial public release.