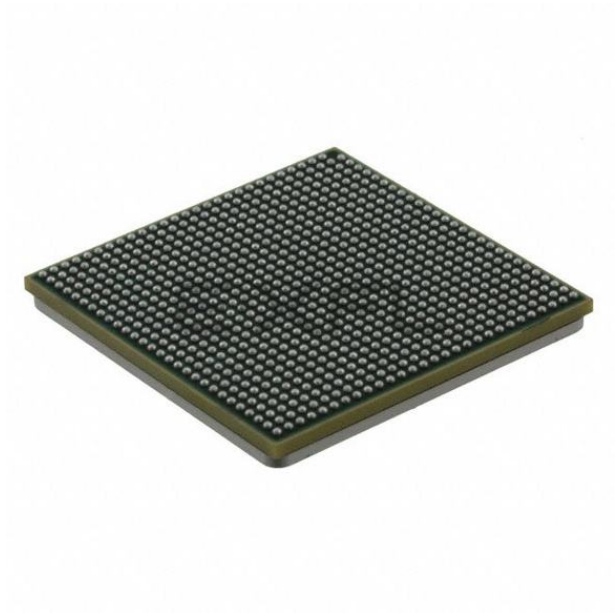


Welcome to E-XFL.COM

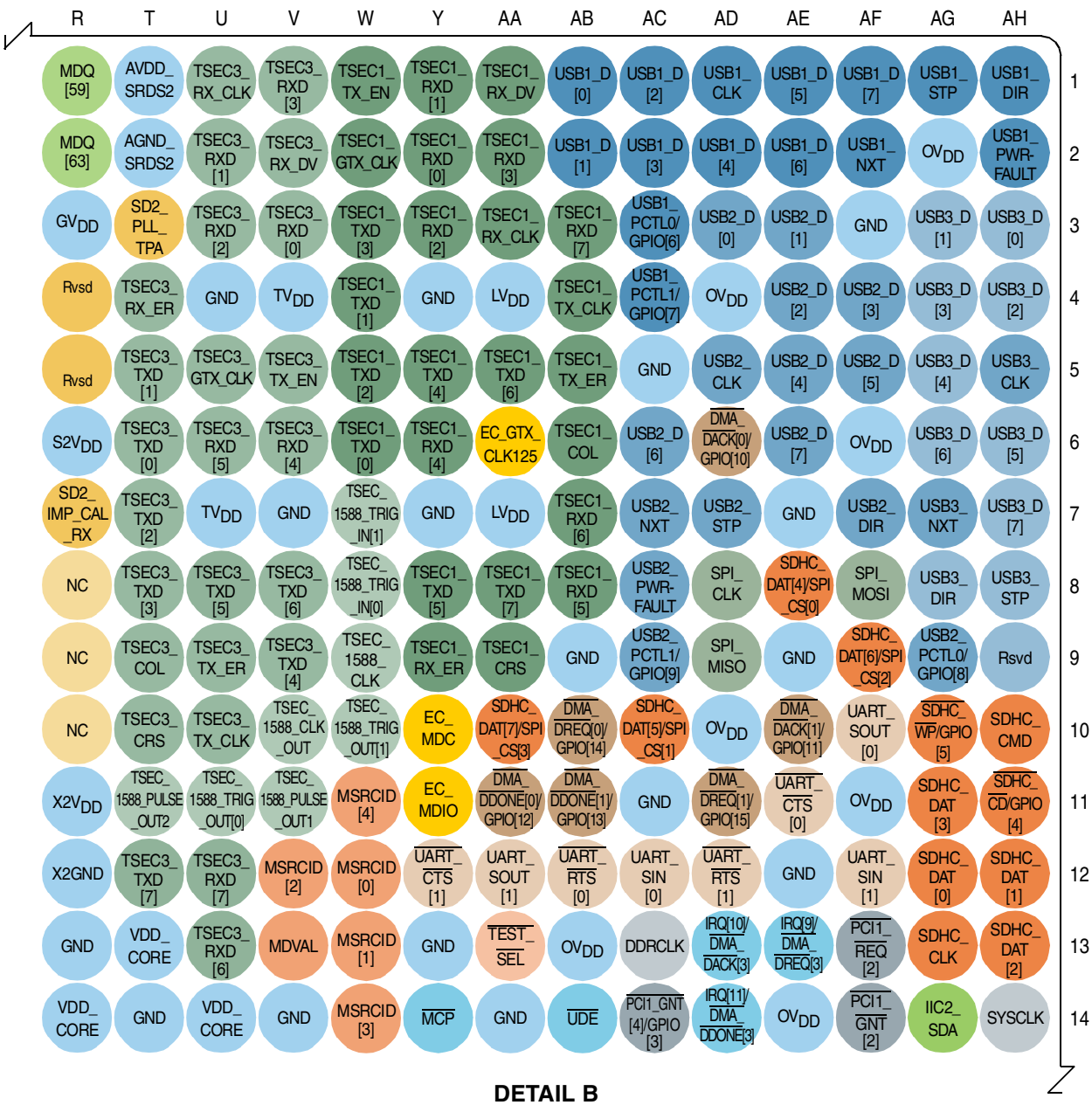
Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.25GHz
Co-Processors/DSP	Security; SEC
RAM Controllers	DDR2, DDR3
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	SATA 3Gbps (1)
USB	USB 2.0 (2)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Cryptography
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/ppc8535ecvtath



DETAIL B

Figure 4. Chip Pin Map Detail B

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
TSEC3_TX_CLK	Transmit clock In	U10	I	TV_{DD}	—
TSEC3_GTX_CLK	Transmit clock Out	U5	O	TV_{DD}	—
TSEC3_CRS	Carrier sense	T10	I/O	TV_{DD}	17
TSEC3_COL	Collision detect	T9	I	TV_{DD}	—
TSEC3_RXD[7:0]	Receive data	U12,U13,U6,V6,V1,U3, U2,V3	I	TV_{DD}	—
TSEC3_RX_DV	Receive data valid	V2	I	TV_{DD}	—
TSEC3_RX_ER	Receive data error	T4	I	TV_{DD}	—
TSEC3_RX_CLK	Receive clock	U1	I	TV_{DD}	—
IEEE 1588					
TSEC_1588_CLK	Clock In	W9	I	LV_{DD}	29
TSEC_1588_TRIG_IN[0:1]	Trigger In	W8,W7	I	LV_{DD}	29
TSEC_1588_TRIG_OUT[0:1]	Trigger Out	U11,W10	O	LV_{DD}	5,9,29
TSEC_1588_CLK_OUT	Clock Out	V10	O	LV_{DD}	5,9,29
TSEC_1588_PULSE_OUT1	Pulse Out1	V11	O	LV_{DD}	5,9,29
TSEC_1588_PULSE_OUT2	Pulse Out2	T11	O	LV_{DD}	5,9,29
eSDHC					
SDHC_CMD	Command line	AH10	I/O	OV_{DD}	29
$\overline{\text{SDHC\_CD}}$/GPIO[4]	Card detection	AH11	I	OV_{DD}	—
SDHC_DAT[0:3]	Data line	AG12,AH12,AH13, AG11	I/O	OV_{DD}	29
SDHC_DAT[4:7] / SPI_CS[0:3]	8-bit MMC Data line / SPI chip select	AE8,AC10,AF9,AA10	I/O	OV_{DD}	29
SDHC_CLK	SD/MMC/SDIO clock	AG13	I/O	OV_{DD}	29
$\overline{\text{SDHC\_WP}}$/GPIO[5]	Card write protection	AG10	I	OV_{DD}	1, 32
eSPI					
SPI_MOSI	Master Out Slave In	AF8	I/O	OV_{DD}	29
SPI_MISO	Master In Slave Out	AD9	I	OV_{DD}	29
SPI_CLK	eSPI clock	AD8	I/O	OV_{DD}	29
SPI_CS[0:3] / SDHC_DAT[4:7]	eSPI chip select / SDHC 8-bit MMC data	AE8,AC10,AF9,AA10	I/O	OV_{DD}	29
DUART					
$\overline{\text{UART\_CTS}}$[0:1]	Clear to send	AE11,Y12	I	OV_{DD}	29
$\overline{\text{UART\_RTS}}$[0:1]	Ready to send	AB12,AD12	O	OV_{DD}	29
UART_SIN[0:1]	Receive data	AC12,AF12	I	OV_{DD}	29

2.6 DDR2 and DDR3 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the chip. Note that DDR2 SDRAM is GV_{DD}(type) = 1.8 V and DDR3 SDRAM is GV_{DD}(type) = 1.5 V.

2.6.1 DDR2 and DDR3 SDRAM DC Electrical Characteristics

This table provides the recommended operating conditions for the DDR SDRAM component(s) of the chip when interfacing to DDR2 SDRAM.

Table 12. DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	1.7	1.9	V	1
I/O reference voltage	MV_{REF}	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2
I/O termination voltage	V_{TT}	MV_{REF} – 0.04	MV_{REF} + 0.04	V	3
Input high voltage	V_{IH}	MV_{REF}+ 0.125	GV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	MV_{REF} – 0.125	V	—
Output leakage current	I_{OZ}	–50	50	μA	4
Output high current (V_{OUT} = 1.420 V)	I_{OH}	–13.4	—	mA	—
Output low current (V_{OUT} = 0.280 V)	I_{OL}	13.4	—	mA	—

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the chip. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

This table provides the recommended operating conditions for the DDR SDRAM controller of the chip when interfacing to DDR3 SDRAM.

Table 13. DDR3 SDRAM Interface DC Electrical Characteristics for GV_{DD}(typ) = 1.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	1.425	1.575	V	1
I/O reference voltage	$MV_{REF}n$	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2
Input high voltage	V_{IH}	$MV_{REF}n$ + 0.100	GV_{DD}	V	—
Input low voltage	V_{IL}	GND	$MV_{REF}n$ – 0.100	V	—
Output leakage current	I_{OZ}	–50	50	μA	3

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. $MV_{REF}n$ is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on $MV_{REF}n$ may not exceed ±1% of the DC value.
3. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

2.6.2.2 DDR2 and DDR3 SDRAM Interface Output AC Timing Specifications

This table contains the output AC timing targets for the DDR2 and DDR3 SDRAM interface.

Table 19. DDR SDRAM Output AC Timing Specifications

At recommended operating conditions with GV_{DD} of 1.8 V ± 5% for DDR2 or 1.5 V ± 5% for DDR3.

Parameter	Symbol [1]	Min	Max	Unit	Notes
MCK[n] cycle time, MCK[n]/$\overline{\text{MCK}}$[n] crossing	t_{MCK}	3.0	5	ns	2
ADDR/CMD output setup with respect to MCK	t_{DDKHAS}			ns	3
667 MHz		1.10	—		7
533 MHz		1.48	—		
400 MHz		1.95	—		
ADDR/CMD output hold with respect to MCK	t_{DDKHAX}			ns	3
667 MHz		1.10	—		7
533 MHz		1.48	—		
400 MHz		1.95	—		
$\overline{\text{MCS}}$[n] output setup with respect to MCK	t_{DDKHCS}			ns	3
667 MHz		1.10	—		7
533 MHz		1.48	—		
400 MHz		1.95	—		
$\overline{\text{MCS}}$[n] output hold with respect to MCK	t_{DDKHCX}			ns	3
667 MHz		1.10	—		7
533 MHz		1.48	—		
400 MHz		1.95	—		
MCK to MDQS Skew	t_{DDKHMH}			ns	4
<= 667 MHz		–0.6	0.6		7
MDQ/MECC/MDM output setup with respect to MDQS	t_{DDKHDS}, t_{DDKLDS}			ps	5
667 MHz		450	—		7
533 MHz		538	—		
400 MHz		700	—		
MDQ/MECC/MDM output hold with respect to MDQS	t_{DDKHDX}, t_{DDKLDX}			ps	5
667 MHz		450	—		7
533 MHz		538	—		
400 MHz		700	—		
MDQS preamble start	t_{DDKHMP}			ns	6

This figure provides the AC test load for the DDR bus.

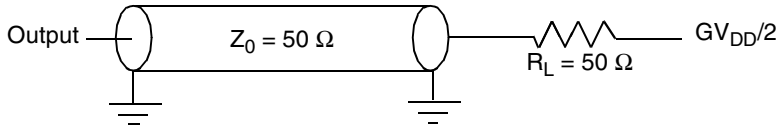


Figure 11. DDR AC Test Load

2.7 eSPI

This section describes the DC and AC electrical specifications for the eSPI of the chip.

2.7.1 eSPI DC Electrical Characteristics

This table provides the DC electrical characteristics for the chip eSPI.

Table 20. SPI DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	—	±10	μA

2.7.2 eSPI AC Timing Specifications

This table and provide the eSPI input and output AC timing specifications.

Table 21. SPI AC Timing Specifications[1]

Characteristic	Symbol [2]	Min	Max	Unit	Note
SPI_MOSI output—Master data hold time	t_{NIKHOX}	0.5	—	ns	3
	t_{NIKHOX}	4.0			4
SPI_MOSI output—Master data delay	t_{NIKHOV}	—	6.0	ns	3
	t_{NIKHOV}		7.4		4
SPI_CS outputs—Master data hold time	$t_{NIKHOX2}$	0	—	ns	—

Table 26. FIFO Mode Transmit AC Timing Specification (continued)

Parameter/Condition	Symbol	Min	Typ	Max	Unit
Rise time TX_CLK (20%–80%)	t_{FITR}	—	—	0.75	ns
Fall time TX_CLK (80%–20%)	t_{FITF}	—	—	0.75	ns
GTX_CLK to FIFO data TXD[7:0], TX_ER, TX_EN hold time	t_{FITDX}[1]	0.5	—	3.0	ns

Note:

1. Data valid t_{FITDV} to GTX_CLK Min Setup time is a function of clock period and max hold time. (Min Setup = Cycle time – Max Hold)
2. The minimum cycle period (or maximum frequency) of the RX_CLK is dependent on the maximum platform frequency of the speed bins the part belongs to as well as the FIFO mode under operation. See Section 2.4.6, "Platform to FIFO Restrictions," for more detailed description.

Table 27. FIFO Mode Receive AC Timing Specification

Parameter/Condition	Symbol	Min	Typ	Max	Unit
RX_CLK clock period[1]	t_{FIR}	6.0	8.0	100	ns
RX_CLK duty cycle	t_{FIRH}/t_{FIRH}	45	50	55	%
RX_CLK peak-to-peak jitter	t_{FIRJ}	—	—	250	ps
Rise time RX_CLK (20%–80%)	t_{FIRR}	—	—	0.75	ns
Fall time RX_CLK (80%–20%)	t_{FIRF}	—	—	0.75	ns
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t_{FIRDV}	1.5	—	—	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t_{FIRDX}	0.5	—	—	ns

Note:

1. The minimum cycle period (or maximum frequency) of the RX_CLK is dependent on the maximum platform frequency of the speed bins the part belongs to as well as the FIFO mode under operation. See Section 2.4.6, "Platform to FIFO Restrictions," for more detailed description.

Timing diagrams for FIFO appear in the following figures.

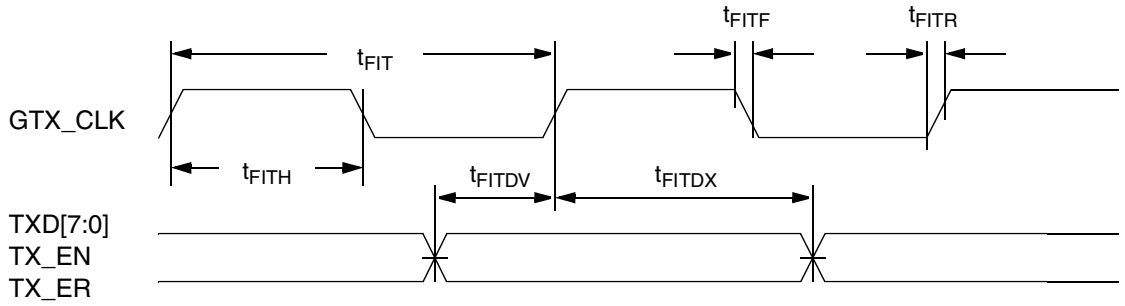


Figure 14. FIFO Transmit AC Timing Diagram

This figure shows the MII receive AC timing diagram.

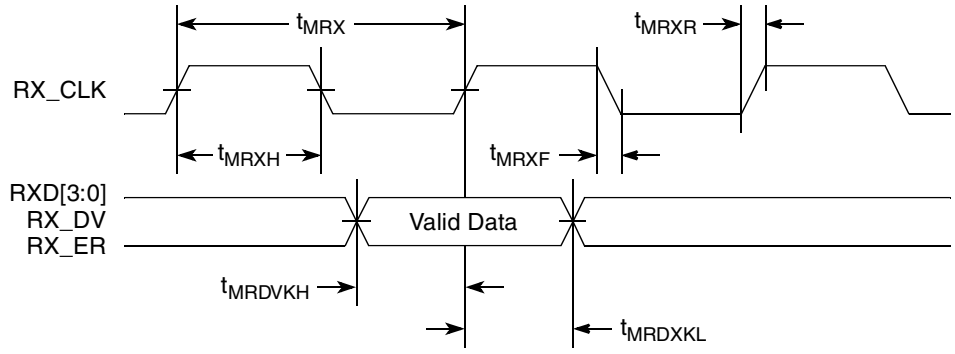


Figure 21. MII Receive AC Timing Diagram

2.9.2.4 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

2.9.2.4.1 TBI Transmit AC Timing Specifications

This table provides the TBI transmit AC timing specifications.

Table 32. TBI Transmit AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
GTX_CLK clock period	t_{TTX}	—	8.0	—	ns
GTX_CLK duty cycle	t_{TTXH}/t_{TTX}	40	—	60	%
GTX_CLK to TCG[9:0] delay time	t_{TTKHDX}[2]	1.0	—	5.0	ns
GTX_CLK rise (20%–80%)	t_{TTXR}	—	—	1.0	ns
GTX_CLK fall time (80%–20%)	t_{TTXF}	—	—	1.0	ns

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{TTKHDV} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TTX} represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Data valid t_{TTKHDV} to GTX_CLK Min Setup time is a function of clock period and max hold time. (Min Setup = Cycle time - Max Hold)

This figure shows the TBI transmit AC timing diagram.

When operating in SGMII mode, the eTSEC EC_GTX_CLK125 clock is not required for this port. Instead, SerDes reference clock is required on SD2_REF_CLK and $\overline{\text{SD2\_REF\_CLK}}$ pins.

2.9.3.1 DC Requirements for SGMII SD2_REF_CLK and SD2_REF_CLK

The characteristics and DC requirements of the separate SerDes reference clock are described in Section 2.20, "High-Speed Serial Interfaces."

2.9.3.2 AC Requirements for SGMII SD2_REF_CLK and $\overline{\text{SD2\_REF\_CLK}}$

This table lists the SGMII SerDes reference clock AC requirements. Please note that SD2_REF_CLK and $\overline{\text{SD2\_REF\_CLK}}$ are not intended to be used with, and should not be clocked by, a spread spectrum clock source.

Table 38. SD2_REF_CLK and $\overline{\text{SD2\_REF\_CLK}}$ AC Requirements

Symbol	Parameter Description	Min	Typical	Max	Units	Notes
t_{REF}	REFCLK cycle time	—	10 (8)	—	ns	1
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles	—	—	100	ps	—
t_{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location	–50	—	50	ps	2,3

Notes:

1. 8 ns applies only when 125 MHz SerDes2 reference clock frequency is selected via cfg_srds_sgmii_refclk during POR.
2. In a frequency band from 150 kHz to 15 MHz, at BER of 10E-12.
3. Total peak-to-peak deterministic jitter "Dj" should be less than or equal to 50 ps.

2.9.3.3 SGMII Transmitter and Receiver DC Electrical Characteristics

The following tables describe the SGMII SerDes transmitter and receiver AC-Coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SD2_TX[n] and $\overline{\text{SD2\_TX}}$[n]) as depicted in Figure 30.

Table 39. SGMII DC Transmitter Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	$X2V_{DD}$	0.95	1.0	1.05	V	—
Output high voltage	VOH	—	—	$X2V_{DD\text{-}Typ}/2 + \lvert V_{OD}\rvert_{-max}/2$	mV	1
Output low voltage	VOL	$X2V_{DD\text{-}Typ}/2 - \lvert V_{OD}\rvert_{-max}/2$	—	—	mV	1
Output ringing	V_{RING}	—	—	10	%	—
Output differential voltage[2, 3, 5]	$\lvert V_{OD}\rvert$	323	500	725	mV	Equalization setting: 1.0x
		296	459	665		Equalization setting: 1.09x
		269	417	604		Equalization setting: 1.2x
		243	376	545		Equalization setting: 1.33x
		215	333	483		Equalization setting: 1.5x
		189	292	424		Equalization setting: 1.71x
		162	250	362		Equalization setting: 2.0x
Output offset voltage	V_{OS}	425	500	575	mV	1, 4
Output impedance (single-ended)	R_O	40	—	60	Ω	—
Mismatch in a pair	ΔR_O	—	—	10	%	—
Change in V_{OD} between “0” and “1”	$\Delta \lvert V_{OD}\rvert$	—	—	25	mV	—
Change in V_{OS} between “0” and “1”	ΔV_{OS}	—	—	25	mV	—
Output current on short to GND	I_{SA}, I_{SB}	—	—	40	mA	—

Notes:

1. This will not align to DC-coupled SGMII. $X2V_{DD\text{-}Typ}$=1.0V.
2. $\lvert V_{OD}\rvert = \lvert V_{SD2\_TXn} - V_{\overline{SD2\_TXn}}\rvert$. $\lvert V_{OD}\rvert$ is also referred as output differential peak voltage. $V_{TX\text{-}DIFFp\text{-}p} = 2*\lvert V_{OD}\rvert$.
3. The $\lvert V_{OD}\rvert$ value shown in the table assumes the following transmit equalization setting in the XMITEQ**AB** (for SerDes 2 lanes A & B) or XMITEQ**EF** (for SerDes 2 lanes E & E) bit field of the chip’s SerDes 2 control register:
   - The MSbit (bit 0) of the above bit field is set to zero (selecting the full $V_{DD\text{-}DIFF\text{-}p\text{-}p}$ amplitude - power up default);
   - The LSbits (bit [1:3]) of the above bit field is set based on the equalization setting shown in table.
4. V_{OS} is also referred to as output common mode voltage.
   - 5.The $\lvert V_{OD}\rvert$ value shown in the Typ column is based on the condition of $X2V_{DD\text{-}Typ}$=1.0V, no common mode offset variation (VOS =550mV), SerDes2 transmitter is terminated with 100-Ω differential load between SD2_TX[n] and SD2_TX[n].

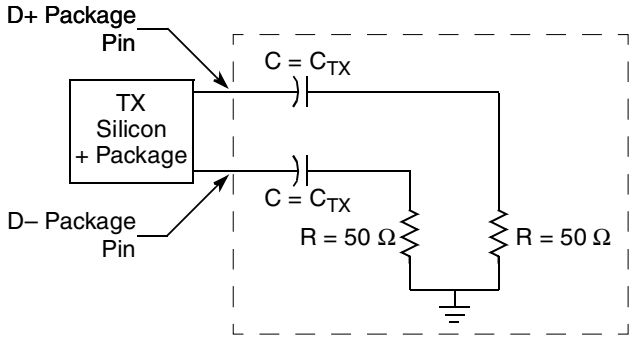


Figure 32. SGMII AC Test/Measurement Load

2.9.4 eTSEC IEEE 1588 AC Specifications

This figure shows the data and command output timing diagram.

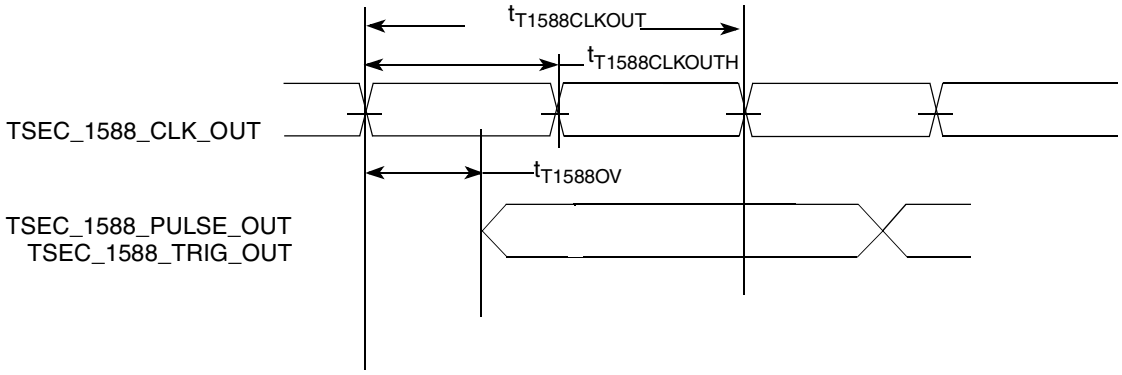


Figure 33. eTSEC IEEE 1588 Output AC timing

[1] The output delay is count starting rising edge if $t_{T1588CLKOUT}$ is non-inverting. Otherwise, it is count starting falling edge.

This figure provides the data and command input timing diagram.

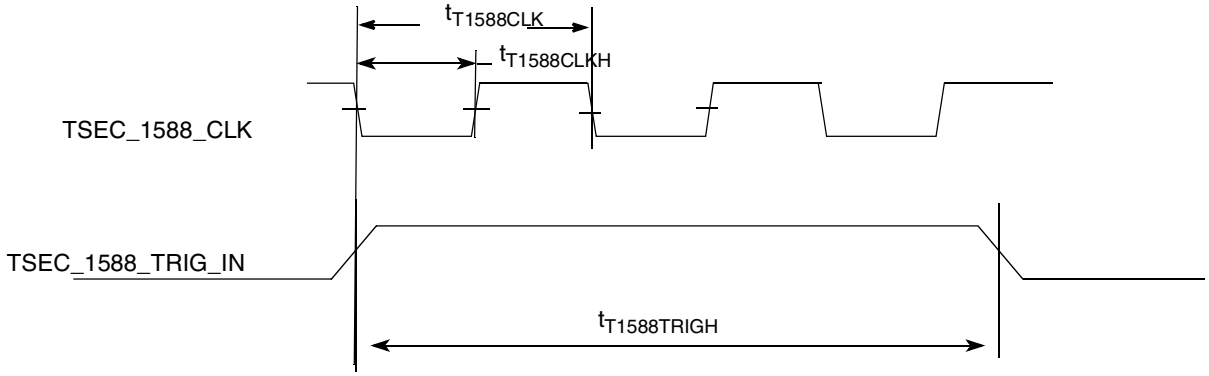


Figure 34. eTSEC IEEE 1588 Input AC timing

The IEEE 1588 AC timing specifications are in the following table.

Table 43. eTSEC IEEE 1588 AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Note
TSEC_1588_CLK clock period	$t_{T1588CLK}$	3.8	—	T_{TX_CLK}*7	ns	1
TSEC_1588_CLK duty cycle	$t_{T1588CLKH}$ /$t_{T1588CLK}$	40	50	60	%	—
TSEC_1588_CLK peak-to-peak jitter	$t_{T1588CLKINJ}$	—	—	250	ps	—
Rise time eTSEC_1588_CLK (20%–80%)	$t_{T1588CLKINR}$	1.0	—	2.0	ns	—
Fall time eTSEC_1588_CLK (80%–20%)	$t_{T1588CLKINF}$	1.0	—	2.0	ns	—
TSEC_1588_CLK_OUT clock period	$t_{T1588CLKOUT}$	2*$t_{T1588CLK}$	—	—	ns	—
TSEC_1588_CLK_OUT duty cycle	$t_{T1588CLKOTH}$ /$t_{T1588CLKOUT}$	30	50	70	%	—
TSEC_1588_PULSE_OUT	$t_{T1588OV}$	0.5	—	3.0	ns	—
TSEC_1588_TRIG_IN pulse width	$t_{T1588TRIGH}$	2*$t_{T1588CLK\_MAX}$	—	—	ns	2

Note:

1. When TMR_CTRL[CKSEL]=00, the external TSEC_1588_CLK input is selected as the 1588 timer reference clock source, with the timing defined in the Table above. The maximum value of $t_{T1588CLK}$ is defined in terms of T_{TX_CLK}, which is the maximum clock cycle period of the equivalent interface speed that the eTSEC1 port is running.
   When eTSEC1 is configured to operate in the parallel mode, the T_{TX_CLK} is the maximum clock period of the TSEC1_TX_CLK. When eTSEC1 operates in SGMII mode, the maximum value of $t_{T1588CLK}$ is defined in terms of the recovered clock from SGMII SerDes. For example, for 10/100/1000 Mbps modes, the maximum value of $t_{T1588CLK}$ will be 2800, 280, and 56 ns respectively.
   See the *MPC8536E PowerQUICC III Integrated Communications Processor Reference Manual* for a description of TMR_CTRL registers.
2. It need to be at least two times of clock period of clock selected by TMR_CTRL[CKSEL]. See the *MPC8536E PowerQUICC III Integrated Processor Reference Manual* for a description of TMR_CTRL registers.

2.10 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals EC_MDIO (management data input/output) and EC_MDC (management data clock). The electrical characteristics for GMII, SGMII, RGMII, RMII, TBI and RTBI are specified in Section 2.9, “Ethernet: Enhanced Three-Speed Ethernet (eTSEC), MII Management”

Table 51. Local Bus General Timing Parameters (BV_{DD} = 3.3 V DC) (continued)

Parameter	Symbol [1]	Min	Max	Unit	Notes
Output hold from local bus clock for LAD/LDP	$t_{LBKHOX2}$	0.7	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$t_{LBKHOZ1}$	—	2.5	ns	5
Local bus clock to output high impedance for LAD/LDP	$t_{LBKHOZ2}$	—	2.5	ns	5

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
3. All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is guaranteed with LBCR[AHD] = 0.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.

This table describes the general timing parameters of the local bus interface at BV_{DD} = 2.5 V DC.

Table 52. Local Bus General Timing Parameters (BV_{DD} = 2.5 V DC)

Parameter	Configuration	Symbol [1]	Min	Max	Unit	Notes
Local bus cycle time	—	t_{LBK}	7.5	12	ns	2
Local bus duty cycle	—	t_{LBKH}/t_{LBK}	43	57	%	—
LCLK[n] skew to LCLK[m] or LSYNC_OUT	—	$t_{LBKSKEW}$	—	150	ps	7
Input setup to local bus clock (except LUPWAIT)	—	$t_{LBIVKH1}$	1.9	—	ns	3, 4
LUPWAIT input setup to local bus clock	—	$t_{LBIVKH2}$	1.8	—	ns	3, 4
Input hold from local bus clock (except LUPWAIT)	—	$t_{LBIXKH1}$	1.1	—	ns	3, 4
LUPWAIT input hold from local bus clock	—	$t_{LBIXKH2}$	1.1	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH setup and hold time)	—	t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	—	$t_{LBKHOV1}$	—	2.4	ns	—
Local bus clock to data valid for LAD/LDP	—	$t_{LBKHOV2}$	—	2.5	ns	3
Local bus clock to address valid for LAD	—	$t_{LBKHOV3}$	—	2.4	ns	3
Local bus clock to LALE assertion	—	$t_{LBKHOV4}$	—	2.4	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	—	$t_{LBKHOX1}$	0.8	—	ns	3

2.18 GPIO

This section describes the DC and AC electrical specifications for the GPIO interface of the chip.

2.18.1 GPIO DC Electrical Characteristics

This table provides the DC electrical characteristics for the GPIO interface.

Table 65. GPIO DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	– 0.3	0.8	V
Input current (V_{IN} [1] = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA
High-level output voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V

Note:

1. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

2.18.2 GPIO AC Electrical Specifications

This table provides the GPIO input and output AC timing specifications.

Table 66. GPIO Input and Output AC Timing Specifications[1]

Characteristic	Symbol [2]	Min	Unit	Notes
GPIO inputs—minimum pulse width	t_{PIWID}	7.5	ns	3
GPIO outputs—minimum pulse width	t_{GTOWID}	12	ns	—

Notes:

1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.
3. The minimum pulse width is a function of the MPX/Platform clock. The minimum pulse width must be greater than or equal to 4 times the MPX/Platform clock period.

This figure provides the AC test load for the GPIO.

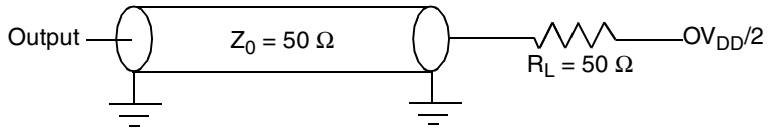


Figure 53. GPIO AC Test Load

This figure shows the PCI output AC timing conditions.

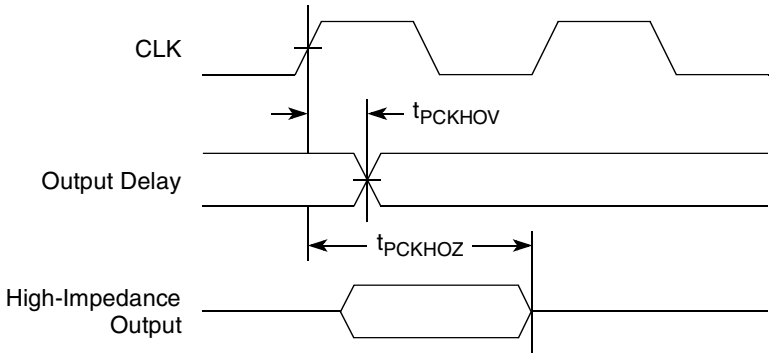


Figure 56. PCI Output AC Timing Measurement Condition

2.20 High-Speed Serial Interfaces

This chip features two Serializer/Deserializer (SerDes) interfaces to be used for high-speed serial interconnect applications. The SerDes1 interface is dedicated for PCI Express data transfers. The SerDes2 can be used for SGMII or SATA.

This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes Reference Clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

2.20.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 57 shows how the signals are defined. For illustration purposes, only one SerDes lane is used for description. The figure shows waveform for either a transmitter output (SDn_TX and $\overline{\text{SDn\_TX}}$) or a receiver input (SDn_RX and $\overline{\text{SDn\_RX}}$). Each signal swings between A Volts and B Volts where A > B.

Using this waveform, the definitions are as follows. To simplify illustration, the following definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

1. **Single-Ended Swing**

The transmitter output signals and the receiver input signals SDn_TX, $\overline{\text{SDn\_TX}}$, SDn_RX and $\overline{\text{SDn\_RX}}$ each have a peak-to-peak swing of A - B Volts. This is also referred as each signal wire's Single-Ended Swing.

2. **Differential Output Voltage, V_{OD}** (or **Differential Output Swing**):

The Differential Output Voltage (or Swing) of the transmitter, V_{OD}, is defined as the difference of the two complimentary output voltages: V_{SDn_TX} - $V_{\overline{SDn\_TX}}$. The V_{OD} value can be either positive or negative.

3. **Differential Input Voltage, V_{ID}** (or **Differential Input Swing**):

The Differential Input Voltage (or Swing) of the receiver, V_{ID}, is defined as the difference of the two complimentary input voltages: V_{SDn_RX} - $V_{\overline{SDn\_RX}}$. The V_{ID} value can be either positive or negative.

4. **Differential Peak Voltage, V_{DIFFp}**

The peak value of the differential transmitter output signal or the differential receiver input signal is defined as Differential Peak Voltage, V_{DIFFp} = |A - B| Volts.

5. **Differential Peak-to-Peak, $V_{DIFFp-p}$**

Since the differential output signal of the transmitter and the differential input signal of the receiver each range from A - B to -(A - B) Volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as Differential Peak-to-Peak Voltage, $V_{DIFFp-p} = 2*V_{DIFFp} = 2 * |(A - B)|$ Volts, which is twice of differential swing in amplitude, or twice of the differential

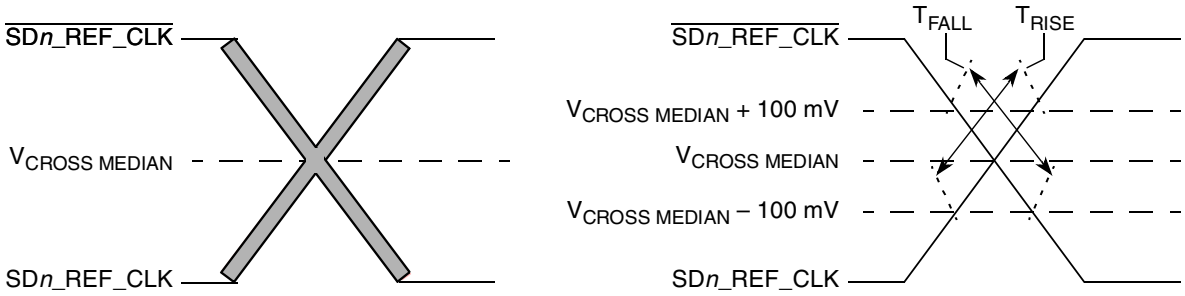


Figure 67. Single-Ended Measurement Points for Rise and Fall Time Matching

The other detailed AC requirements of the SerDes Reference Clocks is defined by each interface protocol based on application usage. See the following sections for detailed information:

- Section 2.9.3.2, "AC Requirements for SGMII SD2_REF_CLK and SD2_REF_CLK"
- Section 2.21.2, "AC Requirements for PCI Express SerDes Clocks"

2.20.2.4.1 Spread Spectrum Clock

SD1_REF_CLK/$\overline{\text{SD1\_REF\_CLK}}$ were designed to work with a spread spectrum clock (+0 to -0.5% spreading at 30–33 kHz rate is allowed), assuming both ends have same reference clock. For better results, a source without significant unintended modulation should be used.

SD2_REF_CLK/$\overline{\text{SD2\_REF\_CLK}}$ are not intended to be used with, and should not be clocked by, a spread spectrum clock source.

2.20.3 SerDes Transmitter and Receiver Reference Circuits

This figure shows the reference circuits for SerDes data lane's transmitter and receiver.

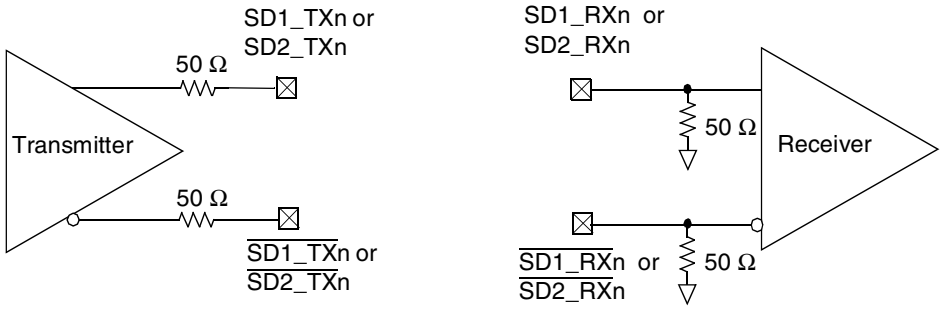


Figure 68. SerDes Transmitter and Receiver Reference Circuits

The DC and AC specification of SerDes data lanes are defined in each interface protocol section below (PCI Express, SATA or SGMII) in this document based on the application usage:

- Section 2.9.3, "SGMII Interface Electrical Characteristics"
- Section 2.21, "PCI Express"
- Section 2.16, "Serial ATA (SATA)"

Please note that external AC Coupling capacitor is required for the above three serial transmission protocols with the capacitor value defined in specification of each protocol section.

Table 71. Differential Transmitter (TX) Output Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Units	Comments
$V_{TX-DE-RATIO}$	De- Emphasized Differential Output Voltage (Ratio)	–3.0	–3.5	–4.0	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. See Note 2.
T_{TX-EYE}	Minimum TX Eye Width	0.70	—	—	UI	The maximum Transmitter jitter can be derived as $T_{TX-MAX-JITTER}$ = 1 – T_{TX-EYE}= 0.3 UI. See Notes 2 and 3.
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median.	—	—	0.15	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p}$ = 0 V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2 and 3.
$T_{TX-RISE}$, $T_{TX-FALL}$	D+/D- TX Output Rise/Fall Time	0.125	—	—	UI	See Notes 2 and 5
$V_{TX-CM-ACp}$	RMS AC Peak Common Mode Output Voltage	—	—	20	mV	$V_{TX-CM-ACp}$ = RMS(|V_{TXD+} +V_{TXD-}|/2 – $V_{TX-CM-DC}$) $V_{TX-CM-DC}$ = $DC_{(avg)}$ of |V_{TX-D+} +V_{TX-D-}|/2 See Note 2
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute Delta of DC Common Mode Voltage During L0 and Electrical Idle	0	—	100	mV	|$V_{TX-CM-DC\ (during\ L0)}$ – $V_{TX-CM-Idle-DC\ (During\ Electrical\ Idle)}$|<=100 mV $V_{TX-CM-DC}$ = $DC_{(avg)}$ of |V_{TX-D+} +V_{TX-D-}|/2 [L0] $V_{TX-CM-Idle-DC}$ = $DC_{(avg)}$ of |V_{TX-D+} + V_{TX-D-}|/2 [Electrical Idle] See Note 2.
$V_{TX-CM-DC-LINE-DELTA}$	Absolute Delta of DC Common Mode between D+ and D–	0	—	25	mV	|$V_{TX-CM-DC-D+}$ – $V_{TX-CM-DC-D-}$| <= 25 mV $V_{TX-CM-DC-D+}$ = $DC_{(avg)}$ of |V_{TX-D+}| $V_{TX-CM-DC-D-}$ = $DC_{(avg)}$ of |V_{TX-D-}| See Note 2.
$V_{TX-IDLE-DIFFp}$	Electrical Idle differential Peak Output Voltage	0	—	20	mV	$V_{TX-IDLE-DIFFp}$ = |$V_{TX-IDLE-D+}$ -$V_{TX-IDLE-D-}$| <= 20 mV See Note 2.
$V_{TX-RCV-DETECT}$	The amount of voltage change allowed during Receiver Detection	—	—	600	mV	The total amount of voltage change that a transmitter can apply to sense whether a low impedance Receiver is present. See Note 6.
$V_{TX-DC-CM}$	The TX DC Common Mode Voltage	0	—	3.6	V	The allowed DC Common Mode voltage under any conditions. See Note 6.
$I_{TX-SHORT}$	TX Short Circuit Current Limit	—	—	90	mA	The total current the Transmitter can provide when shorted to its ground
$T_{TX-IDLE-MIN}$	Minimum time spent in Electrical Idle	50	—	—	UI	Minimum time a Transmitter must be in Electrical Idle Utilized by the Receiver to start looking for an Electrical Idle Exit after successfully receiving an Electrical Idle ordered set

Careful board layout with stubless connections to these pull-down resistors coupled with the large value of the pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

The platform PLL ratio and e500 PLL ratio configuration pins are not equipped with these default pull-up devices.

3.10 JTAG Configuration Signals

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 78. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredicatable results.

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification, but it is provided on all processors built on Power Architecture technology. The chip requires $\overline{\text{TRST}}$ to be asserted during power-on reset flow to ensure that the JTAG boundary logic does not interfere with normal chip operation. While the TAP controller can be forced to the reset state using only the TCK and TMS signals, generally systems assert $\overline{\text{TRST}}$ during the power-on reset flow. Simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP), which implements the debug interface to the chip.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 78 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well.

The COP interface has a standard header, shown in Figure 79, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

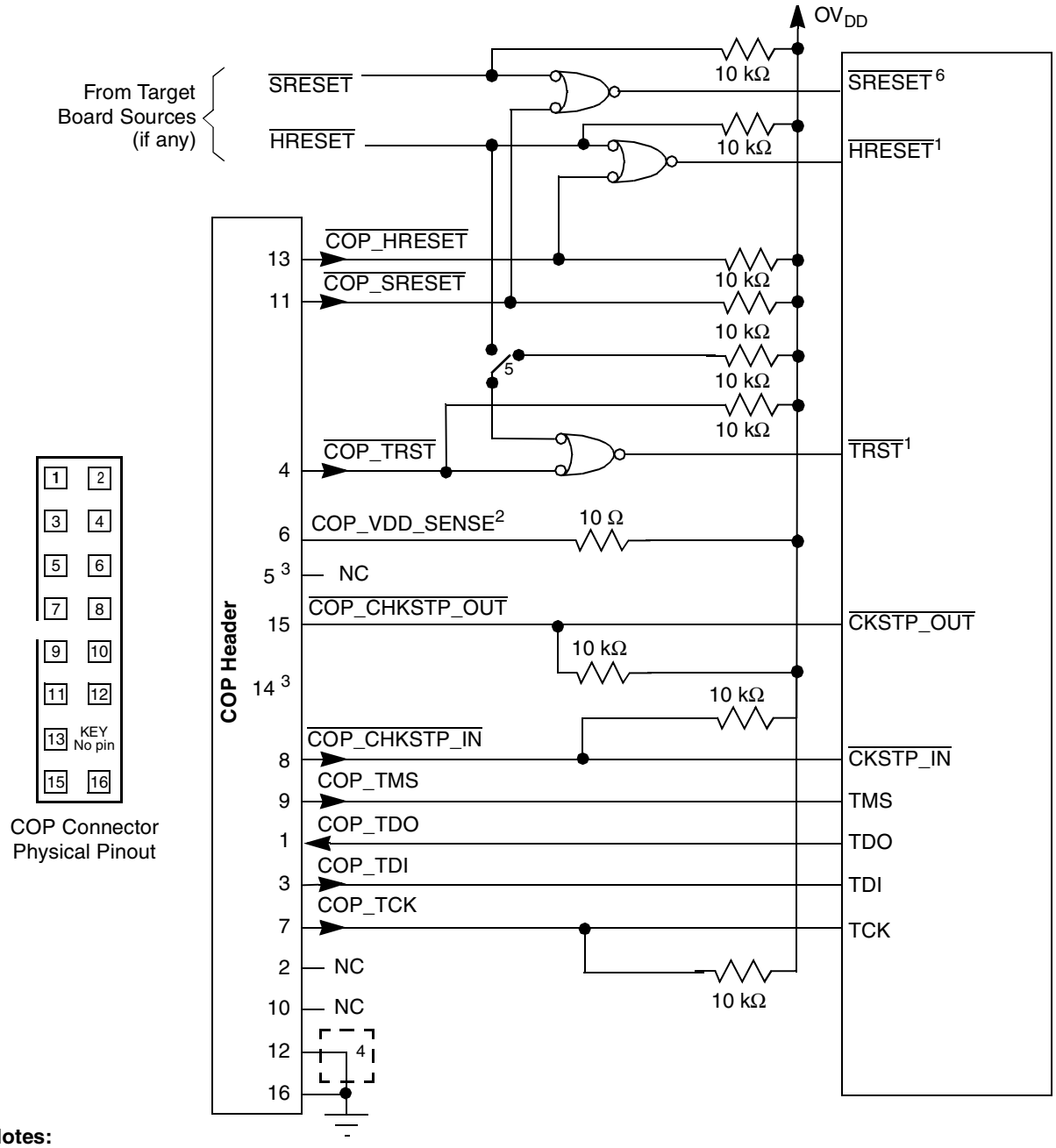
The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 79 is common to all known emulators.

3.10.1 Termination of Unused Signals

If the JTAG interface and COP header will not be used, Freescale recommends the following connections:

- $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0 kΩ isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in Figure 78. If this is not possible, the isolation resistor will allow future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.
- No pull-up/pull-down is required for TDI, TMS, or TDO.



Notes:

1. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown here.
2. Populate this with a 10 Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch should be closed to position A during BSDL testing to avoid accidentally asserting the $\overline{\text{TRST}}$ line. If BSDL testing is not being performed, this switch should be closed to position B.
6. Asserting $\overline{\text{SRESET}}$ causes a machine check interrupt to the e500 core.

Figure 78. JTAG Interface Connection

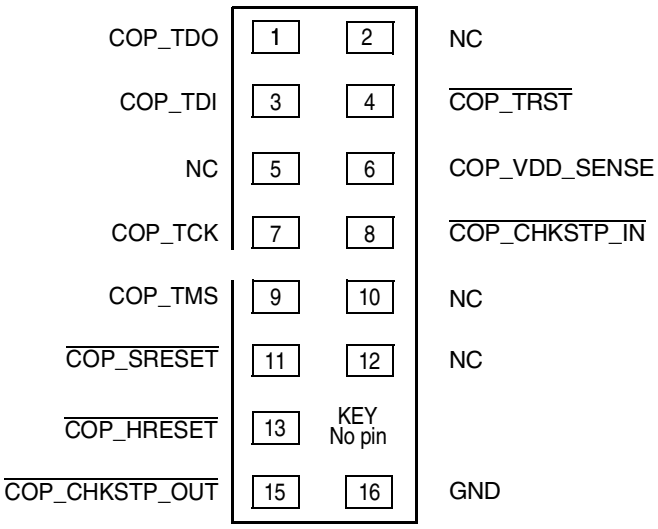


Figure 79. COP Connector Physical Pinout

3.11 Guidelines for High-Speed Interface Termination

3.11.1 SerDes1 Interface Entirely Unused

If the high-speed SerDes interface is not used at all, the unused pin should be terminated as described in this section. However, the SerDes must always have power applied to its supply pins. There are several reserved pins that need to be either left floating or connected to XGND. See SerDes1 in Table 1 for details.

The following pins must be left unconnected (float):

- SD1_TX[7:4]
- $\overline{\text{SD1\_TX[7:4]}}$
- Reserved pins T22, T23

The following pins must be connected to XGND:

- SD1_RX[7:4]
- $\overline{\text{SD1\_RX[7:4]}}$
- SD1_REF_CLK
- $\overline{\text{SD1\_REF\_CLK}}$

The POR configuration pin cfg_io_ports[0:2] on TSEC3_TXD[6:3] can be used to power down SerDes 1 block for power saving. Note that both SVDD and XVDD must remain powered.

3.11.2 SerDes 1 Interface Partly Unused

If only part of the high speed SerDes interface pins are used, the remaining high-speed serial I/O pins should be terminated as described in this section.

The following pins must be left unconnected (float) if not used:

- SD1_TX[7:4]
- $\overline{\text{SD1\_TX[7:4]}}$
- Reserved pins: T22, T23

4.1 Part Numbers Fully Addressed by this Document

This table shows the part numbering nomenclature.

Table 82. Part Numbering Nomenclature

MPC	*nnnn*	*E*	*C*	*VT*	*AA*	*X*	*R*
Product Code	**Part Identifier**	**Security Engine**	**Tiers and Temperature Range**	**Package [1]**	**Processor Frequency [2]**	**DDR Frequency [3]**	**Revision Level**
MPC	8536 8535	E = included	• A = Commercial tier standard temperature range (0° to 90°C) • B or Blank = industrial tier standard temperature range (0° to 105°C) • C = Industrial tier extended temperature range (–40° to 105°C)	• VT = FC-PBGA • (Pb-free) • PX = plastic standard	• AK = 600 MHz • AN = 800 MHz • AQ = 1000 MHz • AT = 1250 MHz • AU = 1333 MHz • AV = 1500 MHz	• G = 400 MHz • H = 500 MHz • J = 533 MHz • L = 667 MHz	• Blank = Ver. 1.0 or 1.1 (SVR = 0x803F0190, 0x803F0191) • A = Ver. 1.2 (SVR = 0x803F0192)
		Blank = not included					• Blank = Ver. 1.0 or 1.1 (SVR = 0x80370190, 0x80370191) • A = Ver. 1.2 (SVR = 0x80370192)

Notes:

1. See Section 5, “Package Information,” for more information on available package types.
2. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.
3. See Table 84 for the corresponding maximum platform frequency.