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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, IR, POR, PWM, WDT
Number of I/O	41
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 25x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8l151c8t7

Table 5. High-density and medium+ density STM8L15x pin description (continued)

Pin number				Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP80	LQFP64	UFQFPN48 and LQFP48	WLCSP32				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
44	36	-	-	PB5/SPI1_SCK/ LCD_SEG15(3)/ADC1_IN13 / *[COMP1_INP]*	I/O	FT(6)	**X**	X	X	HS	X	X	**Port B5**	SPI1 clock / LCD segment 15 / ADC1_IN13/ *[Comparator 1 positive input]*
-	-	29	D1	PB5/SPI1_SCK/ LCD_SEG15(3)/ADC1_IN13 /DAC_OUT2/ *[COMP1_INP]*	I/O	FT(6)	**X**	X	X	HS	X	X	**Port B5**	[SPI1 clock] / LCD segment 15 / ADC1_IN13 / DAC channel 2 output/ *[Comparator 1 positive input]*
45	37	-	-	PB6/SPI1_MOSI/ LCD_SEG16(3)/ADC1_IN12 /*[COMP1_INP]*	I/O	FT(6)	**X**	X	X	HS	X	X	**Port B6**	SPI1 master out/slave in/ LCD segment 16 / ADC1_IN12/ *[Comparator 1 positive input]*
-	-	30	F1	PB6/SPI1_MOSI/ LCD_SEG16(3)/ADC1_IN12 /DAC_OUT2/*[COMP1_INP]*	I/O	FT(6)	**X**	X	X	HS	X	X	**Port B6**	SPI1 master out/ slave in / LCD segment 16 / ADC1_IN12 / DAC channel 2 output/*[Comparator 1 positive input]*
46	38	31	E1	PB7/SPI1_MISO/ LCD_SEG17(3)/ ADC1_IN11/*[COMP1_INP]*	I/O	FT(6)	**X**	X	X	HS	X	X	**Port B7**	SPI1 master in- slave out/ LCD segment 17 / ADC1_IN11/*[Comparator 1 positive input]*
65	53	37	B1	PC0/I2C1_SDA	I/O	FT(6)	**X**	-	X		T(7)		**Port C0**	I2C1 data
66	54	38	A1	PC1/I2C1_SCL	I/O	FT(6)	**X**	-	X		T(7)		**Port C1**	I2C1 clock
69	57	41	B2	PC2/USART1_RX/ LCD_SEG22/ADC1_IN6/ *[COMP1_INP]* /VREFINT	I/O	FT(6)	**X**	X	X	HS	X	X	**Port C2**	USART1 receive / LCD segment 22 / ADC1_IN6/ *[Comparator 1 positive input]* /Internal reference voltage output
-	-	42	A2	PC3/USART1_TX/ LCD_SEG23(3)/ ADC1_IN5	I/O	FT(6)	**X**	X	X	HS	X	X	**Port C3**	USART1 transmit / LCD segment 23 / ADC1_IN5

Table 9. General hardware register map

Address	Block	Register label	Register name	Reset status
0x00 502E to 0x00 5049	Reserved area (28 byte)			
0x00 5050	Flash	FLASH_CR1	Flash control register 1	0x00
0x00 5051		FLASH_CR2	Flash control register 2	0x00
0x00 5052		FLASH _PUKR	Flash program memory unprotection key register	0x00
0x00 5053		FLASH _DUKR	Data EEPROM unprotection key register	0x00
0x00 5054		FLASH _IAPSR	Flash in-application programming status register	0x00
0x00 5055 to 0x00 506F	Reserved area (27 byte)			
0x00 5070	DMA1	DMA1_GCSR	DMA1 global configuration & status register	0xFC
0x00 5071		DMA1_GIR1	DMA1 global interrupt register 1	0x00
0x00 5072 to 0x00 5074		Reserved area (3 byte)		
0x00 5075		DMA1_C0CR	DMA1 channel 0 configuration register	0x00
0x00 5076		DMA1_C0SPR	DMA1 channel 0 status & priority register	0x00
0x00 5077		DMA1_C0NDTR	DMA1 number of data to transfer register (channel 0)	0x00
0x00 5078		DMA1_C0PARH	DMA1 peripheral address high register (channel 0)	0x52
0x00 5079		DMA1_C0PARL	DMA1 peripheral address low register (channel 0)	0x00
0x00 507A		Reserved area (1 byte)		
0x00 507B		DMA1_C0M0ARH	DMA1 memory 0 address high register (channel 0)	0x00
0x00 507C		DMA1_C0M0ARL	DMA1 memory 0 address low register (channel 0)	0x00
0x00 507D to 0x00 507E		Reserved area (2 byte)		
0x00 507F		DMA1_C1CR	DMA1 channel 1 configuration register	0x00
0x00 5080		DMA1_C1SPR	DMA1 channel 1 status & priority register	0x00
0x00 5081		DMA1_C1NDTR	DMA1 number of data to transfer register (channel 1)	0x00
0x00 5082		DMA1_C1PARH	DMA1 peripheral address high register (channel 1)	0x52
0x00 5083	DMA1	DMA1_C1PARL	DMA1 peripheral address low register (channel 1)	0x00

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5084	Reserved area (1 byte)			
0x00 5085	DMA1	DMA1_C1M0ARH	DMA1 memory 0 address high register (channel 1)	0x00
0x00 5086		DMA1_C1M0ARL	DMA1 memory 0 address low register (channel 1)	0x00
0x00 5087 0x00 5088	Reserved area (2 byte)			
0x00 5089	DMA1	DMA1_C2CR	DMA1 channel 2 configuration register	0x00
0x00 508A		DMA1_C2SPR	DMA1 channel 2 status & priority register	0x00
0x00 508B		DMA1_C2NDTR	DMA1 number of data to transfer register (channel 2)	0x00
0x00 508C		DMA1_C2PARH	DMA1 peripheral address high register (channel 2)	0x52
0x00 508D		DMA1_C2PARL	DMA1 peripheral address low register (channel 2)	0x00
0x00 508E	Reserved area (1 byte)			
0x00 508F		DMA1_C2M0ARH	DMA1 memory 0 address high register (channel 2)	0x00
0x00 5090		DMA1_C2M0ARL	DMA1 memory 0 address low register (channel 2)	0x00
0x00 5091 0x00 5092	Reserved area (2 byte)			
0x00 5093	DMA1	DMA1_C3CR	DMA1 channel 3 configuration register	0x00
0x00 5094		DMA1_C3SPR	DMA1 channel 3 status & priority register	0x00
0x00 5095		DMA1_C3NDTR	DMA1 number of data to transfer register (channel 3)	0x00
0x00 5096		DMA1_C3PARH_ C3M1ARH	DMA1 peripheral address high register (channel 3)	0x40
0x00 5097		DMA1_C3PARL_ C3M1ARL	DMA1 peripheral address low register (channel 3)	0x00
0x00 5098		DMA_C3M0EAR	DMA channel 3 memory 0 extended address register	0x00
0x00 5099		DMA1_C3M0ARH	DMA1 memory 0 address high register (channel 3)	0x00
0x00 509A		DMA1_C3M0ARL	DMA1 memory 0 address low register (channel 3)	0x00
0x00 509B to 0x00 509C	Reserved area (3 byte)			

Table 11. Interrupt mapping (continued)

IRQ No.	Source block	Description	Wakeup from Halt mode	Wakeup from Active-halt mode	Wakeup from Wait (WFI mode)	Wakeup from Wait (WFE mode)(1)	Vector address
20	TIM2/ USART2	Capture/Compare/USART 2 interrupt	-	-	Yes	Yes(3)	0x00 8058
21	TIM3/ USART3	TIM3 Update /Overflow/Trigger/Break/ USART3 transmission complete/transmit data register empty interrupt	-	-	Yes	Yes(3)	0x00 805C
22	TIM3/ USART3	TIM3 Capture/Compare/ USART3 Receive register data full/overrun/idle line detected/parity error/ interrupt	-	-	Yes	Yes(3)	0x00 8060
23	TIM1	Update /overflow/trigger/ COM	-	-	-	Yes(3)	0x00 8064
24	TIM1	Capture/Compare	-	-	-	Yes(3)	0x00 8068
25	TIM4	Update/overflow/trigger	-	-	Yes	Yes(3)	0x00 806C
26	SPI1	End of Transfer	Yes	Yes	Yes	Yes(3)	0x00 8070
27	USART 1/ TIM5	USART1 transmission complete/transmit data register empty/ TIM5 update/overflow/ trigger/break	-	-	Yes	Yes(3)	0x00 8074
28	USART 1/ TIM5	USART1 Receive register data full/overrun/idle line detected/parity error/ TIM5 capture/compare	-	-	Yes	Yes(3)	0x00 8078
29	I^2C1/SPI2	I^2C1 interrupt(5)/ SPI2	Yes	Yes	Yes	Yes(3)	0x00 807C

1. The Low-power wait mode is entered when executing a WFE instruction in Low-power run mode.
2. The TLI interrupt is the logic OR between TIM2 overflow interrupt, and TIM4 overflow interrupts.
3. In WFE mode, this interrupt is served if it has been previously enabled. After processing the interrupt, the processor goes back to WFE mode. When this interrupt is configured as a wakeup event, the CPU wakes up and resumes processing.
4. The interrupt from PVD is logically OR-ed with Port E and F interrupts. Register EXTI_CONF allows to select between Port E and Port F interrupt (see *External interrupt port select register (EXTI_CONF)* in the RM0031).
5. The device is woken up from Halt or Active-halt mode only when the address received matches the interface address.

Table 13. Option byte description

Option byte no.	Option description
OPT0	**ROP[7:0]** Memory readout protection (ROP) 0xAA: Disable readout protection (write access via SWIM protocol) Refer to Readout protection section in the STM8L reference manual (RM0031).
OPT1	**UBC[7:0]** Size of the user boot code area UBC[7:0] Size of the user boot code area 0x00: No UBC 0x01: Page 0 reserved for the UBC and write protected. ... 0xFF: Page 0 to 254 reserved for the UBC and write-protected. Refer to User boot code section in the STM8L reference manual (RM0031).
OPT2	**PCODESIZE[7:0]** Size of the proprietary code area 0x00: No proprietary code area 0x01: Page 0 reserved for the proprietary code and read/write protected. ... 0xFF: Page 0 to 254 reserved for the proprietary code and read/write protected. Refer to Proprietary code area (PCODE) section in the STM8L reference manual (RM0031) for more details.
OPT3	**IWDG_HW:** Independent watchdog 0: Independent watchdog activated by software 1: Independent watchdog activated by hardware
	IWDG_HALT: Independent watchdog off in Halt/Active-halt 0: Independent watchdog continues running in Halt/Active-halt mode 1: Independent watchdog stopped in Halt/Active-halt mode
	WWDG_HW: Window watchdog 0: Window watchdog activated by software 1: Window watchdog activated by hardware
	WWDG_HALT: Window window watchdog reset on Halt/Active-halt 0: Window watchdog stopped in Halt mode 1: Window watchdog generates a reset when MCU enters Halt mode
OPT4	**HSECNT**: Number of HSE oscillator stabilization clock cycles 0x00 - 1 clock cycle 0x01 - 16 clock cycles 0x10 - 512 clock cycles 0x11 - 4096 clock cycles
	LSECNT: Number of LSE oscillator stabilization clock cycles 0x00 - 1 clock cycle 0x01 - 16 clock cycles 0x10 - 512 clock cycles 0x11 - 4096 clock cycles

Table 16. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD} power line (source)	80	mA
I_{VSS}	Total current out of V_{SS} ground line (sink)	80	
I_{IO}	Output current sunk by IR_TIM pin (with high sink LED driver capability)	80	
	Output current sunk by any other I/O and control pin	25	
	Output current sourced by any I/Os and control pin	- 25	
$I_{INJ(PIN)}$	Injected current on true open-drain pins (PC0 and PC1)(1)	- 5 / +0	
	Injected current on five-volt tolerant (FT) pins(1)	- 5 / +0	
	Injected current on any other pin (2)	- 5 / +5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins) (3)	± 25	

1. Positive injection is not possible on these I/Os. A negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 15.* for maximum allowed input voltage values.
2. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 15.* for maximum allowed input voltage values.
3. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 17. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	° C
T_J	Maximum junction temperature	150	

9.3 Operating conditions

Subject to general operating conditions for V_{DD} and T_A.

9.3.1 General operating conditions

Table 18. General operating conditions

Symbol	Parameter	Conditions		Min.	Max.	Unit
f_{SYSCLK}(1)	System clock frequency	1.65 V ≤V_{DD} < 3.6 V		0	16	MHz
V_{DD}	Standard operating voltage	BOR detector disabled (D suffix version)		1.65	3.6	V
		BOR detector enabled		1.8(2)		
V_{DDA}	Analog operating voltage	ADC and DAC not used	Must be at the same potential as V_{DD}	1.65	3.6	V
		ADC or DAC used		1.8	3.6	V
P_D(3)	Power dissipation at T_A= 85 °C for suffix 6 devices	LQFP80		-	526	mW
		LQFP64		-	416	
		UFQFPN48		-	625	
		LQFP48		-	307	
		WLCSP32		-	317	
	Power dissipation at T_A= 125 °C for suffix 3 devices and at T_A= 105 °C for suffix 7 devices	LQFP80		-	131	
		LQFP64		-	104	
		UFQFPN48		-	156	
		LQFP48		-	77	
T_A	Temperature range	1.65 V ≤V_{DD} < 3.6 V (6 suffix version)		-40	85	°C
		1.65 V ≤V_{DD} < 3.6 V (7 suffix version)		-40	105	
		1.65 V ≤V_{DD} < 3.6 V (3 suffix version)		-40	125	
T_J	Junction temperature range	-40 °C ≤T_A < 85 °C (6 suffix version)		-40	105	
		-40 °C ≤ T_A < 105 °C (7 suffix version)		-40	110(4)	
		-40 °C≤ T_A < 125 °C (3 suffix version)		-40	130(4)	

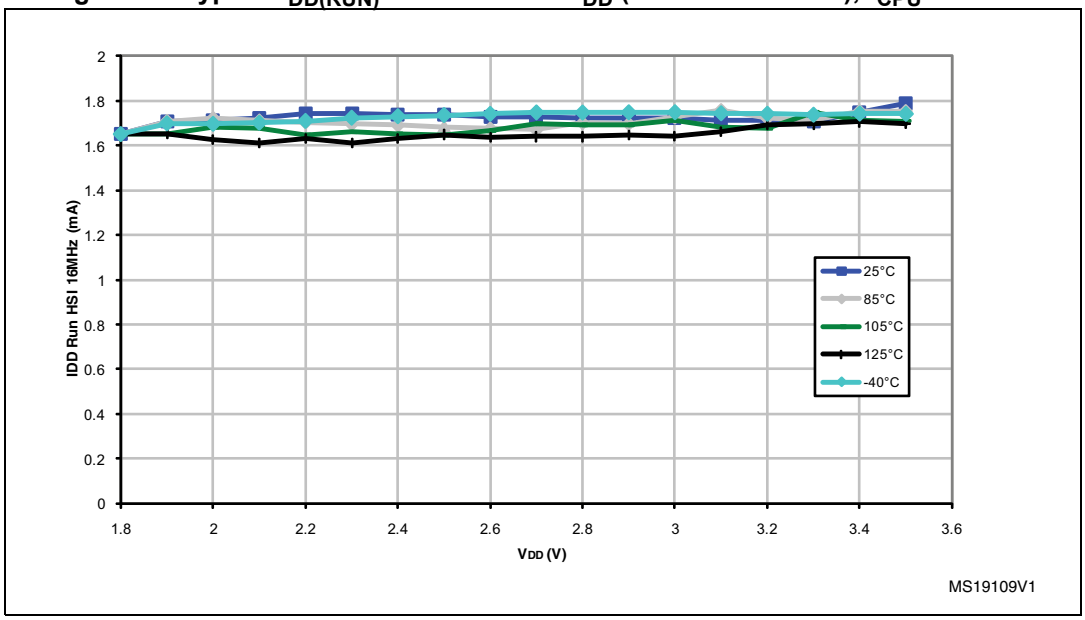
1. $f_{SYSCLK} = f_{CPU}$
2. 1.8 V at power-up, 1.65 V at power-down if BOR is disabled by option byte
3. To calculate $P_{Dmax}(T_A)$, use the formula $P_{Dmax}=(T_{Jmax} - T_A)/\Theta_{JA}$ with T_{Jmax} in this table and Θ_{JA} in “Thermal characteristics” table.
4. T_{Jmax} is given by the test limit. Above this value the product behavior is not guaranteed.

9.3.2 Embedded reset and power control block characteristics

Table 19. Embedded reset and power control block characteristics

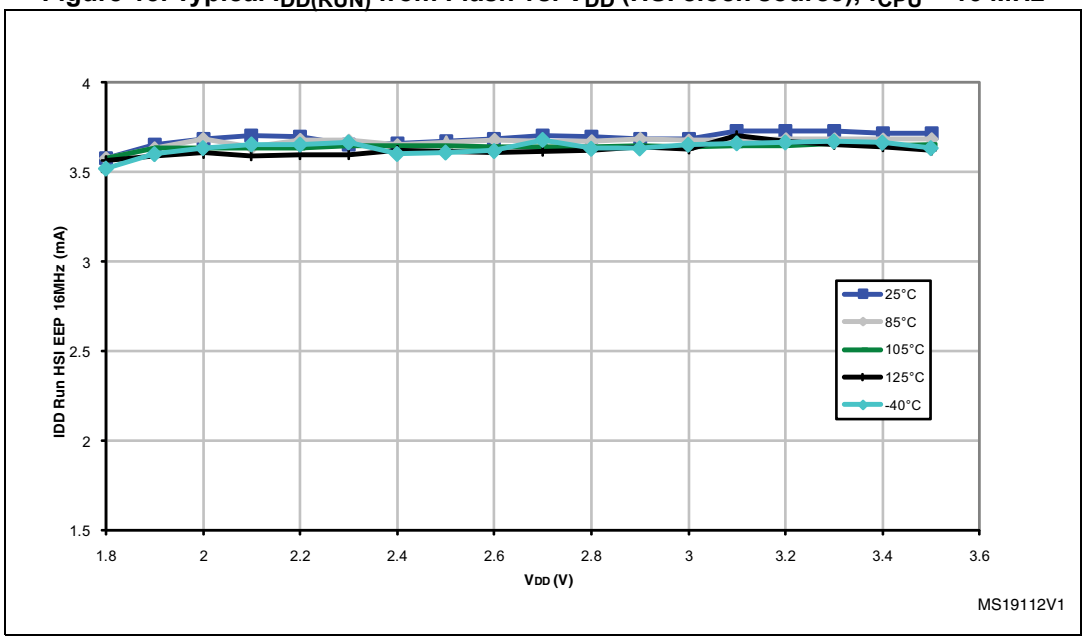
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{VDD}	V_{DD} rise time rate	BOR detector enabled	0(1)	-	∞(1)	µs/V
		BOR detector disabled	0(1)	-	1(1)	ms/V
	V_{DD} fall time rate	BOR detector enabled	20(1)	-	∞(1)	µs/V
		BOR detector disabled	Reset below voltage functional range			
t_{TEMP}	Reset release delay	V_{DD} rising BOR detector enabled	-	3	-	ms
		V_{DD} rising BOR detector disabled	-	1	-	
V_{POR}	Power-on reset threshold	Rising edge	1.3(2)	1.5	1.65	V
V_{PDR}	Power-down reset threshold	Falling edge	1.3(2)	1.5	1.65	
V_{BOR0}	Brown-out reset threshold 0 (BOR_TH[2:0]=000)	Falling edge	1.67	1.7	1.74	
		Rising edge	1.69	1.75	1.80	
V_{BOR1}	Brown-out reset threshold 1 (BOR_TH[2:0]=001)	Falling edge	1.87	1.93	1.97	
		Rising edge	1.96	2.04	2.07	
V_{BOR2}	Brown-out reset threshold 2 (BOR_TH[2:0]=010)	Falling edge	2.22	2.3	2.35	
		Rising edge	2.31	2.41	2.44	
V_{BOR3}	Brown-out reset threshold 3 (BOR_TH[2:0]=011)	Falling edge	2.45	2.55	2.60	
		Rising edge	2.54	2.66	2.7	
V_{BOR4}	Brown-out reset threshold 4 (BOR_TH[2:0]=100)	Falling edge	2.68	2.80	2.85	
		Rising edge	2.78	2.90	2.95	

Figure 14. Typical $I_{DD(RUN)}$ from RAM vs. V_{DD} (HSI clock source), f_{CPU} =16 MHz



1. Typical current consumption measured with code executed from RAM.

Figure 15. Typical $I_{DD(RUN)}$ from Flash vs. V_{DD} (HSI clock source), f_{CPU} = 16 MHz



1. Typical current consumption measured with code executed from Flash.

Table 21. Total current consumption in Wait mode (continued)

Symbol	Parameter	Conditions[1]			Typ	Max				Unit
						55°C	85 °C (2)	105 °C (3)	125 °C (4)	
$I_{DD(Wait)}$	Supply current in Wait mode	CPU not clocked, all peripherals OFF, code executed from Flash, V_{DD} from 1.65 V to 3.6 V	HSI	f_{CPU} = 125 kHz	0.27	0.36	0.42	0.46	0.51	mA
				f_{CPU} = 1 MHz	0.29	0.38	0.44	0.48	0.53	
				f_{CPU} = 4 MHz	0.37	0.46	0.52	0.56	0.61	
				f_{CPU} = 8 MHz	0.45	0.55	0.61	0.65	0.7	
				f_{CPU} = 16 MHz	0.69	0.79	0.85	0.89	0.94	
			HSE[7] external clock (f_{CPU}= HSE)	f_{CPU} = 125 kHz	0.23	0.29	0.32	0.4	0.47	
				f_{CPU} = 1 MHz	0.24	0.31	0.34	0.41	0.48	
				f_{CPU} = 4 MHz	0.32	0.39	0.42	0.49	0.56	
				f_{CPU} = 8 MHz	0.42	0.49	0.51	0.59	0.66	
				f_{CPU} = 16 MHz	0.7	0.77	0.79	0.87	0.94	
			LSI	$f_{CPU} = f_{LSI}$	0.037	0.085	0.105	0.123	0.153	
			LSE[8] external clock (32.768 kHz)	$f_{CPU} = f_{LSE}$	0.036	0.082	0.095	0.119	0.133	

1. All peripherals OFF, V_{DD} from 1.65 V to 3.6 V, HSI internal RC osc., $f_{CPU} = f_{SYSCLK}$
2. For devices with suffix 6.
3. For devices with suffix 7.
4. For devices with suffix 3.
5. Flash is configured in I_{DDQ} mode in Wait mode by setting the EPM or WAITM bit in the Flash_CR1 register.
6. Tested in production.
7. Oscillator bypassed (HSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the HSE consumption ($I_{DD\ HSE}$) must be added. Refer to *Table 31*.
8. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD\ HSE}$) must be added. Refer to *Table 32*

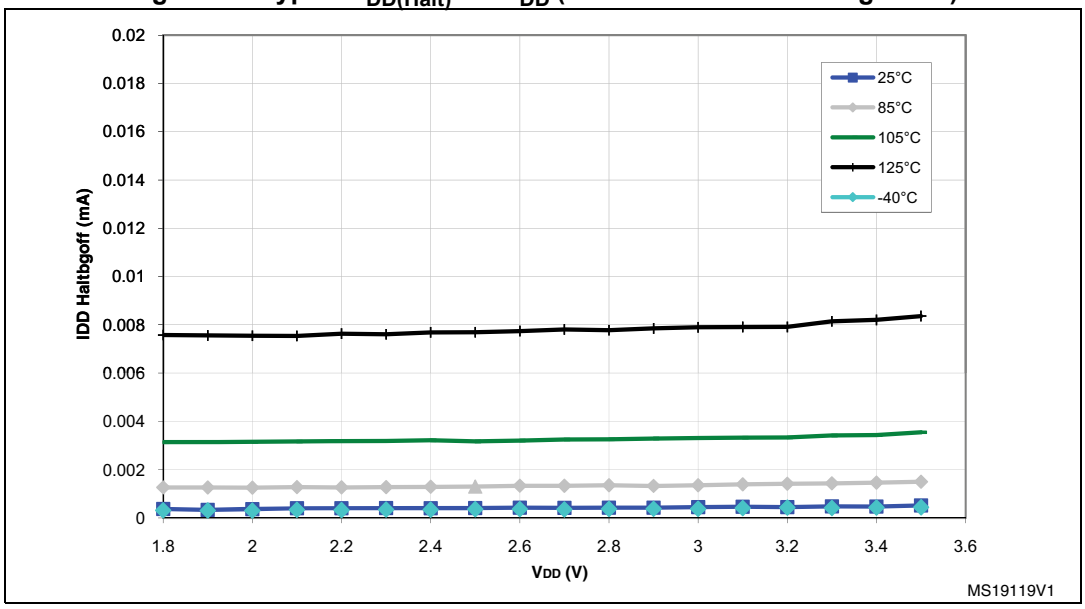
In the following table, data are based on characterization results, unless otherwise specified.

Table 26. Total current consumption and timing in Halt mode at V_{DD} = 1.65 to 3.6 V

Symbol	Parameter	Condition(1)	Typ.	Max.	Unit
$I_{DD(Halt)}$	Supply current in Halt mode (Ultra-low-power ULP bit =1 in the PWR_CSR2 register)	T_A = -40 °C to 25 °C	400	1600(2)	nA
		T_A = 55 °C	810	2400	
		T_A = 85 °C	1600	4500(2)	
		T_A = 105 °C	2900	7700(2)	
		T_A = 125 °C	5.6	18(2)	µA
$I_{DD(WUHalt)}$	Supply current during wakeup time from Halt mode (using HSI)		2.4		mA
$t_{WU\_HSI(Halt)}$(3)(4)	Wakeup time from Halt to Run mode (using HSI)		4.7	7	µs
$t_{WU\_LSI(Halt)}$(3)(4)	Wakeup time from Halt mode to Run mode (using LSI)		150		µs

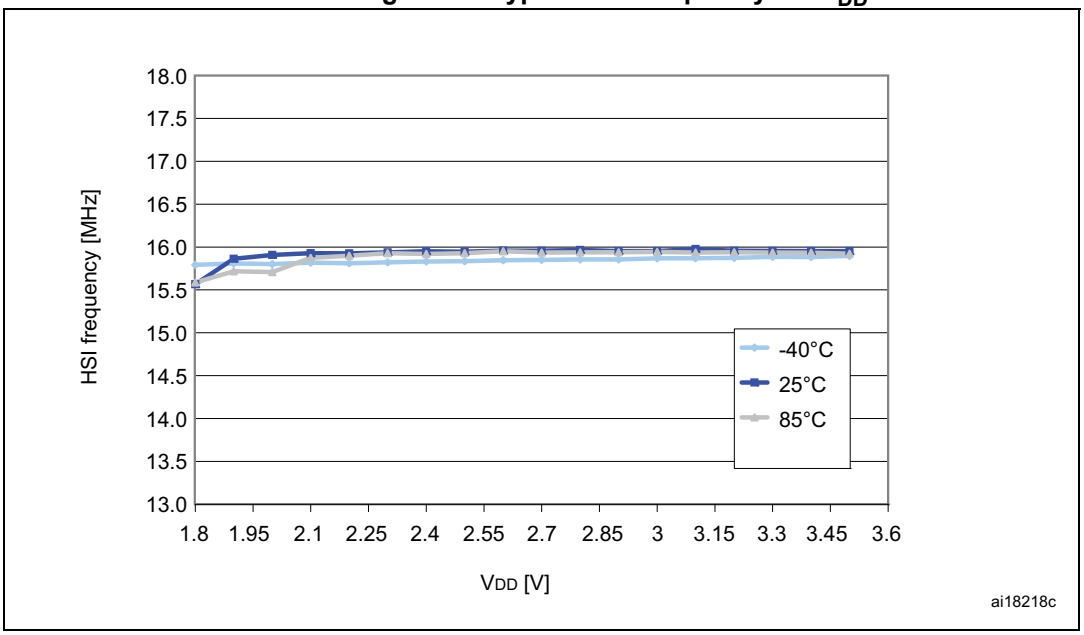
1. T_A = -40 to 125 °C, no floating I/O, unless otherwise specified
2. Tested in production
3. ULP=0 or ULP=1 and FWU=1 in the PWR_CSR2 register
4. Wakeup time until start of interrupt vector fetch.
   The first word of interrupt routine is fetched 4 CPU cycles after t_{WU}

Figure 21. Typical $I_{DD(Halt)}$ vs. V_{DD} (internal reference voltage OFF)



4. Guaranteed by design.

Figure 24. Typical HSI frequency vs. V_{DD}



Low speed internal RC oscillator (LSI)

In the following table, data are based on characterization results.

Table 34. LSI oscillator characteristics

Symbol	Parameter	Conditions(1)	Min.	Typ.	Max.	Unit
f_{LSI}	Frequency		26	38	56	kHz
$t_{su(LSI)}$	LSI oscillator wakeup time				200(2)	µs
$D_{(LSI)}$	LSI oscillator frequency drift(3)	0 °C ≤T_A ≤85 °C	-12		11	%

1. V_{DD} = 1.65 V to 3.6 V, T_A = -40 to 125 °C unless otherwise specified.
2. Guaranteed by design.
3. This is a deviation for an individual part, once the initial frequency has been measured.

9.3.6 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error, out of spec current injection on adjacent pins or other functional failure (for example reset, oscillator frequency deviation, LCD levels, etc.).

The test results are given in the following table.

Table 37. I/O current injection susceptibility

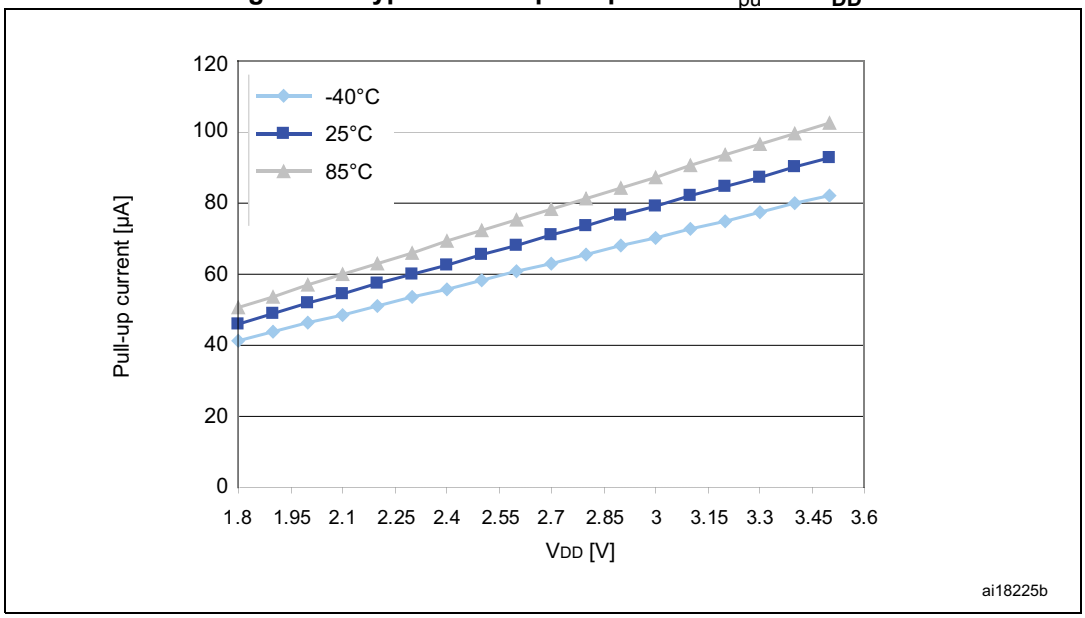
Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on true open-drain pins	-5	+0	mA
	Injected current on all 5 V tolerant (FT) pins	-5	+0	
	Injected current on any other pin	-5	+5	

9.3.7 I/O port pin characteristics

General characteristics

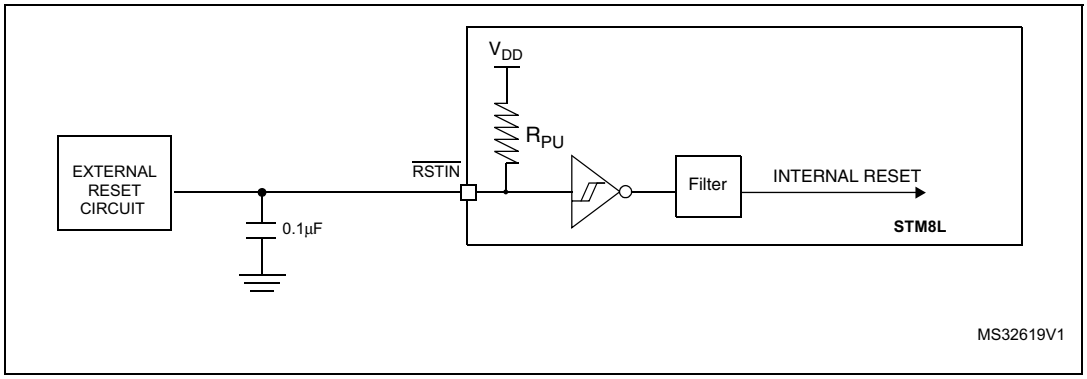
Subject to general operating conditions for V_{DD} and T_A unless otherwise specified. All unused pins must be kept at a fixed voltage: using the output mode of the I/O for example or an external pull-up or pull-down resistor.

Figure 37. Typical NRST pull-up current I_{pu} vs. V_{DD}



The reset network shown in *Figure 38* protects the device against parasitic resets. The user must ensure that the level on the NRST pin can go below the V_{IL} max. level specified in *Table 42*. Otherwise the reset is not taken into account internally. For power consumption-sensitive applications, the capacity of the external reset capacitor can be reduced to limit the charge/discharge current. If the NRST signal is used to reset the external circuitry, the user must pay attention to the charge/discharge time of the external capacitor to meet the reset timing conditions of the external devices. The minimum recommended capacity is 10 nF.

Figure 38. Recommended NRST pin configuration



9.3.10 Embedded reference voltage

In the following table, data are based on characterization results unless otherwise specified.

Table 46. Reference voltage characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{REFINT}	Internal reference voltage consumption	-	-	1.4		µA
$T_{S\_VREFINT}$(1)(2)	ADC sampling time when reading the internal reference voltage	-	-	5	10	µs
I_{BUF}(1)	Internal reference voltage buffer consumption (used for ADC)	-	-	13.5	25	µA
$V_{REFINT\ out}$	Reference voltage output	-	1.202 (3)	1.224	1.242 (3)	V
I_{LPBUF}(1)	Internal reference voltage low-power buffer consumption (used for comparators or output)	-	-	730	1200	nA
I_{REFOUT}(1)(4)	Buffer output current	-	-		1	µA
C_{REFOUT}	Reference voltage output load	-	-		50	pF
$t_{VREFINT}$(1)	Internal reference voltage startup time	-	-	2	3	ms
t_{BUFEN}(1)(2)	Internal reference voltage buffer startup time once enabled	-	-		10	µs
$ACC_{VREFINT}$(5)	Accuracy of V_{REFINT} stored in the VREFINT_Factory_CONV byte	-	-		± 5	mV
$STAB_{VREFINT}$	Stability of V_{REFINT} over temperature	-40 °C ≤T_A ≤ 125 °C	-	20	50	ppm/°C
	Stability of V_{REFINT} over temperature	0 °C ≤T_A ≤ 50 °C	-	-	20	ppm/°C
$STAB_{VREFINT}$	Stability of V_{REFINT} after 1000 hours	-	-	-	1000	ppm

1. Guaranteed by design.
2. Defined when ADC output reaches its final value ±1/2LSB
3. Tested in production at V_{DD} = 3 V ±10 mV.
4. To guarantee less than 1% V_{REFOUT} deviation
5. Measured at V_{DD} = 3 V ±10 mV. This value takes into account V_{DD} accuracy and ADC conversion accuracy.

Figure 43. ADC1 accuracy characteristics

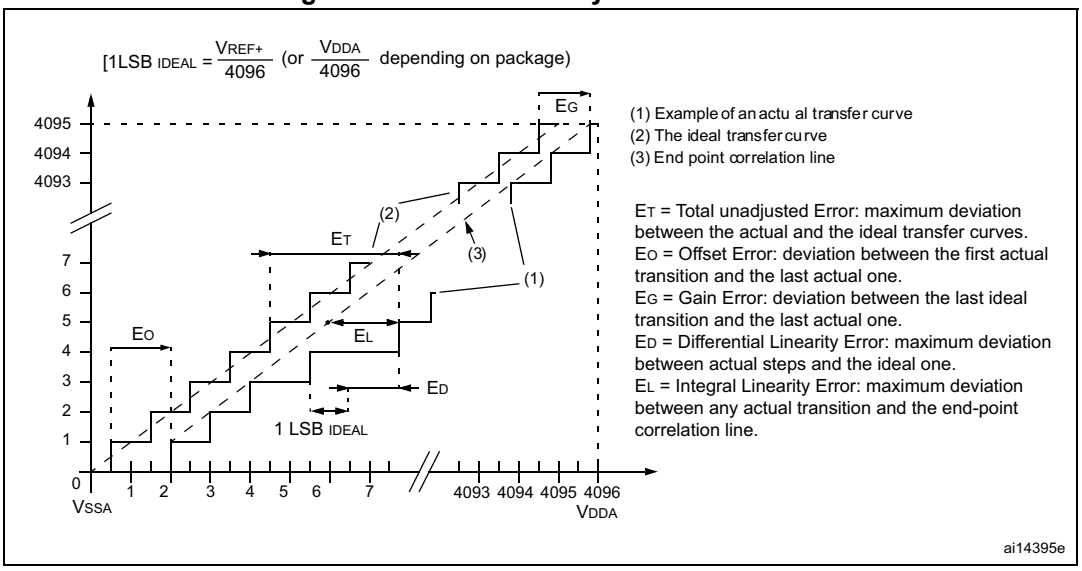
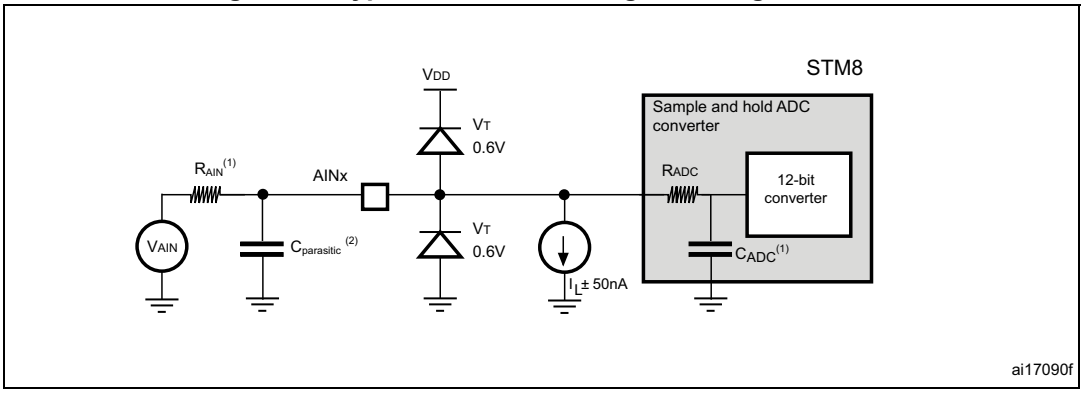


Figure 44. Typical connection diagram using the ADC



1. Refer to *Table 53* for the values of R_{AIN} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

Figure 45. Maximum dynamic current consumption on V_{REF+} supply pin during ADC conversion

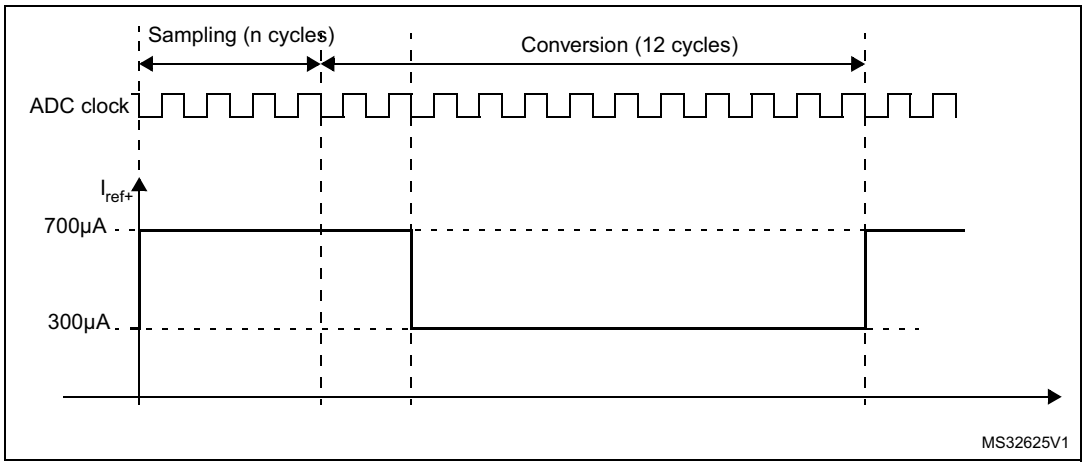


Table 57. R_{AIN} max for f_{ADC} = 16 MHz(1)

Ts (cycles)	Ts (µs)	R_{AIN} max (kohm)			
		Slow channels		Fast channels	
		2.4 V < V_{DDA} < 3.6 V	1.8 V < V_{DDA} < 2.4 V	2.4 V < V_{DDA} < 3.3 V	1.8 V < V_{DDA} < 2.4 V
4	0.25	Not allowed	Not allowed	0.7	Not allowed
9	0.5625	0.8	Not allowed	2.0	1.0
16	1	2.0	0.8	4.0	3.0
24	1.5	3.0	1.8	6.0	4.5
48	3	6.8	4.0	15.0	10.0
96	6	15.0	10.0	30.0	20.0
192	12	32.0	25.0	50.0	40.0
384	24	50.0	50.0	50.0	50.0

1. Guaranteed by design.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 46* or *Figure 47*, depending on whether V_{REF+} is connected to V_{DDA} or not. Good quality ceramic 10 nF capacitors should be used. They should be placed as close as possible to the chip.

Electromagnetic interference (EMI)

Based on a simple application running on the product (toggling 2 LEDs through the I/O ports), the product is monitored in terms of emission. This emission test is in line with the norm IEC61967-2 which specifies the board and the loading of each pin.

Table 59. EMI data (1)

Symbol	Parameter	Conditions	Monitored frequency band	Max vs.	Unit
				16 MHz	
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = +25 °C, LQFP80 conforming to IEC61967-2	0.1 MHz to 30 MHz	10	dBµV
			30 MHz to 130 MHz	4	
			130 MHz to 1 GHz	1	
			SAE EMI Level	1.5	-

1. Not tested in production.

Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). Two models can be simulated: human body model and charge device model. This test conforms to the JESD22-A114A/C101 or ANSI/ESD STM5.3.1 standards.

Table 60. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Package	Class	Maximum value (1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to JESD22-A414	All	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to ANSI/ESD STM5.3.1	WLCSP32	TBD	TBD	
		T_A = +25 °C, conforming to JESD22-C101	All other	II	500	

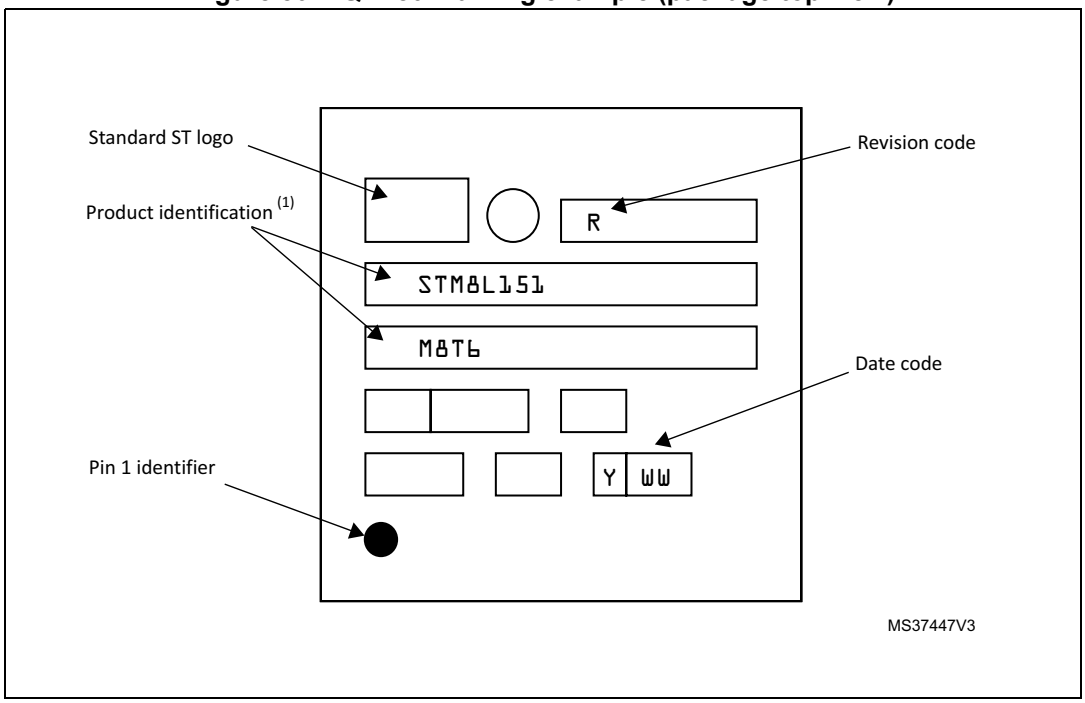
1. Data based on characterization results.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 50. LQFP80 marking example (package top view)



1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.