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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, IR, POR, PWM, WDT
Number of I/O	41
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 25x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-UFQFN Exposed Pad
Supplier Device Package	48-UFQFPN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8l151c8u6

List of figures

Table 5. High-density and medium+ density STM8L15x pin description (continued)

Pin number				Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP80	LQFP64	UFQFPN48 and LQFP48	WLCSP32				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
44	36	-	-	PB5/SPI1_SCK/ LCD_SEG15(3)/ADC1_IN13 / *[COMP1_INP]*	I/O	FT(6)	**X**	X	X	HS	X	X	**Port B5**	SPI1 clock / LCD segment 15 / ADC1_IN13/ *[Comparator 1 positive input]*
-	-	29	D1	PB5/SPI1_SCK/ LCD_SEG15(3)/ADC1_IN13 /DAC_OUT2/ *[COMP1_INP]*	I/O	FT(6)	**X**	X	X	HS	X	X	**Port B5**	[SPI1 clock] / LCD segment 15 / ADC1_IN13 / DAC channel 2 output/ *[Comparator 1 positive input]*
45	37	-	-	PB6/SPI1_MOSI/ LCD_SEG16(3)/ADC1_IN12 /*[COMP1_INP]*	I/O	FT(6)	**X**	X	X	HS	X	X	**Port B6**	SPI1 master out/slave in/ LCD segment 16 / ADC1_IN12/ *[Comparator 1 positive input]*
-	-	30	F1	PB6/SPI1_MOSI/ LCD_SEG16(3)/ADC1_IN12 /DAC_OUT2/*[COMP1_INP]*	I/O	FT(6)	**X**	X	X	HS	X	X	**Port B6**	SPI1 master out/ slave in / LCD segment 16 / ADC1_IN12 / DAC channel 2 output/*[Comparator 1 positive input]*
46	38	31	E1	PB7/SPI1_MISO/ LCD_SEG17(3)/ ADC1_IN11/*[COMP1_INP]*	I/O	FT(6)	**X**	X	X	HS	X	X	**Port B7**	SPI1 master in- slave out/ LCD segment 17 / ADC1_IN11/*[Comparator 1 positive input]*
65	53	37	B1	PC0/I2C1_SDA	I/O	FT(6)	**X**	-	X		T(7)		**Port C0**	I2C1 data
66	54	38	A1	PC1/I2C1_SCL	I/O	FT(6)	**X**	-	X		T(7)		**Port C1**	I2C1 clock
69	57	41	B2	PC2/USART1_RX/ LCD_SEG22/ADC1_IN6/ *[COMP1_INP]* /VREFINT	I/O	FT(6)	**X**	X	X	HS	X	X	**Port C2**	USART1 receive / LCD segment 22 / ADC1_IN6/ *[Comparator 1 positive input]* /Internal reference voltage output
-	-	42	A2	PC3/USART1_TX/ LCD_SEG23(3)/ ADC1_IN5	I/O	FT(6)	**X**	X	X	HS	X	X	**Port C3**	USART1 transmit / LCD segment 23 / ADC1_IN5

Table 5. High-density and medium+ density STM8L15x pin description (continued)

Pin number				Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP80	LQFP64	UFQFPN48 and LQFP48	WLCSP32				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
48	-	-	-	V_{SS4}	S	-	-	-	-	-	-	-	IOs ground voltage	
47	-	-	-	V_{DD4}	S	-	-	-	-	-	-	-	IOs supply voltage	

1. At power-up, the PA1/NRST pin is a reset input pin with pull-up. To be used as a general purpose pin (PA1), it can be configured only as output push-pull, not as output open-drain nor as a general purpose input. Refer to Section *Configuring NRST/PA1 pin as general purpose output* in the STM8L15xxx and STM8L16xxx reference manual (RM0031).
2. [ ] Alternate function remapping option (if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).
3. Available on STM8L152x6/8 devices only.
4. Even if this I/O is not available on the device pin, it is considered as active and must be configured to input pull up or output mode by software to avoid spurious behavior and increased consumption.
5. A pull-up is applied to PB0 and PB4 during the reset phase. These two pins are input floating after reset release.
6. In the 5 V tolerant I/Os, the protection diode to V_{DD} is not implemented.
7. In the open-drain output column, 'T' defines a true open-drain I/O (P-buffer, weak pull-up and protection diode to V_{DD} are not implemented).
8. Available on STM8L152xx devices only. On STM8L151xx devices it is reserved and must be tied to V_{DD}.
9. The PA0 pin is in input pull-up during the reset phase and after reset release.
10. High Sink LED driver capability available on PA0.

Note: Slope control of all GPIO pins can be programmed except true open drain pins and by default is limited to 2 MHz.

System configuration options

As shown in *Table 5: High-density and medium+ density STM8L15x pin description*, some alternate functions can be remapped on different I/O ports by programming one of the two remapping registers described in the "Routing interface (RI) and system configuration controller" section in the STM8L05xxx, STM8L15xxx and STM8L16xxx reference manual (RM0031).

Table 6. Flash and RAM boundary addresses

Memory area	Size	Start address	End address
RAM	2 Kbyte	0x00 0000	0x00 07FF
	4 Kbyte	0x00 0000	0x00 0FFF
Flash program memory	32 Kbyte	0x00 8000	0x00 FFFF
	64 Kbyte		0x01 7FFF

5.2 Register map

Table 7. Factory conversion registers

Address	Block	Register label	Register name	Reset status
0x00 4910	-	VREFINT_Factory_CONV(1)	Internal reference voltage factory conversion	0xXX
0x00 4911	-	TS_Factory_CONV_V90(2)	Temperature sensor output voltage	0xXX

1. The VREFINT_Factory_CONV byte represents the 8 LSB of the result of the VREFINT 12-bit ADC conversion performed in factory. The 2 MSB have a fixed value: 0x6.
2. The TS_Factory_CONV_V90 byte represents the 8 LSB of the result of the V90 12-bit ADC conversion performed in factory. The 2 MSB have a fixed value: 0x3.

Table 8. I/O port hardware register map

Address	Block	Register label	Register name	Reset status
0x00 5000	Port A	PA_ODR	Port A data output latch register	0x00
0x00 5001		PA_IDR	Port A input pin value register	0xXX
0x00 5002		PA_DDR	Port A data direction register	0x00
0x00 5003		PA_CR1	Port A control register 1	0x01
0x00 5004		PA_CR2	Port A control register 2	0x00
0x00 5005	Port B	PB_ODR	Port B data output latch register	0x00
0x00 5006		PB_IDR	Port B input pin value register	0xXX
0x00 5007		PB_DDR	Port B data direction register	0x00
0x00 5008		PB_CR1	Port B control register 1	0x00
0x00 5009		PB_CR2	Port B control register 2	0x00
0x00 500A	Port C	PC_ODR	Port C data output latch register	0x00
0x00 500B		PB_IDR	Port C input pin value register	0xXX
0x00 500C		PC_DDR	Port C data direction register	0x00
0x00 500D		PC_CR1	Port C control register 1	0x00
0x00 500E		PC_CR2	Port C control register 2	0x00

8 Unique ID

STM8 devices feature a 96-bit unique device identifier which provides a reference number that is unique for any device and in any context. The 96 bits of the identifier can never be altered by the user.

The unique device identifier can be read in single bytes and may then be concatenated using a custom algorithm.

The unique device identifier is ideally suited:

- For use as serial numbers
- For use as security keys to increase the code security in the program memory while using and combining this unique ID with software cryptographic primitives and protocols before programming the internal memory.
- To activate secure boot processes

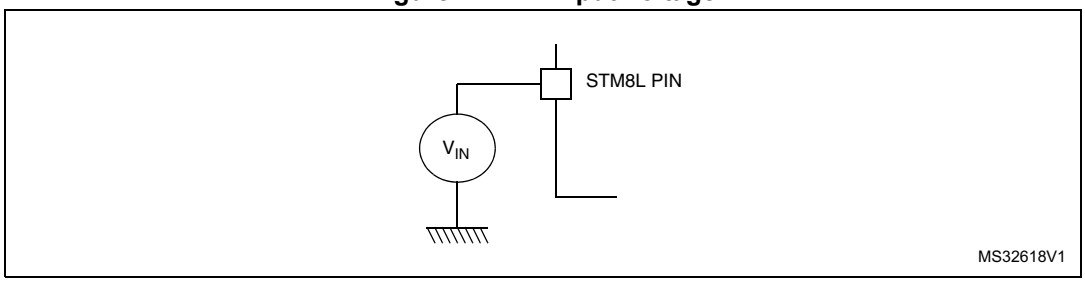
Table 14. Unique ID registers (96 bits)

Address	Content description	Unique ID bits							
		7	6	5	4	3	2	1	0
0x4926	X co-ordinate on the wafer	U_ID[7:0]							
0x4927		U_ID[15:8]							
0x4928	Y co-ordinate on the wafer	U_ID[23:16]							
0x4929		U_ID[31:24]							
0x492A	Wafer number	U_ID[39:32]							
0x492B	Lot number	U_ID[47:40]							
0x492C		U_ID[55:48]							
0x492D		U_ID[63:56]							
0x492E		U_ID[71:64]							
0x492F		U_ID[79:72]							
0x4930		U_ID[87:80]							
0x4931		U_ID[95:88]							

9.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 12*.

Figure 12. Pin input voltage



9.2 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Device mission profile(application conditions)is compliant with JEDEC JESD47 Qualification Standard. Extended mission profiles are available on demand.

Table 15. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD}- V_{SS}	External supply voltage (including V_{DDA})(1)	- 0.3	4.0	V
V_{IN}(2)	Input voltage on true open-drain pins (PC0 and PC1)	V_{SS} - 0.3	V_{DD} + 4.0	
	Input voltage on five-volt tolerant (FT) pins	V_{SS} - 0.3	V_{DD} + 4.0	
	Input voltage on any other pin	V_{SS} - 0.3	4.0	
V_{ESD}	Electrostatic discharge voltage	see *Absolute maximum ratings (electrical sensitivity) on page 122*		

1. All power (V_{DD1}, V_{DD2}, V_{DD3}, V_{DD4}, V_{DDA}) and ground (V_{SS1}, V_{SS2}, V_{SS3}, V_{SS4}, V_{SSA}) pins must always be connected to the external power supply.
2. V_{IN} maximum must always be respected. Refer to *Table 16.* for maximum allowed injected current values.

In the following table, data are based on characterization results, unless otherwise specified.

Table 24. Total current consumption and timing in Active-halt mode at V_{DD} = 1.65 V to 3.6 V

Symbol	Parameter	Conditions[1]			Typ.	Max.	Unit
$I_{DD(AH)}$	Supply current in Active-halt mode	LSI RC (at 38 kHz)	LCD OFF[2]	T_A = -40 °C to 25 °C	0.92	2.25	µA
				T_A = 55 °C	1.32	3.44	
				T_A = 85 °C	1.63	3.87	
				T_A = 105 °C	3	7.94	
				T_A = 125 °C	5.6	13.8	
			LCD ON (static duty/ external V_{LCD}) [3]	T_A = -40 °C to 25 °C	1.56	3.6	
				T_A = 55 °C	1.64	3.8	
				T_A = 85 °C	2.12	5.03	
				T_A = 105 °C	3.34	8.2	
				T_A = 125 °C	5.83	14.4	
			LCD ON (1/4 duty/ external V_{LCD}) [4]	T_A = -40 °C to 25 °C	1.92	4.56	
				T_A = 55 °C	2.1	4.97	
				T_A = 85 °C	2.6	6.14	
				T_A = 105 °C	3.62	8.49	
				T_A = 125 °C	6.1	15.92	
			LCD ON (1/4 duty/ internal V_{LCD}) [5]	T_A = -40 °C to 25 °C	4.2	9.88	
				T_A = 55 °C	4.39	10.32	
				T_A = 85 °C	4.84	11.5	
				T_A = 105 °C	5.98	15	
				T_A = 125 °C	7.21	18.07	

LSE external clock (LSEBYP=1 in CLK_ECKCR)

The LSE is available on STM8L151xx and STM8L152xx devices only.

Subject to general operating conditions for V_{DD} and T_A.

Table 30. LSE external clock characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{LSE_ext}(1)	External clock source frequency		32.768		kHz
V_{LSEH}(2)	OSC32_IN input pin high level voltage	0.7 x V_{DD}		V_{DD}	V
V_{LSEL}(2)	OSC32_IN input pin low level voltage	V_{SS}		0.3 x V_{DD}	
$C_{in(LSE)}$(1)	OSC32_IN input capacitance		0.6		pF
I_{LEAK_LSE}	OSC32_IN input leakage current			±1	µA

1. Guaranteed by design.
2. Data based on characterization results.

HSE crystal/ceramic resonator oscillator

The HSE clock can be supplied with a 1 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph is based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy...).

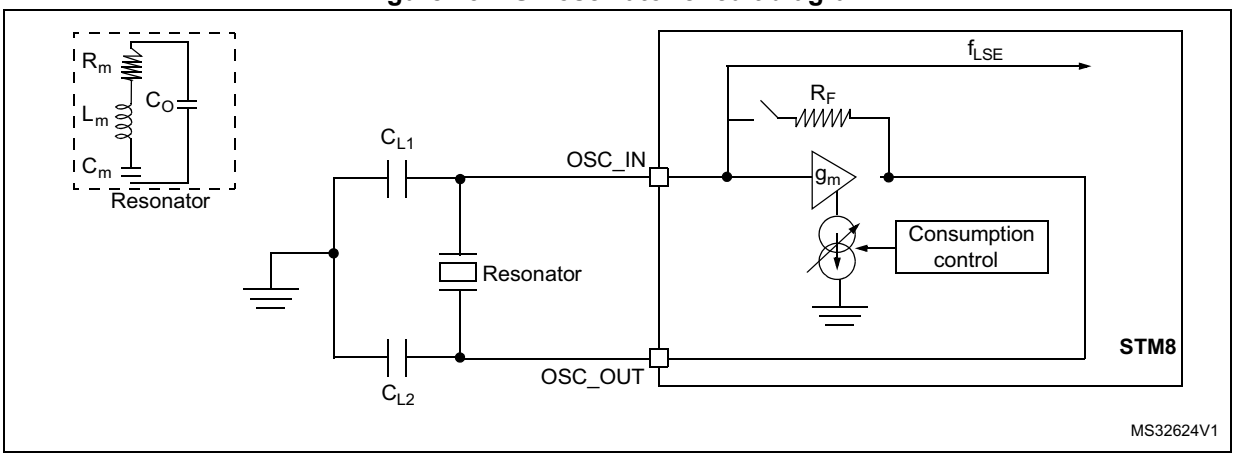
Table 31. HSE oscillator characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{HSE}	High speed external oscillator frequency		1		16	MHz
R_F	Feedback resistor			200		kΩ
C(1)(2)	Recommended load capacitance			20		pF
$I_{DD(HSE)}$	HSE oscillator power consumption	C = 20 pF, f_{OSC} = 16 MHz			2.5 (startup) 0.7 (stabilized)(3)	mA
		C = 10 pF, f_{OSC} =16 MHz			2.5 (startup) 0.46 (stabilized)(3)	
g_m	Oscillator transconductance		3.5(3)			mA/V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabilized		1		ms

1. C=C_{L1}=C_{L2} is approximately equivalent to 2 x crystal C_{LOAD}.
2. The oscillator selection can be optimized in terms of supply current using a high quality resonator with small R_m value. Refer to crystal manufacturer for more details
3. Guaranteed by design.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 16 MHz oscillation. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

4. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Figure 23. LSE oscillator circuit diagram



Internal clock sources

Subject to general operating conditions for V_{DD}, and T_A.

High speed internal RC oscillator (HSI)

In the following table, data are based on characterization results unless otherwise specified.

Table 33. HSI oscillator characteristics

Symbol	Parameter	Conditions(1)	Min.	Typ.	Max.	Unit
f_{HSI}	Frequency	V_{DD} = 3.0 V		16		MHz
ACC_{HSI}	Accuracy of HSI oscillator (factory calibrated)	V_{DD} = 3.0 V, T_A = 25 °C	-1 (2)		1 (2)	%
		V_{DD} = 3.0 V, 0 °C ≤T_A ≤ 55 °C	-1.5		1.5	%
		V_{DD} = 3.0 V, -10 °C ≤T_A ≤ 70 °C	-2		2	%
		V_{DD} = 3.0 V, -10 °C ≤T_A ≤ 85 °C	-2.5		2	%
		V_{DD} = 3.0 V, -10 °C ≤T_A ≤ 125 °C	-4.5		2	%
		1.65 V ≤V_{DD} ≤ 3.6 V, -40 °C ≤T_A ≤ 125 °C	-4.5		3	%
TRIM	HSI user trimming step(3)	Trimming code ≠ multiple of 16		0.4	0.7	%
		Trimming code = multiple of 16			± 1.5	%
$t_{su(HSI)}$	HSI oscillator setup time (wakeup time)			3.7	6 (4)	µs
$I_{DD(HSI)}$	HSI oscillator power consumption			100	140(4)	µA

1. V_{DD} = 3.0 V, T_A = -40 to 125 °C unless otherwise specified.
2. Tested in production.
3. The trimming step differs depending on the trimming code. It is usually negative on the codes which are multiples of 16 (0x00, 0x10, 0x20, 0x30...0xE0). Refer to the AN3101 “STM8L15x internal RC oscillator calibration” application note for more details.

9.3.6 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error, out of spec current injection on adjacent pins or other functional failure (for example reset, oscillator frequency deviation, LCD levels, etc.).

The test results are given in the following table.

Table 37. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on true open-drain pins	-5	+0	mA
	Injected current on all 5 V tolerant (FT) pins	-5	+0	
	Injected current on any other pin	-5	+5	

9.3.7 I/O port pin characteristics

General characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified. All unused pins must be kept at a fixed voltage: using the output mode of the I/O for example or an external pull-up or pull-down resistor.

Table 42. $\overline{\text{NRST}}$ pin characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{IL(NRST)}$	NRST input low level voltage (1)	-	V_{SS}	-	0.8	V
$V_{IH(NRST)}$	NRST input high level voltage (1)	-	1.4	-	V_{DD}	
$V_{OL(NRST)}$	NRST output low level voltage (1)	I_{OL} = 2 mA 2.7 V ≤V_{DD} ≤3.6 V	-	-	0.4	
		I_{OL} = 1.5 mA V_{DD} < 2.7 V	-	-		
V_{HYST}	NRST input hysteresis(3)	-	10%V_{DD}(2)	-	-	mV
$R_{PU(NRST)}$	NRST pull-up equivalent resistor(1)	-	30	45	60	kΩ
$V_{F(NRST)}$	NRST input filtered pulse (3)	-		-	50	ns
$V_{NF(NRST)}$	NRST input not filtered pulse (3)	-	300	-	-	

1. Data based on characterization results.
2. 200 mV min.
3. Data guaranteed by design.

Figure 36. Typical NRST pull-up resistance R_{PU} vs. V_{DD}

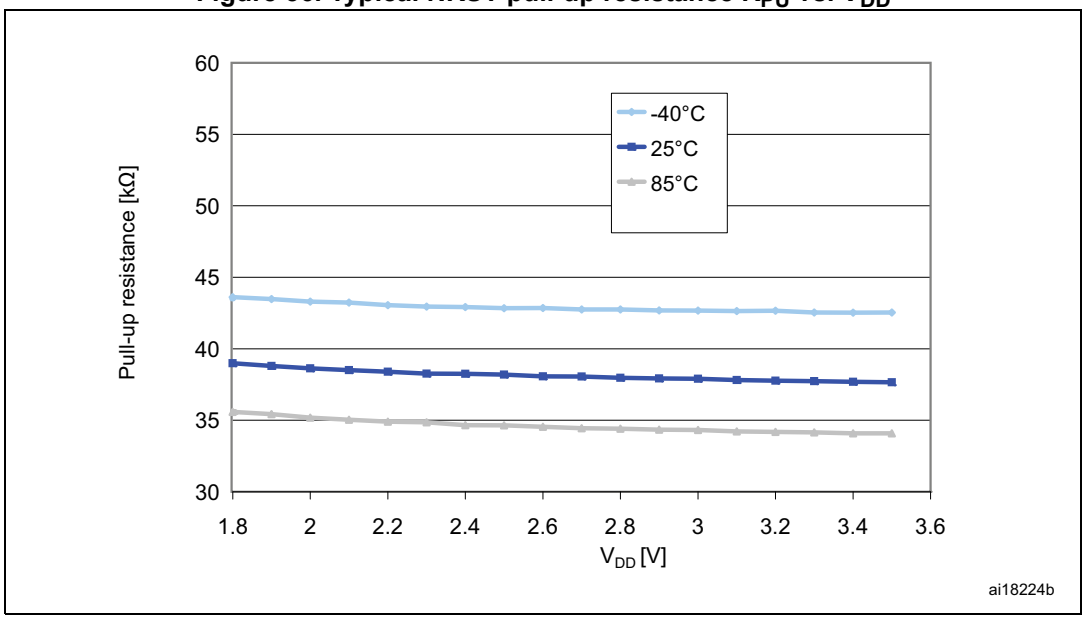


Figure 39. SPI1 timing diagram - slave mode and CPHA=0

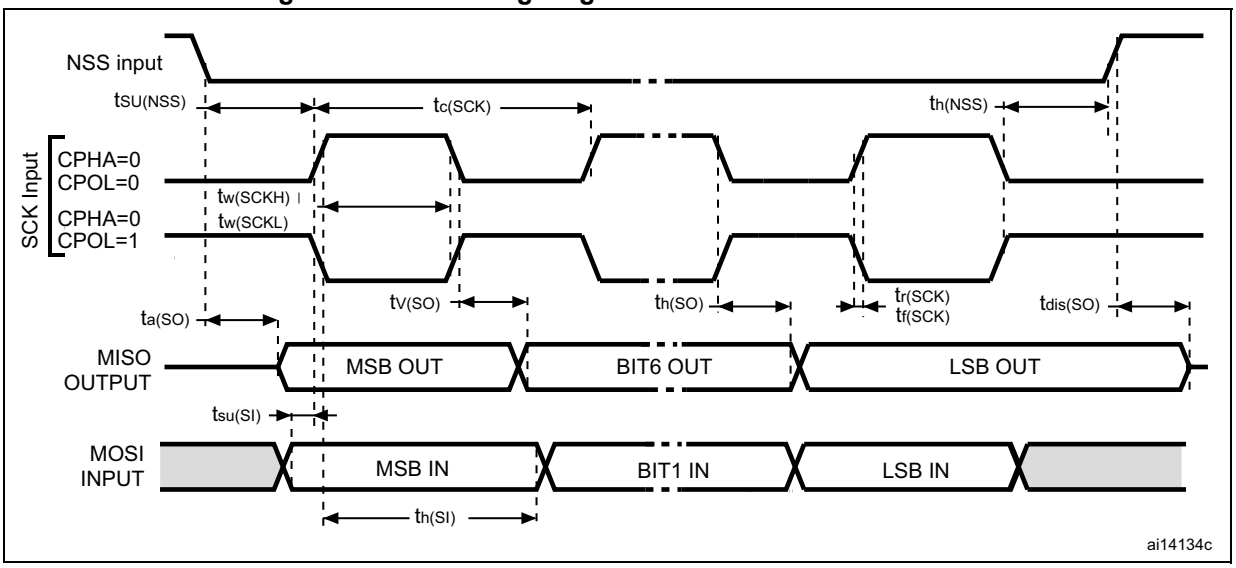
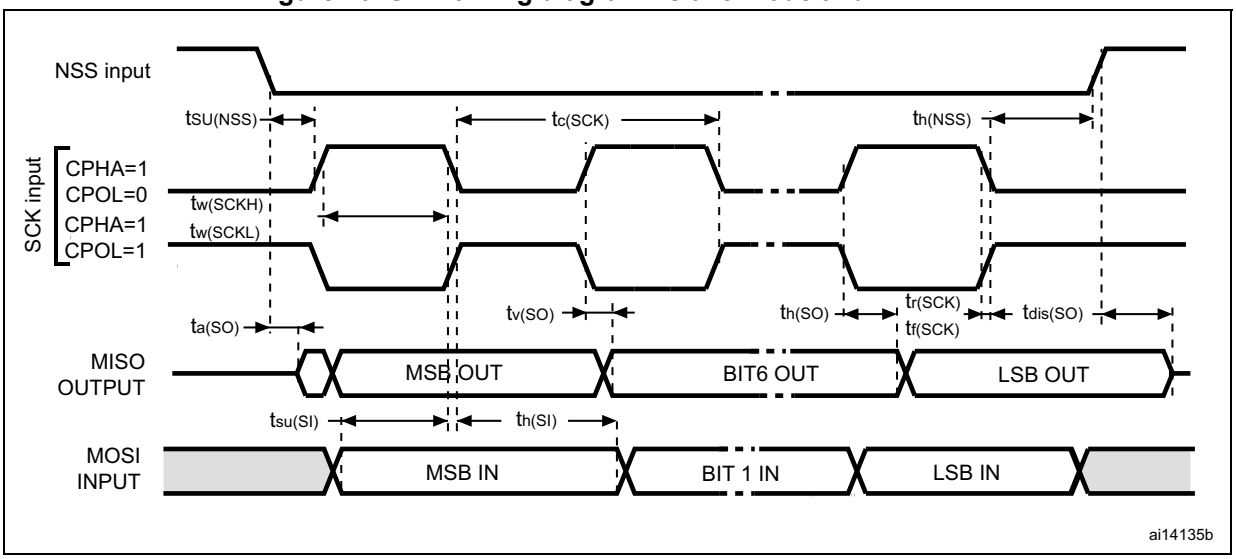


Figure 40. SPI1 timing diagram - slave mode and CPHA=1



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

9.3.9 LCD controller (STM8L152x6/8 only)

In the following table, data are guaranteed by design.

Table 45. LCD characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{LCD}	LCD external voltage	-		3.6	V
V_{LCD0}	LCD internal reference voltage 0	-	2.6	-	
V_{LCD1}	LCD internal reference voltage 1	-	2.7	-	
V_{LCD2}	LCD internal reference voltage 2	-	2.8	-	
V_{LCD3}	LCD internal reference voltage 3	-	3.0	-	
V_{LCD4}	LCD internal reference voltage 4	-	3.1	-	
V_{LCD5}	LCD internal reference voltage 5	-	3.2	-	
V_{LCD6}	LCD internal reference voltage 6	-	3.4	-	
V_{LCD7}	LCD internal reference voltage 7	-	3.5	-	
C_{EXT}	V_{LCD} external capacitance	0.1	1	2	µF
I_{DD}	Supply current(1) at V_{DD} = 1.8 V	-	3	-	µA
	Supply current(1) at V_{DD} = 3 V	-	3	-	
R_{HN}(2)	High value resistive network (low drive)	-	6.6	-	MΩ
R_{LN}(3)	Low value resistive network (high drive)	-	240	-	kΩ
V_{33}	Segment/Common higher level voltage	-		V_{LCDx}	V
V_{34}	Segment/Common 3/4 level voltage	-	$3/4V_{LCDx}$	-	
V_{23}	Segment/Common 2/3 level voltage	-	$2/3V_{LCDx}$	-	
V_{12}	Segment/Common 1/2 level voltage	-	$1/2V_{LCDx}$	-	
V_{13}	Segment/Common 1/3 level voltage	-	$1/3V_{LCDx}$	-	
V_{14}	Segment/Common 1/4 level voltage	-	$1/4V_{LCDx}$	-	
V_0	Segment/Common lowest level voltage	0	-	-	

1. LCD enabled with 3 V internal booster (LCD_CR1 = 0x08), 1/4 duty, 1/3 bias, division ratio= 64, all pixels active, no LCD connected.
2. R_{HN} is the total high value resistive network.
3. R_{LN} is the total low value resistive network.

VLCD external capacitor (STM8L152x6/8 only)

The application can achieve a stabilized LCD reference voltage by connecting an external capacitor C_{EXT} to the V_{LCD} pin. C_{EXT} is specified in *Table 45*.

9.3.11 Temperature sensor

In the following table, data are based on characterization results unless otherwise specified.

Table 47. TS characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{90} (1)	Sensor reference voltage at 90°C ±5 °C,	0.580	0.597	0.614	V
T_L	V_{SENSOR} linearity with temperature	-	±1	±2	°C
Avg_slope(2)	Average slope	1.59	1.62	1.65	mV/°C
$IDD_{(TEMP)}$(2)	Consumption	-	3.4	6	µA
T_{START}(2)(3)	Temperature sensor startup time	-	-	10	µs
T_{S_TEMP}(2)	ADC sampling time when reading the temperature sensor	-	5	10	µs

1. Tested in production at V_{DD} = 3 V ±10 mV. The 8 LSB of the V_{90} ADC conversion result are stored in the TS_Factory_CONV_V90 byte.
2. Guaranteed by design.
3. Defined for ADC output reaching its final value ±1/2LSB.

9.3.12 Comparator characteristics

In the following tables, data are guaranteed by design.

Table 48. Comparator 1 characteristics

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
V_{DDA}	Analog supply voltage		1.65	-	3.6	V
R_{400K}	R_{400K} value	-	-	400	-	kΩ
R_{10K}	R_{10K} value	-	-	10	-	
V_{IN}	Comparator 1 input voltage range	-	0.6	-	V_{DDA}	V
t_{START}	Comparator startup time	-	-	7	10	µs
td	Propagation delay(2)	-	-	3	10	
Voffset	Comparator offset	-	-	±3	±10	mV
$d_{Voffset}/dt$	Comparator offset variation in worst voltage stress conditions	V_{DDA} = 3.6 V V_{IN+} = 0 V V_{IN-} = V_{REFINT} T_A = 25 °C	0	1.5	10	mV/1000 h
I_{COMP1}	Current consumption(3)	-	-	160	260	nA

1. Based on characterization.
2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.
3. Comparator consumption only. Internal reference voltage not included.

9.3.14 12-bit ADC1 characteristics

In the following table, data are guaranteed by design.

Table 53. ADC1 characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DDA}	Analog supply voltage	-	1.8		3.6	V
V_{REF+}	Reference supply voltage	2.4 V ≤V_{DDA}≤ 3.6 V	2.4		V_{DDA}	V
		1.8 V≤V_{DDA}≤ 2.4 V	V_{DDA}			
V_{REF-}	Lower reference voltage	-	V_{SSA}			
I_{VDDA}	Current on the V_{DDA} input pin	-	-	1000	1450	µA
I_{VREF+}	Current on the V_{REF+} input pin	-	-	400	700 (peak)(1)	
		-	-		450 (average)(1)	
V_{AIN}	Conversion voltage range	-	0(2)	-	V_{REF+}	
T_A	Temperature range	-	-40	-	125	°C
R_{AIN}	External resistance on V_{AIN}	on PF0/1/2/3 fast channels	-	-	50(3)	kΩ
		on all other channels	-	-		
C_{ADC}	Internal sample and hold capacitor	on PF0/1/2/3 fast channels	-	16	-	pF
		on all other channels	-		-	
f_{ADC}	ADC sampling clock frequency	2.4 V≤V_{DDA}≤3.6 V without zooming	0.320	-	16	MHz
		1.8 V≤V_{DDA}≤2.4 V with zooming	0.320	-	8	
f_{CONV}	12-bit conversion rate	V_{AIN} on PF0/1/2/3 fast channels	-	-	1(3)(4)	
		V_{AIN} on all other channels	-	-	760(3)(4)	kHz
f_{TRIG}	External trigger frequency	-	-	-	t_{conv}	$1/f_{ADC}$
t_{LAT}	External trigger latency	-	-	-	3.5	$1/f_{SYSCLK}$

In the following three tables, data are guaranteed by characterization result.

Table 54. ADC1 accuracy with V_{DDA} = 3.3 V to 2.5 V

Symbol	Parameter	Conditions	Typ.	Max.	Unit
DNL	Differential non linearity	f_{ADC} = 16 MHz	1	1.6	LSB
		f_{ADC} = 8 MHz	1	1.6	
		f_{ADC} = 4 MHz	1	1.5	
INL	Integral non linearity	f_{ADC} = 16 MHz	1.2	2	
		f_{ADC} = 8 MHz	1.2	1.8	
		f_{ADC} = 4 MHz	1.2	1.7	
TUE	Total unadjusted error	f_{ADC} = 16 MHz	2.2	3.0	
		f_{ADC} = 8 MHz	1.8	2.5	
		f_{ADC} = 4 MHz	1.8	2.3	
Offset	Offset error	f_{ADC} = 16 MHz	1.5	2	
		f_{ADC} = 8 MHz	1	1.5	
		f_{ADC} = 4 MHz	0.7	1.2	
Gain	Gain error	f_{ADC} = 16 MHz	1	1.5	
		f_{ADC} = 8 MHz			
		f_{ADC} = 4 MHz			

Table 55. ADC1 accuracy with V_{DDA} = 2.4 V to 3.6 V

Symbol	Parameter	Typ.	Max.	Unit
DNL	Differential non linearity	1	2	LSB
INL	Integral non linearity	1.7	3	
TUE	Total unadjusted error	2	4	
Offset	Offset error	1	2	
Gain	Gain error	1.5	3	

Table 56. ADC1 accuracy with V_{DDA} = V_{REF}^+ = 1.8 V to 2.4 V

Symbol	Parameter	Typ.	Max.	Unit
DNL	Differential non linearity	1	2	LSB
INL	Integral non linearity	2	3	
TUE	Total unadjusted error	3	5	
Offset	Offset error	2	3	
Gain	Gain error	2	3	

9.3.15 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

Functional EMS (electromagnetic susceptibility)

Based on a simple running application on the product (toggling 2 LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electrostatic discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 61000 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 61000 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Prequalification trials:

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Table 58. EMS data

Symbol	Parameter	Conditions		Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{CPU}= 16 MHz, conforms to IEC 61000		2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{CPU} = 16 MHz, conforms to IEC 61000	Using HSI	4A
			Using HSE	2B

Table 65. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Table 67. WLCSP32 - 32-ball, 1.913 x 3.329 mm, 0.4 mm pitch wafer level chip scale package mechanical data(1)

Symbol	millimeters			inches(2)		
	Min	Typ	Max	Min	Typ	Max
A	0.525	0.555	0.585	0.0207	0.0219	0.0230
A1	-	0.175	-	-	0.0069	-
A2	-	0.380	-	-	0.0150	-
A3(3)	-	0.025	-	-	0.0010	-
b(4)	0.220	0.250	0.280	0.0087	0.0098	0.0110
D	1.878	1.913	1.948	0.0739	0.0753	0.0767
E	3.294	3.329	3.364	0.1297	0.1311	0.1324
e	-	0.400	-	-	0.0157	-
e1	-	1.200	-	-	0.0472	-
e2	-	2.800	-	-	0.1102	-
F	-	0.3565	-	-	0.0140	-
G	-	0.2645	-	-	0.0104	-
aaa	-	-	0.100	-	-	0.0039
bbb	-	-	0.100	-	-	0.0039
ccc	-	-	0.100	-	-	0.0039
ddd	-	-	0.050	-	-	0.0020
eee	-	-	0.050	-	-	0.0020

1. Preliminary data.
2. Values in inches are converted from mm and rounded to 4 decimal digits.
3. Back side coating.
4. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

Figure 61. WLCSP32 - 32-ball, 1.913 x 3.329 mm, 0.4 mm pitch wafer level chip scale package recommended footprint