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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, IR, POR, PWM, WDT
Number of I/O	41
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 25x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-UFQFN Exposed Pad
Supplier Device Package	48-UFQFPN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8l151c8u6tr

2.3 Ultra-low-power continuum

The ultra-low-power STM8L151x6/8, STM8L152x6/8 and STM8L162x8 are fully pin-to-pin, software and feature compatible. Besides the full compatibility within the family, the devices are part of STMicroelectronics microcontrollers ultra-low-power strategy which also includes STM8L101 line, STM8L151/152 lines, and STM8L162 line. The STM8L and STM32L families allow a continuum of performance, peripherals, system architecture, and features.

They are all based on STMicroelectronics 0.13 µm ultra low-leakage process.

Note: 1 The STM8L151xx and STM8L152xx are pin-to-pin compatible with STM8L101xx devices.

2 The STM32L family is pin-to-pin compatible with the general purpose STM32F family. Please refer to STM32Lxxxxx documentation for more information on these devices.

Performance

All families incorporate highly energy-efficient cores with both Harvard architecture and pipelined execution: advanced STM8 core for STM8L families and ARM® Cortex®-M3 core for STM32L family. In addition specific care for the design architecture has been taken to optimize the mA/DMIPS and mA/MHz ratios.

This allows the ultra-low-power performance to range from 5 up to 33.3 DMIPs.

Shared peripherals

STM8L15xx6/8 and STM32Lxxxxx share identical peripherals which ensure a very easy migration from one family to another:

- Analog peripherals: ADC1, DAC1/DAC2, and comparators COMP1/COMP2
- Digital peripherals: RTC and some communication interfaces

Common system strategy

To offer flexibility and optimize performance, the STM8L15xx6/8 and STM32Lxxxxx devices use a common architecture:

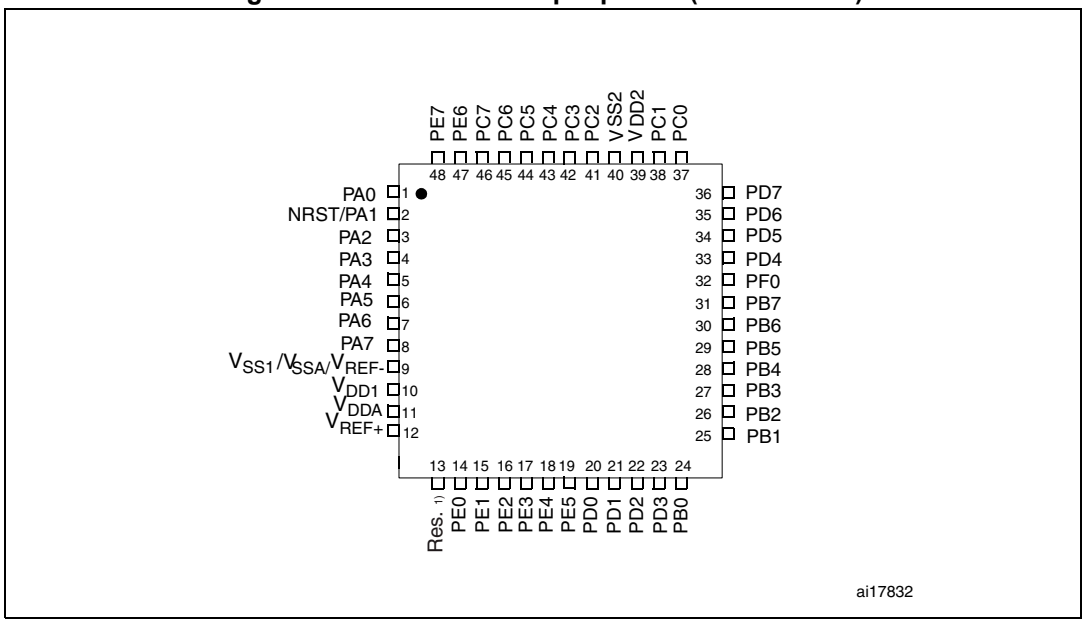
- Same power supply range from 1.65 to 3.6 V. For STM8L101xx and medium-density STM8L15xxx, the power supply must be above 1.8 V at power-on, and go below 1.65 V at power-down.
- Architecture optimized to reach ultra low consumption both in low-power modes and Run mode
- Fast startup strategy from low-power modes
- Flexible system clock
- Ultra safe reset: same reset strategy for both STM8L15xx6/8 and STM32Lxxxxx including power-on reset, power-down reset, brownout reset and programmable voltage detector.

Features

STMicroelectronics ultra-low-power continuum also lies in feature compatibility:

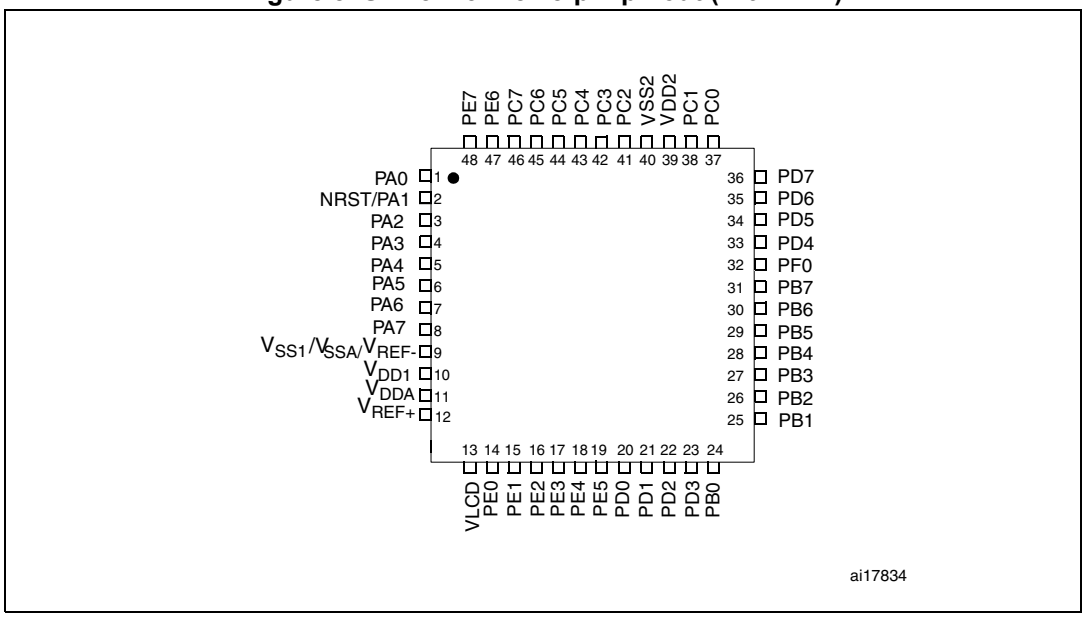
- More than 10 packages with pin counts from 20 to 100 pins and size down to 3 x 3 mm
- Memory density ranging from 4 to 128 Kbyte

Figure 7. STM8L151C8 48-pin pinout (without LCD)



1. Pin 13 is reserved and must be tied to V_{DD}.
2. The above figure shows the package top view.

Figure 8. STM8L152C8 48-pin pinout (with LCD)



1. The above figure shows the package top view.

Table 5. High-density and medium+ density STM8L15x pin description (continued)

Pin number				Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP80	LQFP64	UFQFPN48 and LQFP48	WLCSP32				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
-	-	46	-(4)	PC7/LCD_SEG25(3)/ ADC1_IN3/USART3_CK/ *[COMP2_INM]* / *[COMP1_INP]* / *[LCD_COM5]*	I/O	FT(6)	**X**	X	X	HS	X	X	**Port C7**	LCD segment 25 /ADC1_IN3/ USART3 synchronous clock/ *[Comparator 2 negative input]* / *[Comparator 1 positive input]*/ *[LCD_COM5]*(3)
29	25	20	G3	PD0/TIM3_CH2/ *[ADC1_TRIG]*(2)/ LCD_SEG7(3)/ADC1_IN22/ *[COMP2_INP]*	I/O	FT(6)	**X**	X	X	HS	X	X	**Port D0**	Timer 3 - channel 2 / *[ADC1_Trigger]* / LCD segment 7 / ADC1_IN22 / *[Comparator 2 positive input]*
30	26	21	G2	PD1/TIM3_ETR/ LCD_COM3(3)/ADC1_IN21/ *[COMP1_INP]*// *[COMP2_INP]*	I/O	FT(6)	**X**	X	X	HS	X	X	**Port D1**	Timer 3 - trigger / LCD_COM3 / ADC1_IN21 / *[Comparator 1 positive input]* /*[Comparator 2 positive input]*
31	27	22	E4	PD2/TIM1_CH1 /LCD_SEG8(3)/ADC1_IN20/ *[COMP1_INP]*	I/O	FT(6)	**X**	X	X	HS	X	X	**Port D2**	Timer 1 - channel 1 / LCD segment 8 / ADC1_IN20/ *[Comparator 1 positive input]*
32	28	23	F3	PD3/ TIM1_ETR/ LCD_SEG9(3)/ ADC1_IN19/ *[COMP1_INP]*	I/O	FT(6)	**X**	X	X	HS	X	X	**Port D3**	Timer 1 - trigger / LCD segment 9 / ADC1_IN19/ *[Comparator 1 positive input]*
57	45	-	-	PD4/TIM1_CH2 /LCD_SEG18(3)/ ADC1_IN10/ *[COMP1_INP]*	I/O	FT(6)	**X**	X	X	HS	X	X	**Port D4**	Timer 1 - channel 2 / LCD segment 18 / ADC1_IN10/ *[Comparator 1 positive input]*
-	-	33	C1	PD4/TIM1_CH2 /LCD_SEG18(3)/ ADC1_IN10/SPI2_MISO/ *[COMP1_INP]*	I/O	FT(6)	**X**	X	X	HS	X	X	**Port D4**	Timer 1 - channel 2 / LCD segment 18 / ADC1_IN10/SPI2 master in/slave out/ *[Comparator 1 positive input]*

Table 5. High-density and medium+ density STM8L15x pin description (continued)

Pin number				Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP80	LQFP64	UFQFPN48 and LQFP48	WLCSP32				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
62	50	-	-	PG5/LCD_SEG33/ SPI2_SCK	I/O	FT(6)	**X**	X	X	HS	X	X	**Port G5**	LCD segment 33 / SPI2 clock
63	51	-	-	PG6/LCD_SEG34/ SPI2_MOSI	I/O	FT(6)	**X**	X	X	HS	X	X	**Port G6**	LCD segment 34 / SPI2 master out- slave in
64	52	-	-	PG7/LCD_SEG35/ SPI2_MISO	I/O	FT(6)	**X**	X	X	HS	X	X	**Port G7**	LCD segment 35 / SPI2 master in- slave out
23	19	14	-(4)	PE0/LCD_SEG1(3)/ TIM5_CH2	I/O	FT(6)	**X**	X	X	HS	X	X	**Port E0**	LCD segment 1/ Timer 5 channel 2
24	20	15	-(4)	PE1/TIM1_CH2N /LCD_SEG2(3)	I/O	FT(6)	**X**	X	X	HS	X	X	**Port E1**	Timer 1 - inverted channel 2 / LCD segment 2
25	21	16	-(4)	PE2/TIM1_CH3N /LCD_SEG3(3)/ *[CCO]*(2)	I/O	FT(6)	**X**	X	X	HS	X	X	**Port E2**	Timer 1 - inverted channel 3 / LCD segment 3 / *[Configurable clock output]*
26	-	-	-	PE3/LCD_SEG4(3)	I/O	FT(6)	**X**	X	X	HS	X	X	**Port E3**	LCD segment 4
-	22	17	H2	PE3/LCD_SEG4(3)/ USART2_RX	I/O	FT(6)	**X**	X	X	HS	X	X	**Port E3**	LCD segment 4/ USART2 receive
27	-	-	-	PE4/LCD_SEG5(3)/ DAC_TRIG1	I/O	FT(6)	**X**	X	X	HS	X	X	**Port E4**	LCD segment 5/ DAC 1 trigger
-	23	18	H3	PE4/LCD_SEG5(3)/ DAC_TRIG2/USART2_TX	I/O	FT(6)	**X**	X	X	HS	X	X	**Port E4**	LCD segment 5/ DAC 2 trigger/ USART2 transmit
28	-	-	-	PE5/LCD_SEG6(3)/ ADC1_IN23/*[COMP1_INP]*/ *[COMP2_INP]*	I/O	FT(6)	**X**	X	X	HS	X	X	**Port E5**	LCD segment 6 / ADC1_IN23/ *[Comparator 1 positive input]* /*[Comparator 2 positive input]*
-	24	19	-(4)	PE5/LCD_SEG6(3)/ ADC1_IN23/*[COMP1_INP]*/ *[COMP2_INP]* / USART2_CK	I/O	FT(6)	**X**	X	X	HS	X	X	**Port E5**	LCD segment 6 / ADC1_IN23/ *[Comparator 1 positive input]* / *[Comparator 2 positive input]* /USART2 synchronous clock

Table 5. High-density and medium+ density STM8L15x pin description (continued)

Pin number				Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP80	LQFP64	UFQFPN48 and LQFP48	WLCSP32				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
50	-	-	-	PF1/ADC1_IN25/ DAC_OUT2/ *[USART3_RX]/ [SPI1_MOSI]*	I/O	-	**X**	X	X	HS	X	X	**Port F1**	ADC1_IN25/ DAC channel 2 output/ *[USART3 receive] [SPI1* master out- slave in*]*
-	40	-	-	PF1/ADC1_IN25/ DAC_OUT2/ *[USART3_RX]*	I/O	-	**X**	X	X	HS	X	X	**Port F1**	ADC1_IN25/ DAC channel 2 output/ *[USART3 receive]*
51	-	-	-	PF2/ADC1_IN26/ *[SPI1_SCK]/ [USART3_SCK]*	I/O	-	**X**	X	X	HS	X	X	**Port F2**	ADC1_IN26 *[SPI1 clock] [USART3 clock]*
52	-	-	-	PF3/ADC1_IN27/ *[SPI1_NSS]*	I/O	-	**X**	X	X	HS	X	X	**Port F3**	ADC1_IN27 *[SPI1 master/slave select]*
-	41	-	-	PF4/LCD_SEG36/ *[LCD _COM4]*(10)	I/O	FT(6)	**X**	X	X	HS	X	X	**Port F4**	LCD segment 36/ *[LCD_COM4]*(10)
53	-	-	-	PF4/LCD_SEG40/ *[LCD_COM4]*	I/O	FT(6)	**X**	X	X	HS	X	X	**Port F4**	LCD segment 40/ *[LCD_COM4]*(10)
-	42	-	-	PF5/LCD_SEG37/ *[LCD_COM5]*(10)	I/O	FT(6)	**X**	X	X	HS	X	X	**Port F5**	LCD segment 37/ *[LCD COM5]*(10)
54	-	-	-	PF5/LCD_SEG41/ *[LCD_COM5]*	I/O	FT(6)	**X**	X	X	HS	X	X	**Port F5**	LCD segment 41/ *[LCD COM5]*(10)
-	43	-	-	PF6/LCD_SEG38 /*[LCD_COM6]*(10)	I/O	FT(6)	**X**	X	X	HS	X	X	**Port F6**	LCD segment 38/ *[LCD COM6]*(10)
55	-	-	-	PF6/LCD_SEG42/ *[LCD_COM6]*	I/O	FT(6)	**X**	X	X	HS	X	X	**Port F6**	LCD segment 42/ *[LCD COM6]*(10)
-	44	-	-	PF7/LCD_SEG39/ *[LCD_COM7]*(10)	I/O	FT(6)	**X**	X	X	HS	X	X	**Port F7**	LCD segment 39/ *[LCD COM7]*(10)
56	-	-	-	PF7/LCD_SEG43/ *[LCD_COM7]*	I/O	FT(6)	**X**	X	X	HS	X	X	**Port F7**	LCD segment 43/ *[LCD COM7]*(10)
22	18	13	H4	VLCD(8)	S	-	-	-	-	-	-	-	LCD booster external capacitor	
15	11	10	-	V_{DD1}	S	-	-	-	-	-	-	-	Digital power supply	
14	10	-	-	V_{SS1}	S	-	-	-	-	-	-	-	I/O ground	
16	12	11	-	V_{DDA}	S	-	-	-	-	-	-	-	Analog supply voltage	

Table 5. High-density and medium+ density STM8L15x pin description (continued)

Pin number				Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP80	LQFP64	UFQFPN48 and LQFP48	WLCSP32				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
-	-	-	G4	$V_{DD1}/V_{DDA}/V_{REF+}$	S	-	-	-	-	-	-	-	Digital power supply / Analog power supply / ADC1 positive voltage reference	
17	13	12	-	V_{REF+}/V_{REF+_DAC}	S	-	-	-	-	-	-	-	ADC1 and DAC1/2 positive voltage reference	
18	14	-	-	PG0/LCD SEG28(3) /USART3_RX/ *[TIM2_BKIN]*	I/O	FT(6)	**X**	X	X	HS	X	X	**Port G0**	LCD segment 28/ USART3 receive / *[Timer 2 - break input]*
19	15	-	-	PG1/LCD SEG29(3) /USART3_TX/ *[TIM3_BKIN]*	I/O	FT(6)	**X**	X	X	HS	X	X	**Port G1**	LCD segment 29/ USART3 transmit / *[Timer 3 -break input]*
20	16	-	-	PG2/LCD_SEG30(3)/ USART3_CK	I/O	FT(6)	**X**	X	X	HS	X	X	**Port G2**	LCD segment 30/ USART 3 synchronous clock
21	17	-	-	PG3/LCD SEG 31 (3)/ *[TIM3_ETR]*	I/O	FT(6)	**X**	X	X	HS	X	X	**Port G3**	LCD segment 31/ *[Timer 3 - trigger]*
33	-	-	-	PH4/USART2_RX	I/O	FT(6)	**X**	X	X	HS	X	X	**Port H4**	USART2 receive
34	-	-	-	PH5/USART2_TX	I/O	FT(6)	**X**	X	X	HS	X	X	**Port H5**	USART2 transmit
35	-	-	-	PH6/USART2_CK/ TIM5_CH1	I/O	FT(6)	**X**	X	X	HS	X	X	**Port H6**	USART2 synchronous clock/ Timer 5 - channel 1
36	-	-	-	PH7/TIM5_CH2	I/O	FT(6)	**X**	X	X	HS	X	X	**Port H7**	Timer 5 - channel 2
-	-	9	F4	V_{SS} /V_{SSA} /V_{REF-}	S	-	-	-	-	-	-	-	I/O ground / Analog ground voltage / ADC1 negative voltage reference	
13	9	-	-	V_{SSA} /V_{REF-}	S	-	-	-	-	-	-	-	Analog ground voltage / ADC1 negative voltage reference	
37	29	-	-	V_{DD3}	S	-	-	-	-	-	-	-	IOs supply voltage	
38	30	-	H1	V_{SS3}	S	-	-	-	-	-	-	-	IOs ground voltage	
5	1	1	A4	PA0(9)/*[USART1_CK]*(2)/ SWIM/BEEP/IR_TIM (10)	I/O		X	**X**	X	HS	X	X	**Port A0**	*[USART1 synchronous clock]*(2)/ SWIM input and output / Beep output / Infrared Timer output
68	56	40	-	V_{SS2}	S	-	-	-	-	-	-	-	IOs ground voltage	
67	55	39	-	V_{DD2}	S	-	-	-	-	-	-	-	IOs supply voltage	

Table 5. High-density and medium+ density STM8L15x pin description (continued)

Pin number				Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP80	LQFP64	UFQFPN48 and LQFP48	WLCSP32				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
48	-	-	-	V_{SS4}	S	-	-	-	-	-	-	-	IOs ground voltage	
47	-	-	-	V_{DD4}	S	-	-	-	-	-	-	-	IOs supply voltage	

1. At power-up, the PA1/NRST pin is a reset input pin with pull-up. To be used as a general purpose pin (PA1), it can be configured only as output push-pull, not as output open-drain nor as a general purpose input. Refer to Section *Configuring NRST/PA1 pin as general purpose output* in the STM8L15xxx and STM8L16xxx reference manual (RM0031).
2. [ ] Alternate function remapping option (if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).
3. Available on STM8L152x6/8 devices only.
4. Even if this I/O is not available on the device pin, it is considered as active and must be configured to input pull up or output mode by software to avoid spurious behavior and increased consumption.
5. A pull-up is applied to PB0 and PB4 during the reset phase. These two pins are input floating after reset release.
6. In the 5 V tolerant I/Os, the protection diode to V_{DD} is not implemented.
7. In the open-drain output column, 'T' defines a true open-drain I/O (P-buffer, weak pull-up and protection diode to V_{DD} are not implemented).
8. Available on STM8L152xx devices only. On STM8L151xx devices it is reserved and must be tied to V_{DD}.
9. The PA0 pin is in input pull-up during the reset phase and after reset release.
10. High Sink LED driver capability available on PA0.

Note: Slope control of all GPIO pins can be programmed except true open drain pins and by default is limited to 2 MHz.

System configuration options

As shown in *Table 5: High-density and medium+ density STM8L15x pin description*, some alternate functions can be remapped on different I/O ports by programming one of the two remapping registers described in the "Routing interface (RI) and system configuration controller" section in the STM8L05xxx, STM8L15xxx and STM8L16xxx reference manual (RM0031).

Table 8. I/O port hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 500F	Port D	PD_ODR	Port D data output latch register	0x00
0x00 5010		PD_IDR	Port D input pin value register	0xXX
0x00 5011		PD_DDR	Port D data direction register	0x00
0x00 5012		PD_CR1	Port D control register 1	0x00
0x00 5013		PD_CR2	Port D control register 2	0x00
0x00 5014	Port E	PE_ODR	Port E data output latch register	0x00
0x00 5015		PE_IDR	Port E input pin value register	0xXX
0x00 5016		PE_DDR	Port E data direction register	0x00
0x00 5017		PE_CR1	Port E control register 1	0x00
0x00 5018		PE_CR2	Port E control register 2	0x00
0x00 5019	Port F	PF_ODR	Port F data output latch register	0x00
0x00 501A		PF_IDR	Port F input pin value register	0xXX
0x00 501B		PF_DDR	Port F data direction register	0x00
0x00 501C		PF_CR1	Port F control register 1	0x00
0x00 501D		PF_CR2	Port F control register 2	0x00
0x00 501E	Port G	PG_ODR	Port F data output latch register	0x00
0x00 501F		PG_IDR	Port G input pin value register	0xXX
0x00 5020		PG_DDR	Port G data direction register	0x00
0x00 5021		PG_CR1	Port G control register 1	0x00
0x00 5022		PG_CR2	Port G control register 2	0x00
0x00 5023	Port H	PH_ODR	Port H data output latch register	0x00
0x00 5024		PH_IDR	Port H input pin value register	0xXX
0x00 5025		PH_DDR	Port H data direction register	0x00
0x00 5026		PH_CR1	Port H control register 1	0x00
0x00 5027		PH_CR2	Port H control register 2	0x00
0x00 5028	Port I	PI_ODR	Port I data output latch register	0x00
0x00 5029		PI_IDR	Port I input pin value register	0xXX
0x00 502A		PI_DDR	Port I data direction register	0x00
0x00 502B		PI_CR1	Port I control register 1	0x00
0x00 502C		PI_CR2	Port I control register 2	0x00

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 509D	SYSCFG	SYSCFG_RMPCR3	Remapping register 3	0x00
0x00 509E		SYSCFG_RMPCR1	Remapping register 1	0x00
0x00 509F		SYSCFG_RMPCR2	Remapping register 2	0x00
0x00 50A0	ITC - EXTI	EXTI_CR1	External interrupt control register 1	0x00
0x00 50A1		EXTI_CR2	External interrupt control register 2	0x00
0x00 50A2		EXTI_CR3	External interrupt control register 3	0x00
0x00 50A3		EXTI_SR1	External interrupt status register 1	0x00
0x00 50A4		EXTI_SR2	External interrupt status register 2	0x00
0x00 50A5		EXTI_CONF1	External interrupt port select register 1	0x00
0x00 50A6	WFE	WFE_CR1	WFE control register 1	0x00
0x00 50A7		WFE_CR2	WFE control register 2	0x00
0x00 50A8		WFE_CR3	WFE control register 3	0x00
0x00 50A9		WFE_CR4	WFE control register 4	0x00
0x00 50AA	ITC - EXTI	EXTI_CR4	External interrupt control register 4	0x00
0x00 50AB		EXTI_CONF2	External interrupt port select register 2	0x00
0x00 50A9 to 0x00 50AF	Reserved area (7 byte)			
0x00 50B0	RST	RST_CR	Reset control register	0x00
0x00 50B1		RST_SR	Reset status register	0x01
0x00 50B2	PWR	PWR_CSR1	Power control and status register 1	0x00
0x00 50B3		PWR_CSR2	Power control and status register 2	0x00
0x00 50B4 to 0x00 50BF	Reserved area (12 byte)			
0x00 50C0	CLK	CLK_CKDIVR	Clock master divider register	0x03
0x00 50C1		CLK_CRTCR	Clock RTC register	0x00(1)
0x00 50C2		CLK_ICKCR	Internal clock control register	0x11
0x00 50C3		CLK_PCKENR1	Peripheral clock gating register 1	0x00
0x00 50C4		CLK_PCKENR2	Peripheral clock gating register 2	0x00
0x00 50C5		CLK_CCOR	Configurable clock control register	0x00
0x00 50C6		CLK_ECKCR	External clock control register	0x00
0x00 50C7		CLK_SCSR	System clock status register	0x01
0x00 50C8		CLK_SWR	System clock switch register	0x01
0x00 50C9		CLK_SWCR	Clock switch control register	0xX0

9 Electrical parameters

9.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

9.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A= 25 °C and T_A = T_A max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

9.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

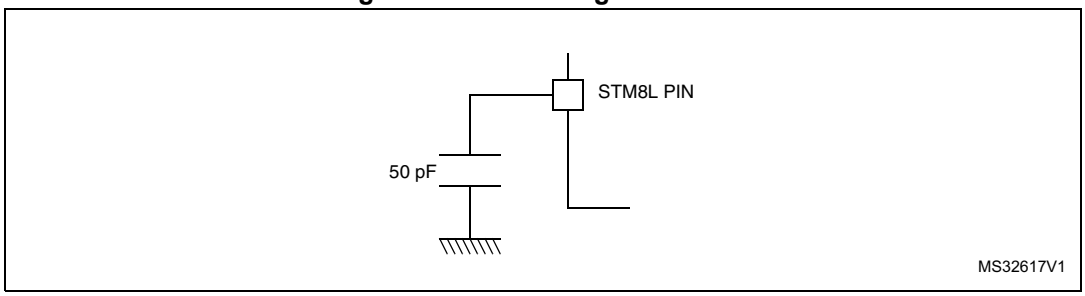
9.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

9.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 11*.

Figure 11. Pin loading conditions



9.3 Operating conditions

Subject to general operating conditions for V_{DD} and T_A.

9.3.1 General operating conditions

Table 18. General operating conditions

Symbol	Parameter	Conditions		Min.	Max.	Unit
f_{SYSCLK}(1)	System clock frequency	1.65 V ≤V_{DD} < 3.6 V		0	16	MHz
V_{DD}	Standard operating voltage	BOR detector disabled (D suffix version)		1.65	3.6	V
		BOR detector enabled		1.8(2)		
V_{DDA}	Analog operating voltage	ADC and DAC not used	Must be at the same potential as V_{DD}	1.65	3.6	V
		ADC or DAC used		1.8	3.6	V
P_D(3)	Power dissipation at T_A= 85 °C for suffix 6 devices	LQFP80		-	526	mW
		LQFP64		-	416	
		UFQFPN48		-	625	
		LQFP48		-	307	
		WLCSP32		-	317	
	Power dissipation at T_A= 125 °C for suffix 3 devices and at T_A= 105 °C for suffix 7 devices	LQFP80		-	131	
		LQFP64		-	104	
		UFQFPN48		-	156	
		LQFP48		-	77	
T_A	Temperature range	1.65 V ≤V_{DD} < 3.6 V (6 suffix version)		-40	85	°C
		1.65 V ≤V_{DD} < 3.6 V (7 suffix version)		-40	105	
		1.65 V ≤V_{DD} < 3.6 V (3 suffix version)		-40	125	
T_J	Junction temperature range	-40 °C ≤T_A < 85 °C (6 suffix version)		-40	105	
		-40 °C ≤ T_A < 105 °C (7 suffix version)		-40	110(4)	
		-40 °C≤ T_A < 125 °C (3 suffix version)		-40	130(4)	

1. $f_{SYSCLK} = f_{CPU}$
2. 1.8 V at power-up, 1.65 V at power-down if BOR is disabled by option byte
3. To calculate $P_{Dmax}(T_A)$, use the formula $P_{Dmax}=(T_{Jmax} - T_A)/\Theta_{JA}$ with T_{Jmax} in this table and Θ_{JA} in “Thermal characteristics” table.
4. T_{Jmax} is given by the test limit. Above this value the product behavior is not guaranteed.

Figure 13. Power supply thresholds

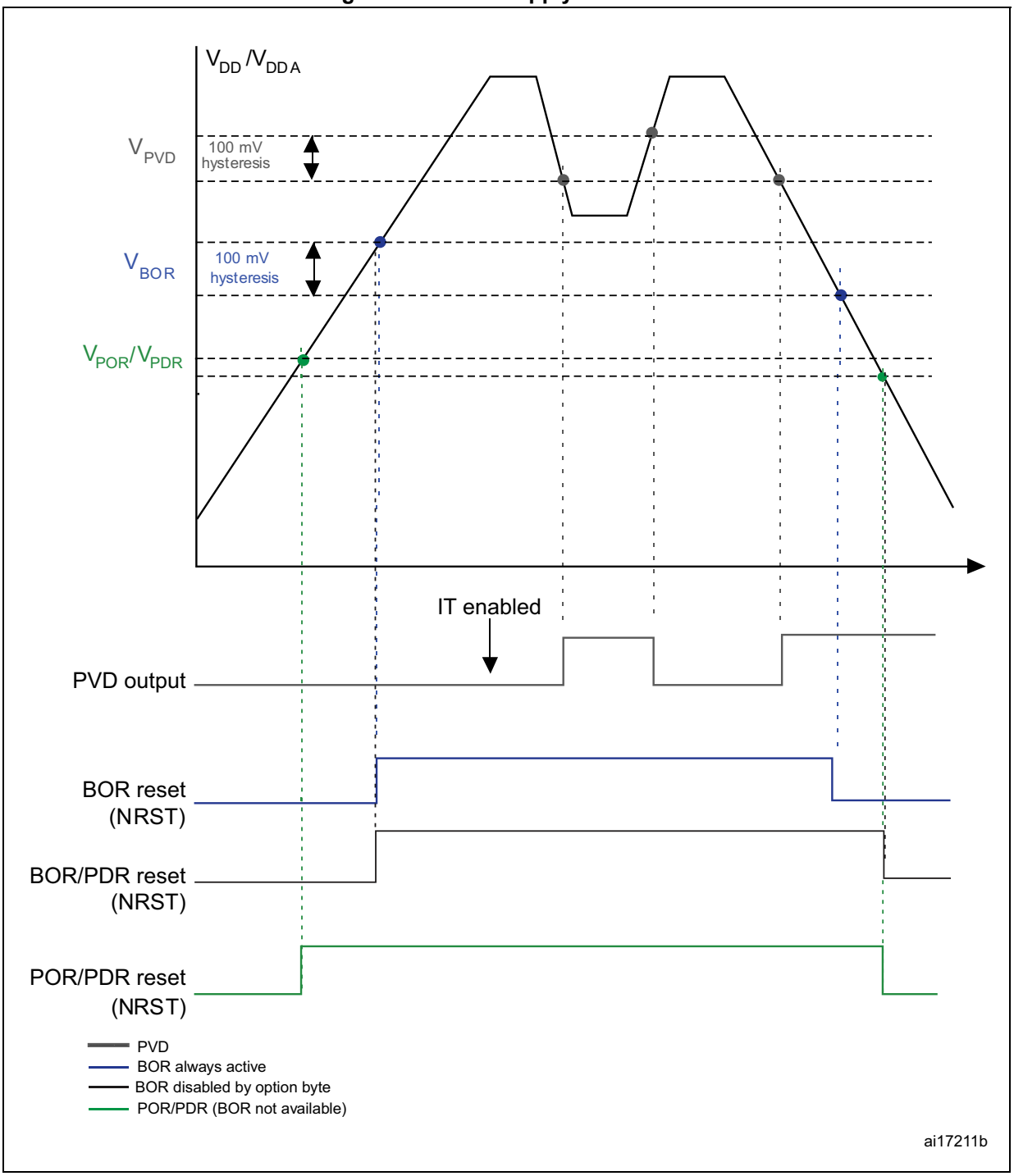


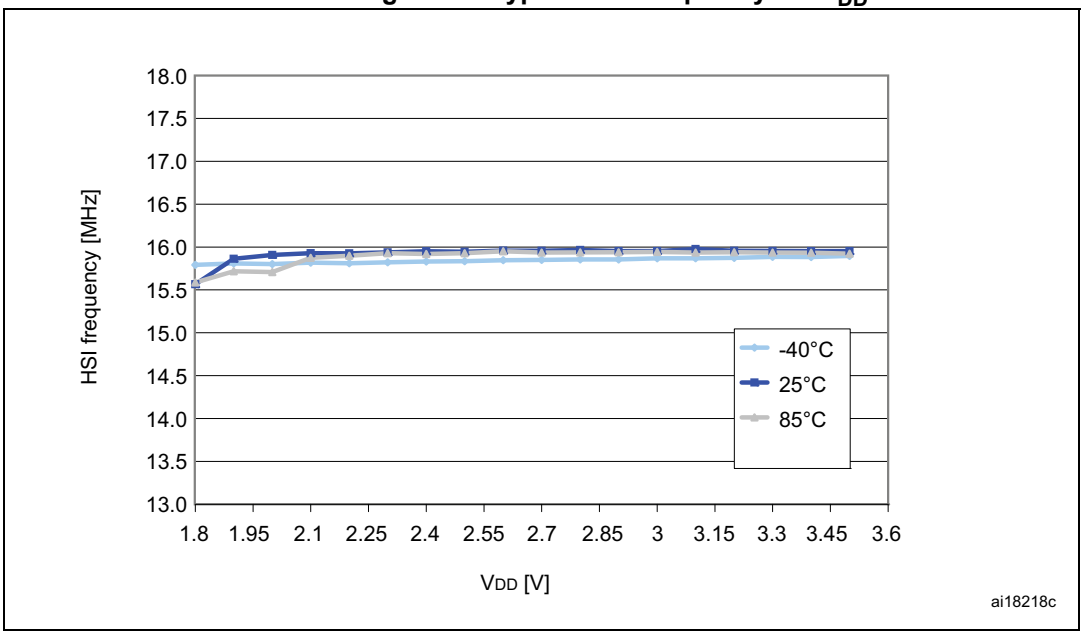
Table 21. Total current consumption in Wait mode (continued)

Symbol	Parameter	Conditions[1]			Typ	Max				Unit
						55°C	85 °C (2)	105 °C (3)	125 °C (4)	
$I_{DD(Wait)}$	Supply current in Wait mode	CPU not clocked, all peripherals OFF, code executed from Flash, V_{DD} from 1.65 V to 3.6 V	HSI	f_{CPU} = 125 kHz	0.27	0.36	0.42	0.46	0.51	mA
				f_{CPU} = 1 MHz	0.29	0.38	0.44	0.48	0.53	
				f_{CPU} = 4 MHz	0.37	0.46	0.52	0.56	0.61	
				f_{CPU} = 8 MHz	0.45	0.55	0.61	0.65	0.7	
				f_{CPU} = 16 MHz	0.69	0.79	0.85	0.89	0.94	
			HSE[7] external clock (f_{CPU}= HSE)	f_{CPU} = 125 kHz	0.23	0.29	0.32	0.4	0.47	
				f_{CPU} = 1 MHz	0.24	0.31	0.34	0.41	0.48	
				f_{CPU} = 4 MHz	0.32	0.39	0.42	0.49	0.56	
				f_{CPU} = 8 MHz	0.42	0.49	0.51	0.59	0.66	
				f_{CPU} = 16 MHz	0.7	0.77	0.79	0.87	0.94	
			LSI	$f_{CPU} = f_{LSI}$	0.037	0.085	0.105	0.123	0.153	
			LSE[8] external clock (32.768 kHz)	$f_{CPU} = f_{LSE}$	0.036	0.082	0.095	0.119	0.133	

1. All peripherals OFF, V_{DD} from 1.65 V to 3.6 V, HSI internal RC osc., $f_{CPU} = f_{SYSCLK}$
2. For devices with suffix 6.
3. For devices with suffix 7.
4. For devices with suffix 3.
5. Flash is configured in I_{DDQ} mode in Wait mode by setting the EPM or WAITM bit in the Flash_CR1 register.
6. Tested in production.
7. Oscillator bypassed (HSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the HSE consumption ($I_{DD\ HSE}$) must be added. Refer to *Table 31*.
8. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD\ HSE}$) must be added. Refer to *Table 32*

4. Guaranteed by design.

Figure 24. Typical HSI frequency vs. V_{DD}



Low speed internal RC oscillator (LSI)

In the following table, data are based on characterization results.

Table 34. LSI oscillator characteristics

Symbol	Parameter	Conditions(1)	Min.	Typ.	Max.	Unit
f_{LSI}	Frequency		26	38	56	kHz
$t_{su(LSI)}$	LSI oscillator wakeup time				200(2)	µs
$D_{(LSI)}$	LSI oscillator frequency drift(3)	0 °C ≤T_A ≤85 °C	-12		11	%

1. V_{DD} = 1.65 V to 3.6 V, T_A = -40 to 125 °C unless otherwise specified.
2. Guaranteed by design.
3. This is a deviation for an individual part, once the initial frequency has been measured.

9.3.8 Communication interfaces

SPI1 - Serial peripheral interface

Unless otherwise specified, the parameters given in *Table 43* are derived from tests performed under ambient temperature, f_{SYSCLK} frequency and V_{DD} supply voltage conditions summarized in *Section 9.3.1*. Refer to I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 43. SPI1 characteristics

Symbol	Parameter	Conditions(1)	Min.	Max.	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI1 clock frequency	Master mode	0	8	MHz
		Slave mode	0	8	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI1 clock rise and fall time	Capacitive load: C = 30 pF	-	30	ns
$t_{su(NSS)}$(2)	NSS setup time	Slave mode	4 x $1/f_{SYSCLK}$	-	
$t_{h(NSS)}$(2)	NSS hold time	Slave mode	80	-	
$t_{w(SCKH)}$(2) $t_{w(SCKL)}$(2)	SCK high and low time	Master mode, f_{MASTER} = 8 MHz, f_{SCK}= 4 MHz	105	145	
$t_{su(MI)}$(2) $t_{su(SI)}$(2)	Data input setup time	Master mode	30	-	
		Slave mode	3	-	
$t_{h(MI)}$(2) $t_{h(SI)}$(2)	Data input hold time	Master mode	15	-	
		Slave mode	0	-	
$t_{a(SO)}$(2)(3)	Data output access time	Slave mode	-	3x $1/f_{SYSCLK}$	
$t_{dis(SO)}$(2)(4)	Data output disable time	Slave mode	30	-	
$t_{v(SO)}$(2)	Data output valid time	Slave mode (after enable edge)	-	60	
$t_{v(MO)}$(2)	Data output valid time	Master mode (after enable edge)	-	20	
$t_{h(SO)}$(2)	Data output hold time	Slave mode (after enable edge)	15	-	
$t_{h(MO)}$(2)		Master mode (after enable edge)	1	-	

1. Parameters are given by selecting 10 MHz I/O output frequency.
2. Values based on design simulation and/or characterization results.
3. Min. time is for the minimum time to drive the output and max. time is for the maximum time to validate the data.
4. Min. time is for the minimum time to invalidate the output and max. time is for the maximum time to put the data in Hi-Z.

9.3.9 LCD controller (STM8L152x6/8 only)

In the following table, data are guaranteed by design.

Table 45. LCD characteristics

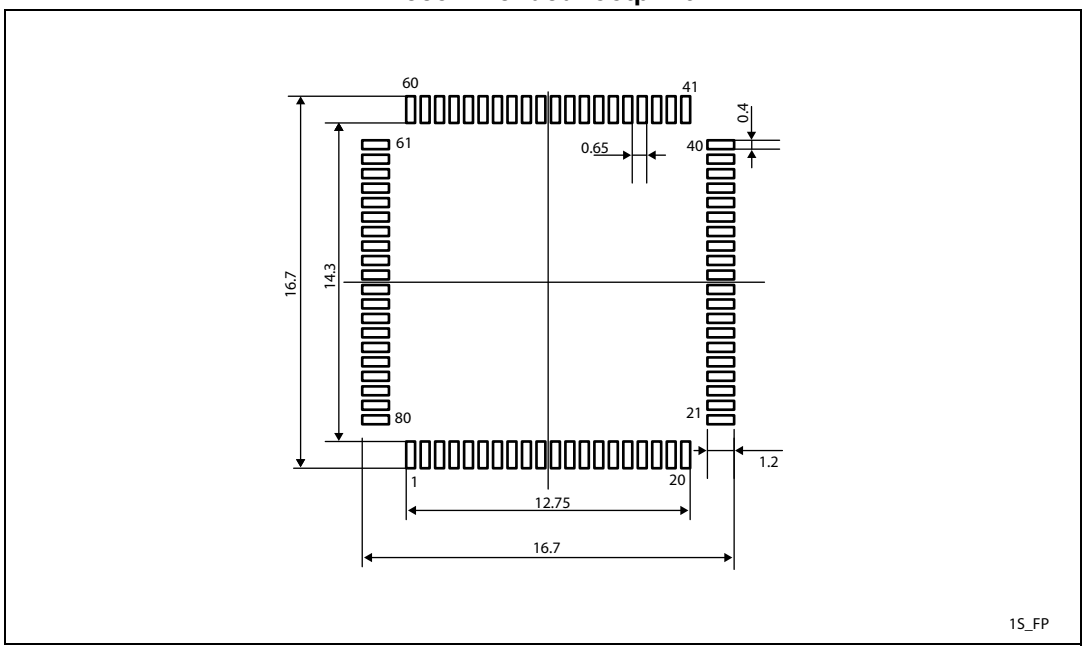
Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{LCD}	LCD external voltage	-		3.6	V
V_{LCD0}	LCD internal reference voltage 0	-	2.6	-	
V_{LCD1}	LCD internal reference voltage 1	-	2.7	-	
V_{LCD2}	LCD internal reference voltage 2	-	2.8	-	
V_{LCD3}	LCD internal reference voltage 3	-	3.0	-	
V_{LCD4}	LCD internal reference voltage 4	-	3.1	-	
V_{LCD5}	LCD internal reference voltage 5	-	3.2	-	
V_{LCD6}	LCD internal reference voltage 6	-	3.4	-	
V_{LCD7}	LCD internal reference voltage 7	-	3.5	-	
C_{EXT}	V_{LCD} external capacitance	0.1	1	2	µF
I_{DD}	Supply current(1) at V_{DD} = 1.8 V	-	3	-	µA
	Supply current(1) at V_{DD} = 3 V	-	3	-	
R_{HN}(2)	High value resistive network (low drive)	-	6.6	-	MΩ
R_{LN}(3)	Low value resistive network (high drive)	-	240	-	kΩ
V_{33}	Segment/Common higher level voltage	-		V_{LCDx}	V
V_{34}	Segment/Common 3/4 level voltage	-	$3/4V_{LCDx}$	-	
V_{23}	Segment/Common 2/3 level voltage	-	$2/3V_{LCDx}$	-	
V_{12}	Segment/Common 1/2 level voltage	-	$1/2V_{LCDx}$	-	
V_{13}	Segment/Common 1/3 level voltage	-	$1/3V_{LCDx}$	-	
V_{14}	Segment/Common 1/4 level voltage	-	$1/4V_{LCDx}$	-	
V_0	Segment/Common lowest level voltage	0	-	-	

1. LCD enabled with 3 V internal booster (LCD_CR1 = 0x08), 1/4 duty, 1/3 bias, division ratio= 64, all pixels active, no LCD connected.
2. R_{HN} is the total high value resistive network.
3. R_{LN} is the total low value resistive network.

VLCD external capacitor (STM8L152x6/8 only)

The application can achieve a stabilized LCD reference voltage by connecting an external capacitor C_{EXT} to the V_{LCD} pin. C_{EXT} is specified in *Table 45*.

Figure 49. LQFP80 - 80-pin, 14 x 14 mm low-profile quad flat package recommended footprint



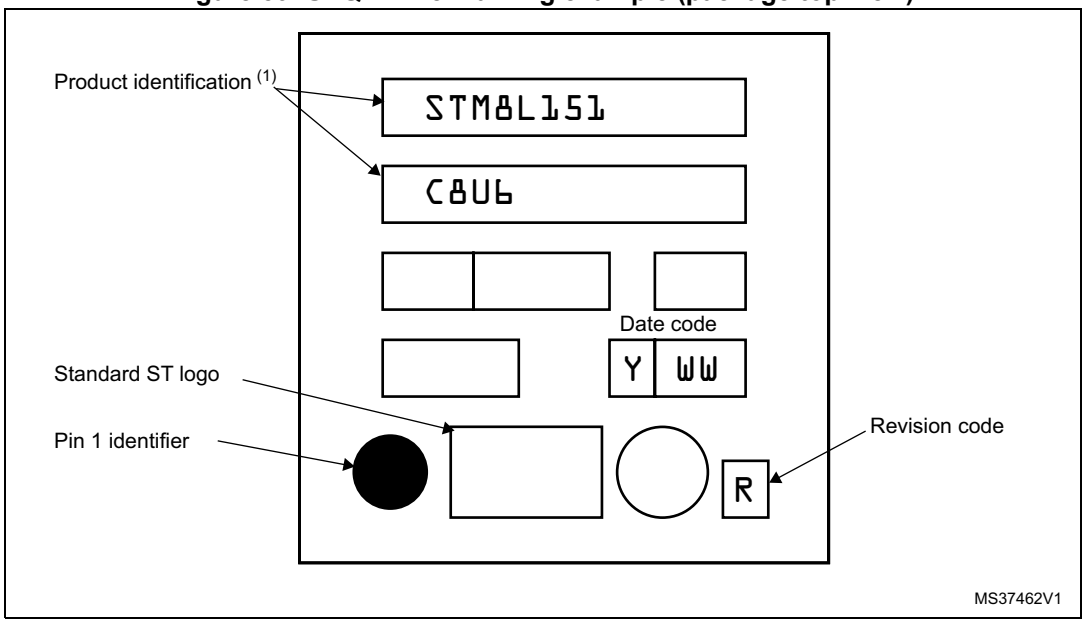
1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 59. UFQFPN48 marking example (package top view)



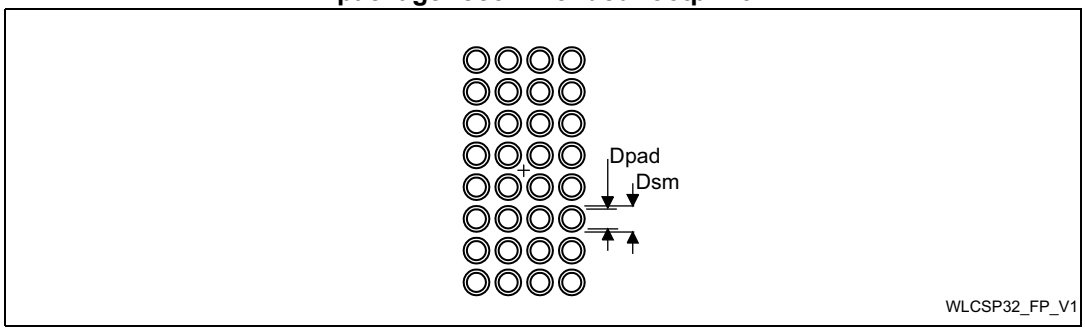
1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 67. WLCSP32 - 32-ball, 1.913 x 3.329 mm, 0.4 mm pitch wafer level chip scale package mechanical data(1)

Symbol	millimeters			inches(2)		
	Min	Typ	Max	Min	Typ	Max
A	0.525	0.555	0.585	0.0207	0.0219	0.0230
A1	-	0.175	-	-	0.0069	-
A2	-	0.380	-	-	0.0150	-
A3(3)	-	0.025	-	-	0.0010	-
b(4)	0.220	0.250	0.280	0.0087	0.0098	0.0110
D	1.878	1.913	1.948	0.0739	0.0753	0.0767
E	3.294	3.329	3.364	0.1297	0.1311	0.1324
e	-	0.400	-	-	0.0157	-
e1	-	1.200	-	-	0.0472	-
e2	-	2.800	-	-	0.1102	-
F	-	0.3565	-	-	0.0140	-
G	-	0.2645	-	-	0.0104	-
aaa	-	-	0.100	-	-	0.0039
bbb	-	-	0.100	-	-	0.0039
ccc	-	-	0.100	-	-	0.0039
ddd	-	-	0.050	-	-	0.0020
eee	-	-	0.050	-	-	0.0020

1. Preliminary data.
2. Values in inches are converted from mm and rounded to 4 decimal digits.
3. Back side coating.
4. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

Figure 61. WLCSP32 - 32-ball, 1.913 x 3.329 mm, 0.4 mm pitch wafer level chip scale package recommended footprint



12 Revision history

Table 70. Document revision history

Date	Revision	Changes
13-Sep-2010	1	Initial release.
20-Dec-2010	2	Updated *Section 9.3.3: Supply current characteristics* Updated *Section 9.3.2: Embedded reset and power control block characteristics*. Updated *Section 9.3.3: Supply current characteristics* Updated *Section 9.3.13: 12-bit DAC characteristics* Updated *Section 9.3.14: 12-bit ADC1 characteristics* Updated *Section 9.3.15: EMC characteristics*
17-Jan-2011	3	Removed references to STM8L150M8 devices.
11-Mar-2011	4	Updated *Table 1: Device summary*. *Table 5: High-density and medium+ density STM8L15x pin description*: updated PB4/43&35, PB4/28, PC1, PI3, and pins 33 to 36 of LQFP80; updated footnotes. TIMx_TRIG changed to TIMx_ETR and “Standard port” changed to “high sink port”. *Table 15: Voltage characteristics*: updated *Table 16: Current characteristics*: updated *Table 35: RAM and hardware registers*: updated VRM data min. retention. Added *Table 9.3.6: I/O current injection characteristics*. *Table 38: I/O static characteristics*: updated *Table 45: LCD characteristics*: updated