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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, IR, POR, PWM, WDT
Number of I/O	68
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 28x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8l151m8t6tr

1 Introduction

This document describes the features, pinout, mechanical data and ordering information for: devices.

- **High-density STM8L15xxx devices:** STM8L151x8 and STM8L152x8 microcontrollers with a Flash memory density of 64 Kbyte.
- **Medium+ density STM8L15xxx devices**: STM8L151R6 and STM8L152R6 microcontrollers with Flash memory density of 32 Kbyte.

For further details on the STMicroelectronics ultra-low-power family please refer to *Section 2.3: Ultra-low-power continuum on page 12*.

For detailed information on device operation and registers, refer to the reference manual (RM0031).

For information on to the Flash program memory and data EEPROM, refer to the programming manual (PM0054).

For information on the debug module and SWIM (single wire interface module), refer to the STM8 SWIM communication protocol and debug module user manual (UM0470).

For information on the STM8 core, refer to the STM8 CPU programming manual (PM0044).

2 Description

The high-density and medium+ density STM8L15xx6/8 ultra-low-power devices feature an enhanced STM8 CPU core providing increased processing power (up to 16 MIPS at 16 MHz) while maintaining the advantages of a CISC architecture with improved code density, a 24-bit linear addressing space and an optimized architecture for low-power operations.

The family includes an integrated debug module with a hardware interface (SWIM) which allows non-intrusive in-application debugging and ultrafast Flash programming.

All high-density and medium+ density STM8L15xx6/8 microcontrollers feature embedded data EEPROM and low-power low-voltage single-supply program Flash memory.

The devices incorporate an extensive range of enhanced I/Os and peripherals, a 12-bit ADC, two DACs, two comparators, a real-time clock, four 16-bit timers, one 8-bit timer, as well as standard communication interfaces such as two SPIs, an I^2C interface, and three USARTs. A 8x40 or 4x44-segment LCD is available on the STM8L152x8 devices. The modular design of the peripheral set allows the same peripherals to be found in different ST microcontroller families including 32-bit families. This makes any transition to a different family very easy, and simplified even more by the use of a common set of development tools.

3.6 LCD (Liquid crystal display)

The LCD is only available on STM8L152x6/8 devices.

The liquid crystal display drives up to 8 common terminals and up to 40 segment terminals to drive up to 320 pixels. It can also be configured to drive up to 4 common and 44 segments (up to 176 pixels).

- Internal step-up converter to guarantee contrast control whatever V_{DD}.
- Static 1/2, 1/3, 1/4, 1/8 duty supported.
- Static 1/2, 1/3, 1/4 bias supported.
- Phase inversion to reduce power consumption and EMI.
- Up to 8 pixels which can programmed to blink.
- The LCD controller can operate in Halt mode.

Note: Unnecessary segments and common pins can be used as general I/O pins.

3.7 Memories

The high-density and medium+ density STM8L15xx6/8 devices have the following main features:

- Up to 4 Kbyte of RAM
- The non-volatile memory is divided into three arrays:
  - Up to 64 Kbyte of medium-density embedded Flash program memory
  - Up to 2 Kbyte of Data EEPROM
  - Option bytes.

The EEPROM embeds the error correction code (ECC) feature. It supports the read-while-write (RWW): it is possible to execute the code from the program matrix while programming/erasing the data matrix.

The option byte protects part of the Flash program memory from write and readout piracy.

3.8 DMA

A 4-channel direct memory access controller (DMA1) offers a memory-to-memory and peripherals-from/to-memory transfer capability. The 4 channels are shared between the following IPs with DMA capability: ADC1, DAC1,DAC2, I2C1, SPI1, SPI2, USART1, USART2, USART3, and the 5 Timers.

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5148	RTC	RTC_CR1	Control register 1	0x00(1)
0x00 5149		RTC_CR2	Control register 2	0x00(1)
0x00 514A		RTC_CR3	Control register 3	0x00(1)
0x00 514B		Reserved area (1 byte)		
0x00 514C		RTC_ISR1	Initialization and status register 1	0x01
0x00 514D		RTC_ISR2	Initialization and Status register 2	0x00
0x00 514E 0x00 514F	Reserved area (2 byte)			
0x00 5150	RTC	RTC_SPRERH	Synchronous prescaler register high	0x00(1)
0x00 5151		RTC_SPRERL	Synchronous prescaler register low	0xFF(1)
0x00 5152		RTC_APRER	Asynchronous prescaler register	0x7F(1)
0x00 5153	Reserved area (1 byte)			
0x00 5154	RTC	RTC_WUTRH	Wakeup timer register high	0xFF(1)
0x00 5155		RTC_WUTRL	Wakeup timer register low	0xFF(1)
0x00 5156	Reserved area (1 byte)			
0x00 5157	RTC	RTC_SSRL	Subsecond register low	0x00
0x00 5158		RTC_SSRH	Subsecond register high	0x00
0x00 5159		RTC_WPR	Write protection register	0x00
0x00 5158		RTC_SSRH	Subsecond register high	0x00
0x00 5159		RTC_WPR	Write protection register	0x00
0x00 515A		RTC_SHIFTRH	Shift register high	0x00
0x00 515B		RTC_SHIFTRL	Shift register low	0x00
0x00 515C		RTC_ALRMAR1	Alarm A register 1	0x00(1)
0x00 515D		RTC_ALRMAR2	Alarm A register 2	0x00(1)
0x00 515E		RTC_ALRMAR3	Alarm A register 3	0x00(1)
0x00 515F		RTC_ALRMAR4	Alarm A register 4	0x00(1)
0x00 5160 to 0x00 5163	Reserved area (4 byte)			
0x00 5164	RTC	RTC_ALRMASSRH	Alarm A subsecond register high	0x00(1)
0x00 5165		RTC_ALRMASSRL	Alarm A subsecond register low	0x00(1)
0x00 5166		RTC_ALRMASSMSKR	Alarm A masking register	0x00(1)
0x00 5167 to 0x00 5169	Reserved area (3 byte)			

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5310	TIM5	TIM5_ARRL	TIM5 Auto-reload register low	0xFF
0x00 5311		TIM5_CCR1H	TIM5 Capture/Compare register 1 high	0x00
0x00 5312		TIM5_CCR1L	TIM5 Capture/Compare register 1 low	0x00
0x00 5313		TIM5_CCR2H	TIM5 Capture/Compare register 2 high	0x00
0x00 5314		TIM5_CCR2L	TIM5 Capture/Compare register 2 low	0x00
0x00 5315		TIM5_BKR	TIM5 break register	0x00
0x00 5316		TIM5_OISR	TIM5 output idle state register	0x00
0x00 5317 to 0x00 533F	Reserved area			
0x00 5340	ADC1	ADC1_CR1	ADC1 configuration register 1	0x00
0x00 5341		ADC1_CR2	ADC1 configuration register 2	0x00
0x00 5342		ADC1_CR3	ADC1 configuration register 3	0x1F
0x00 5343		ADC1_SR	ADC1 status register	0x00
0x00 5344		ADC1_DRH	ADC1 data register high	0x00
0x00 5345		ADC1_DRL	ADC1 data register low	0x00
0x00 5346		ADC1_HTRH	ADC1 high threshold register high	0x0F
0x00 5347		ADC1_HTRL	ADC1 high threshold register low	0xFF
0x00 5348		ADC1_LTRH	ADC1 low threshold register high	0x00
0x00 5349		ADC1_LTRL	ADC1 low threshold register low	0x00
0x00 534A		ADC1_SQR1	ADC1 channel sequence 1 register	0x00
0x00 534B		ADC1_SQR2	ADC1 channel sequence 2 register	0x00
0x00 534C		ADC1_SQR3	ADC1 channel sequence 3 register	0x00
0x00 534D		ADC1_SQR4	ADC1 channel sequence 4 register	0x00
0x00 534E		ADC1_TRIGR1	ADC1 trigger disable 1	0x00
0x00 534F		ADC1_TRIGR2	ADC1 trigger disable 2	0x00
0x00 5350		ADC1_TRIGR3	ADC1 trigger disable 3	0x00
0x00 5351		ADC1_TRIGR4	ADC1 trigger disable 4	0x00
0x00 5352 to 0x00 537F	Reserved area (46 byte)			
0x00 5380	DAC	DAC_CH1CR1	DAC channel 1 control register 1	0x00
0x00 5381		DAC_CH1CR2	DAC channel 1 control register 2	0x00
0x00 5382		DAC_CH2CR1	DAC channel 2 control register 1	0x00
0x00 5383		DAC_CH2CR2	DAC channel 2 control register 2	0x00
0x00 5384		DAC_SWTRIG	DAC software trigger register	0x00
0x00 5385		DAC_SR	DAC status register	0x00

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5400	LCD	LCD_CR1	LCD control register 1	0x00
0x00 5401		LCD_CR2	LCD control register 2	0x00
0x00 5402		LCD_CR3	LCD control register 3	0x00
0x00 5403		LCD_FRQ	LCD frequency selection register	0x00
0x00 5404		LCD_PM0	LCD Port mask register 0	0x00
0x00 5405		LCD_PM1	LCD Port mask register 1	0x00
0x00 5406		LCD_PM2	LCD Port mask register 2	0x00
0x00 5407		LCD_PM3	LCD Port mask register 3	0x00
0x00 5408		LCD_PM4	LCD Port mask register 4	0x00
0x00 5409		LCD_PM5	LCD Port mask register 5	0x00
0x00 540A to 0x00 540B	Reserved area (2 byte)			
0x00 540C	LCD	LCD_RAM0	LCD display memory 0	0x00
0x00 540D		LCD_RAM1	LCD display memory 1	0x00
0x00 540E		LCD_RAM2	LCD display memory 2	0x00
0x00 540F		LCD_RAM3	LCD display memory 3	0x00
0x00 5410		LCD_RAM4	LCD display memory 4	0x00
0x00 5411		LCD_RAM5	LCD display memory 5	0x00
0x00 5412		LCD_RAM6	LCD display memory 6	0x00
0x00 5413		LCD_RAM7	LCD display memory 7	0x00
0x00 5414		LCD_RAM8	LCD display memory 8	0x00
0x00 5415		LCD_RAM9	LCD display memory 9	0x00
0x00 5416		LCD_RAM10	LCD display memory 10	0x00
0x00 5417		LCD_RAM11	LCD display memory 11	0x00
0x00 5418		LCD_RAM12	LCD display memory 12	0x00
0x00 5419		LCD_RAM13	LCD display memory 13	0x00
0x00 541A		LCD_RAM14	LCD display memory 14	0x00
0x00 541B		LCD_RAM15	LCD display memory 15	0x00
0x00 541C		LCD_RAM16	LCD display memory 16	0x00
0x00 541D		LCD_RAM17	LCD display memory 17	0x00
0x00 541E		LCD_RAM18	LCD display memory 18	0x00
0x00 541F		LCD_RAM19	LCD display memory 19	0x00
0x00 5420		LCD_RAM20	LCD display memory 20	0x00
0x00 5421	LCD	LCD_RAM21	LCD display memory 21	0x00

9 Electrical parameters

9.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

9.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A= 25 °C and T_A = T_A max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

9.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

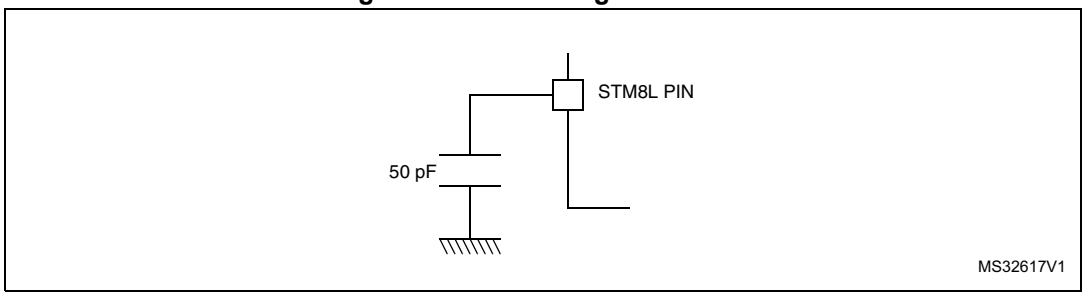
9.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

9.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 11*.

Figure 11. Pin loading conditions



9.3 Operating conditions

Subject to general operating conditions for V_{DD} and T_A.

9.3.1 General operating conditions

Table 18. General operating conditions

Symbol	Parameter	Conditions		Min.	Max.	Unit
f_{SYSCLK}(1)	System clock frequency	1.65 V ≤V_{DD} < 3.6 V		0	16	MHz
V_{DD}	Standard operating voltage	BOR detector disabled (D suffix version)		1.65	3.6	V
		BOR detector enabled		1.8(2)		
V_{DDA}	Analog operating voltage	ADC and DAC not used	Must be at the same potential as V_{DD}	1.65	3.6	V
		ADC or DAC used		1.8	3.6	V
P_D(3)	Power dissipation at T_A= 85 °C for suffix 6 devices	LQFP80		-	526	mW
		LQFP64		-	416	
		UFQFPN48		-	625	
		LQFP48		-	307	
		WLCSP32		-	317	
	Power dissipation at T_A= 125 °C for suffix 3 devices and at T_A= 105 °C for suffix 7 devices	LQFP80		-	131	
		LQFP64		-	104	
		UFQFPN48		-	156	
		LQFP48		-	77	
T_A	Temperature range	1.65 V ≤V_{DD} < 3.6 V (6 suffix version)		-40	85	°C
		1.65 V ≤V_{DD} < 3.6 V (7 suffix version)		-40	105	
		1.65 V ≤V_{DD} < 3.6 V (3 suffix version)		-40	125	
T_J	Junction temperature range	-40 °C ≤T_A < 85 °C (6 suffix version)		-40	105	
		-40 °C ≤ T_A < 105 °C (7 suffix version)		-40	110(4)	
		-40 °C≤ T_A < 125 °C (3 suffix version)		-40	130(4)	

1. $f_{SYSCLK} = f_{CPU}$
2. 1.8 V at power-up, 1.65 V at power-down if BOR is disabled by option byte
3. To calculate $P_{Dmax}(T_A)$, use the formula $P_{Dmax}=(T_{Jmax} - T_A)/\Theta_{JA}$ with T_{Jmax} in this table and Θ_{JA} in “Thermal characteristics” table.
4. T_{Jmax} is given by the test limit. Above this value the product behavior is not guaranteed.

Figure 13. Power supply thresholds

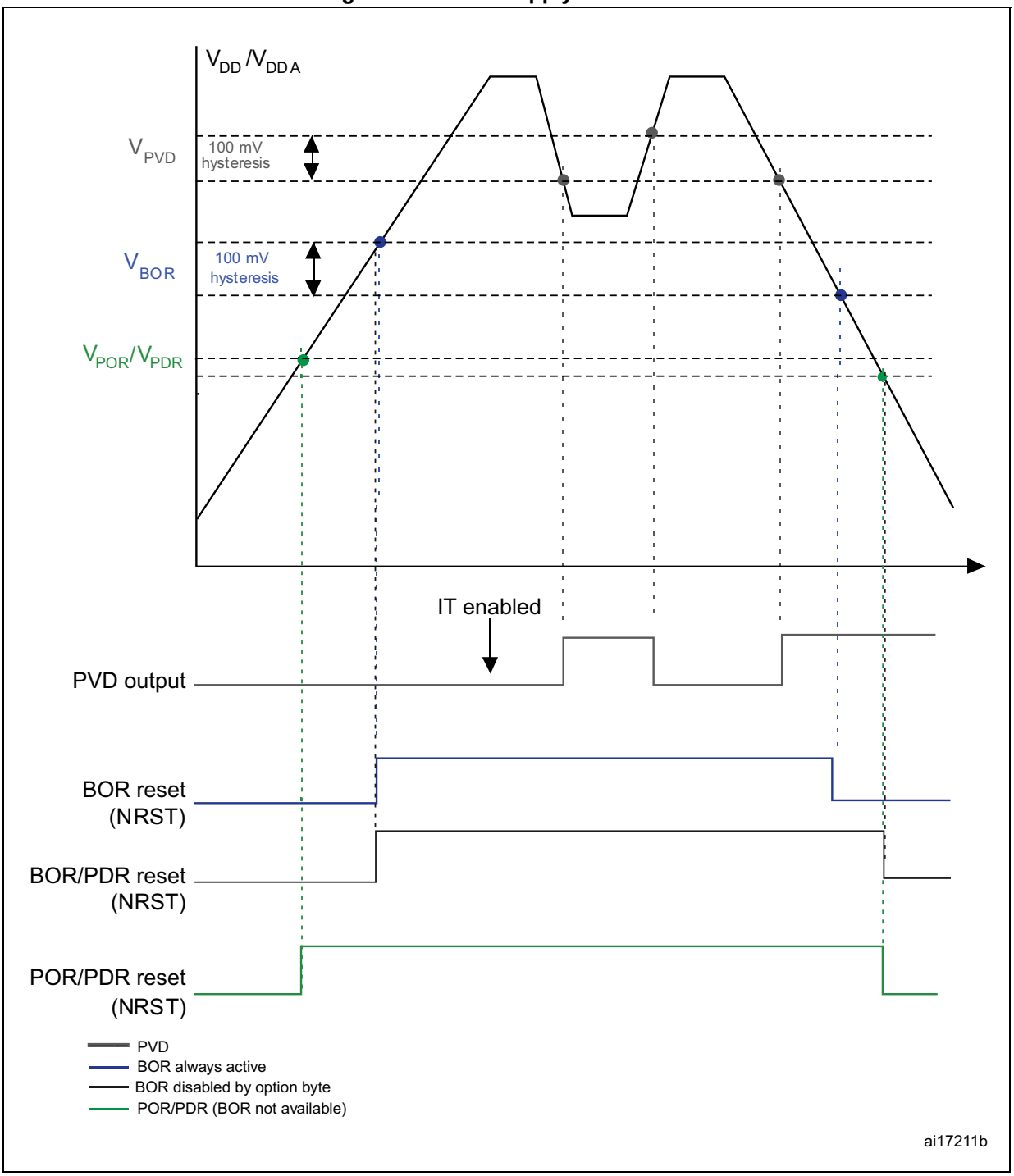
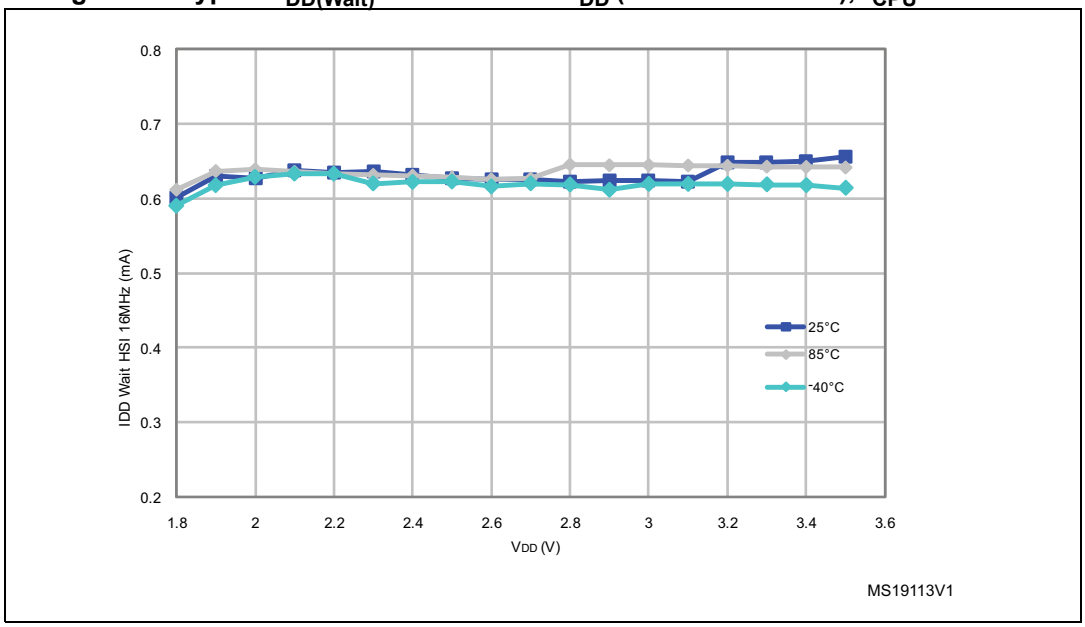
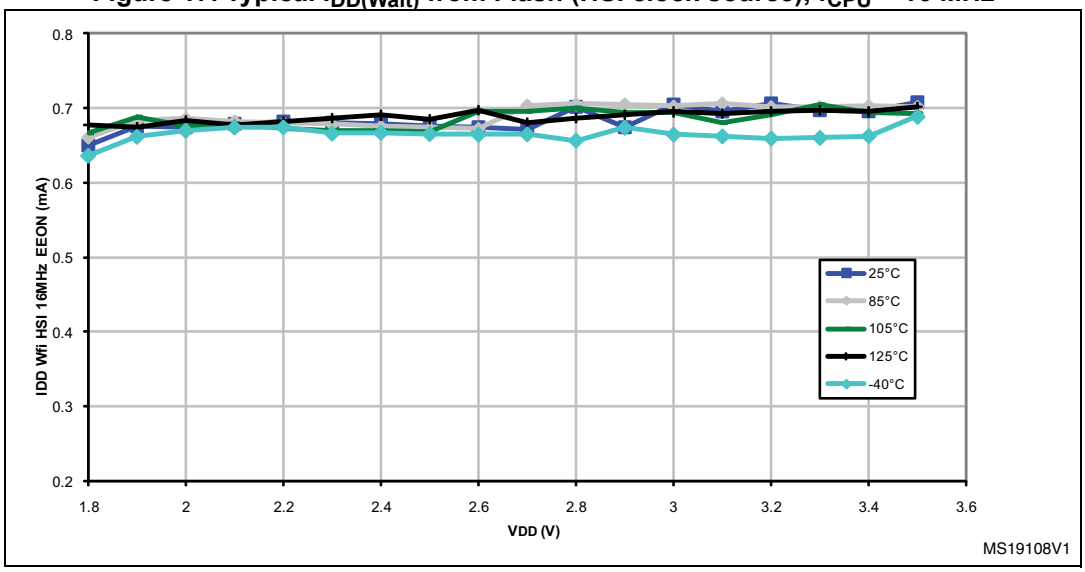


Figure 16. Typical $I_{DD(Wait)}$ from RAM vs. V_{DD} (HSI clock source), f_{CPU} = 16 MHz



1. Typical current consumption measured with code executed from RAM.

Figure 17. Typical $I_{DD(Wait)}$ from Flash (HSI clock source), f_{CPU} = 16 MHz



1. Typical current consumption measured with code executed from Flash.

Table 24. Total current consumption and timing in Active-halt mode at V_{DD} = 1.65 V to 3.6 V (continued)

Symbol	Parameter	Conditions[1]			Typ.	Max.	Unit
$I_{DD(AH)}$	Supply current in Active-halt mode	LSE external clock (32.768 kHz) (6)	LCD OFF[7]	T_A = -40 °C to 25 °C	0.54	1.35	µA
				T_A = 55 °C	0.61	1.44	
				T_A = 85 °C	0.91	2.27	
				T_A = 105 °C	2.24	5.42	
				T_A = 125 °C	5.03	12	
			LCD ON (static duty/ external V_{LCD}) [3]	T_A = -40 °C to 25 °C	0.91	2.13	
				T_A = 55 °C	1.05	2.55	
				T_A = 85 °C	1.42	3.65	
				T_A = 105 °C	2.63	6.35	
				T_A = 125 °C	5.24	13.15	
			LCD ON (1/4 duty/ external V_{LCD}) [4]	T_A = -40 °C to 25 °C	1.6	2.84	
				T_A = 55 °C	1.76	4.37	
				T_A = 85 °C	2.14	5.23	
				T_A = 105 °C	3.37	8.5	
				T_A = 125 °C	5.92	15.19	
			LCD ON (1/4 duty/ internal V_{LCD}) [5]	T_A = -40 °C to 25 °C	3.89	9.15	
				T_A = 55 °C	3.89	9.15	
				T_A = 85 °C	4.25	10.49	
				T_A = 105 °C	5.42	16.31	
				T_A = 125 °C	6.58	16.6	
$I_{DD(WUFAH)}$	Supply current during wakeup time from Active-halt mode (using HSI)	-	-	-	2.4	-	mA
$t_{WU\_HSI(AH)}$[8][9]	Wakeup time from Active-halt mode to Run mode (using HSI)	-	-	-	4.7	7	µs
$t_{WU\_LSI(AH)}$[8][9]	Wakeup time from Active-halt mode to Run mode (using LSI)	-	-	-	150	-	µs

1. No floating I/O, unless otherwise specified.
2. RTC enabled. Clock source = LSI
3. RTC enabled, LCD enabled with external V_{LCD} = 3 V, static duty, division ratio = 256, all pixels active, no LCD connected.
4. RTC enabled, LCD enabled with external V_{LCD}, 1/4 duty, 1/3 bias, division ratio = 64, all pixels active, no LCD connected.
5. LCD enabled with internal LCD booster V_{LCD} = 3 V, 1/4 duty, 1/3 bias, division ratio = 64, all pixels active, no LCD connected.
6. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD\ LSE}$) must be added. Refer to *Table 32*

Figure 28. Typical pull-up resistance R_{PU} vs. V_{DD} with $V_{IN}=V_{SS}$

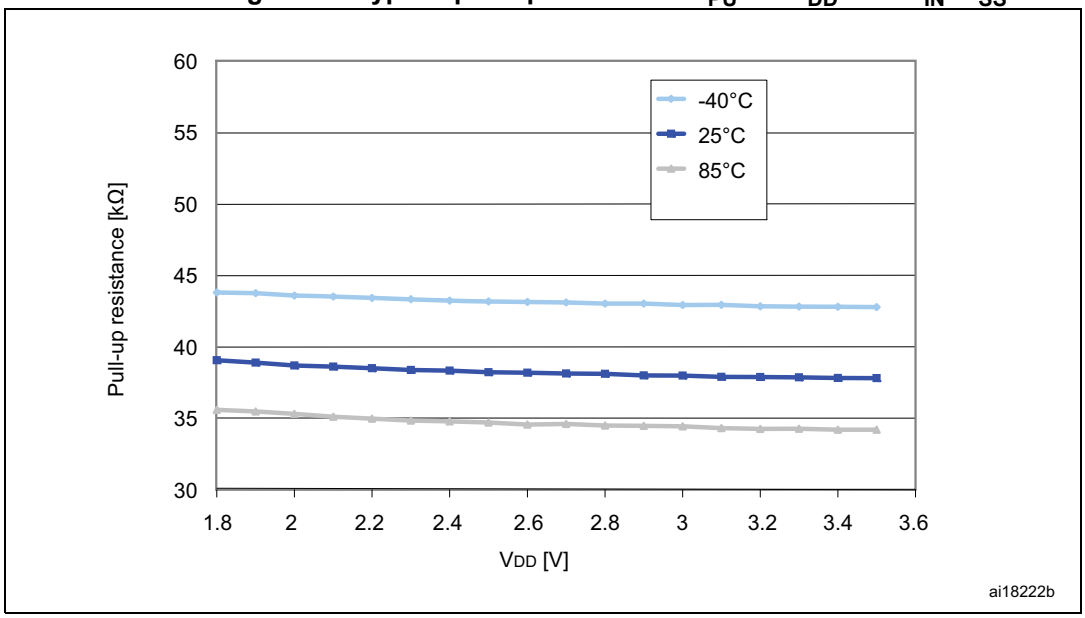
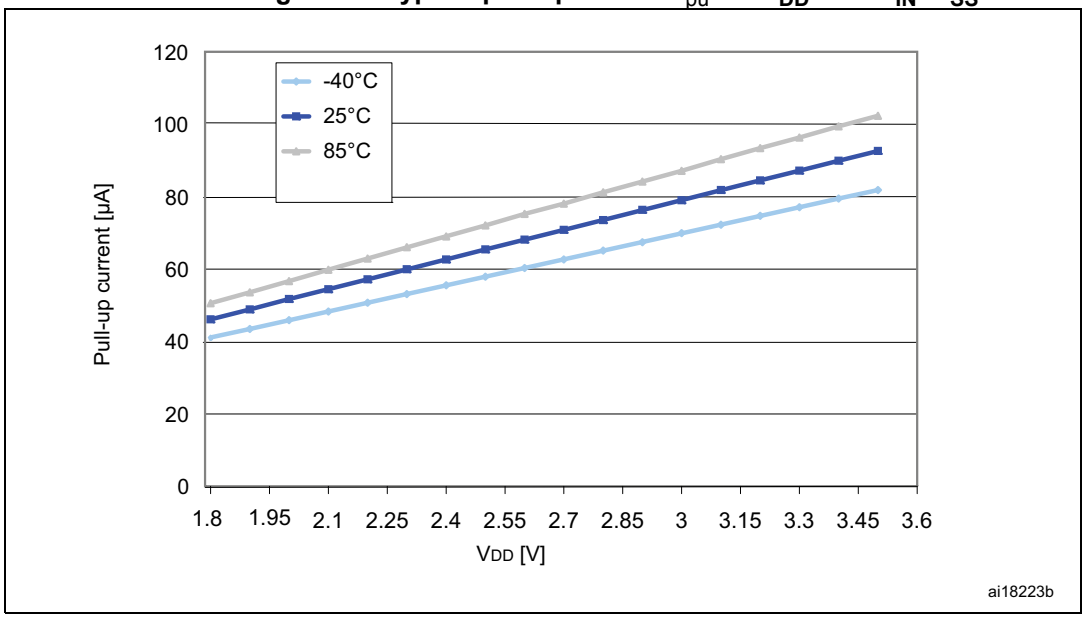


Figure 29. Typical pull-up current I_{pu} vs. V_{DD} with $V_{IN}=V_{SS}$



Output driving current

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

I²C - Inter IC control interface

Subject to general operating conditions for V_{DD}, f_{SYSCLK}, and T_A unless otherwise specified.

The STM8L I²C interface (I2C1) meets the requirements of the Standard I²C communication protocol described in the following table with the restriction mentioned below:

Refer to I/O port characteristics for more details on the input/output alternate function characteristics (SDA and SCL).

Table 44. I2C characteristics

Symbol	Parameter	Standard mode I²C		Fast mode I²C(1)		Unit
		Min.(2)	Max. (2)	Min. (2)	Max. (2)	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	0	-	0	900	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	-	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	START condition hold time	4.0	-	0.6	-	µs
$t_{su(STA)}$	Repeated START condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	STOP condition setup time	4.0	-	0.6	-	µs
$t_{w(STO:STA)}$	STOP to START condition time (bus free)	4.7	-	1.3	-	µs
C_b	Capacitive load for each bus line	-	400	-	400	pF

1. f_{SYSCLK} must be at least equal to 8 MHz to achieve max fast I²C speed (400 kHz).
2. Data based on standard I²C protocol requirement, not tested in production.

Note: For speeds around 200 kHz, the achieved speed can have a ±5% tolerance.
For other speed ranges, the achieved speed can have a ±2% tolerance.
The above variations depend on the accuracy of the external components used.

9.3.10 Embedded reference voltage

In the following table, data are based on characterization results unless otherwise specified.

Table 46. Reference voltage characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{REFINT}	Internal reference voltage consumption	-	-	1.4		µA
$T_{S\_VREFINT}$(1)(2)	ADC sampling time when reading the internal reference voltage	-	-	5	10	µs
I_{BUF}(1)	Internal reference voltage buffer consumption (used for ADC)	-	-	13.5	25	µA
$V_{REFINT\ out}$	Reference voltage output	-	1.202 (3)	1.224	1.242 (3)	V
I_{LPBUF}(1)	Internal reference voltage low-power buffer consumption (used for comparators or output)	-	-	730	1200	nA
I_{REFOUT}(1)(4)	Buffer output current	-	-		1	µA
C_{REFOUT}	Reference voltage output load	-	-		50	pF
$t_{VREFINT}$(1)	Internal reference voltage startup time	-	-	2	3	ms
t_{BUFEN}(1)(2)	Internal reference voltage buffer startup time once enabled	-	-		10	µs
$ACC_{VREFINT}$(5)	Accuracy of V_{REFINT} stored in the VREFINT_Factory_CONV byte	-	-		± 5	mV
$STAB_{VREFINT}$	Stability of V_{REFINT} over temperature	-40 °C ≤T_A ≤ 125 °C	-	20	50	ppm/°C
	Stability of V_{REFINT} over temperature	0 °C ≤T_A ≤ 50 °C	-	-	20	ppm/°C
$STAB_{VREFINT}$	Stability of V_{REFINT} after 1000 hours	-	-	-	1000	ppm

1. Guaranteed by design.
2. Defined when ADC output reaches its final value ±1/2LSB
3. Tested in production at V_{DD} = 3 V ±10 mV.
4. To guarantee less than 1% V_{REFOUT} deviation
5. Measured at V_{DD} = 3 V ±10 mV. This value takes into account V_{DD} accuracy and ADC conversion accuracy.

Table 53. ADC1 characteristics (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_S	Sampling time	V_{AIN} PF0/1/2/3 fast channels V_{DDA} < 2.4 V	0.43(3)(4)	-	-	µs
		V_{AIN} PF0/1/2/3 fast channels 2.4 V ≤V_{DDA}≤ 3.6 V	0.22(3)(4)	-	-	
		V_{AIN} on slow channels V_{DDA} < 2.4 V	0.86(3)(4)	-	-	
		V_{AIN} on slow channels 2.4 V ≤V_{DDA}≤ 3.6 V	0.41(3)(4)	-	-	
t_{conv}	12-bit conversion time	-	12 + t_S			$1/f_{ADC}$
		16 MHz	1(3)			µs
t_{WKUP}	Wakeup time from OFF state	-	-	-	3	µs
t_{IDLE}(5)	Time before a new conversion	-	-	-	∞	s
$t_{VREFINT}$	Internal reference voltage startup time	-	-	-	refer to *Table 46*	ms

1. The current consumption through V_{REF} is composed of two parameters:
   - one constant (max 300 µA)
   - one variable (max 400 µA), only during sampling time + 2 first conversion pulses.
   So, peak consumption is 300+400 = 700 µA and average consumption is 300 + [(4 sampling + 2) /16] x 400 = 450 µA at 1Msps
2. V_{REF-} must be tied to ground.
3. Minimum sampling and conversion time is reached for maximum R_{AIN}= 0.5 kΩ.
4. Value obtained for continuous conversion on fast channel.
5. The time between 2 conversions, or between ADC ON and the first conversion must be lower than t_{IDLE}.

Figure 45. Maximum dynamic current consumption on V_{REF+} supply pin during ADC conversion

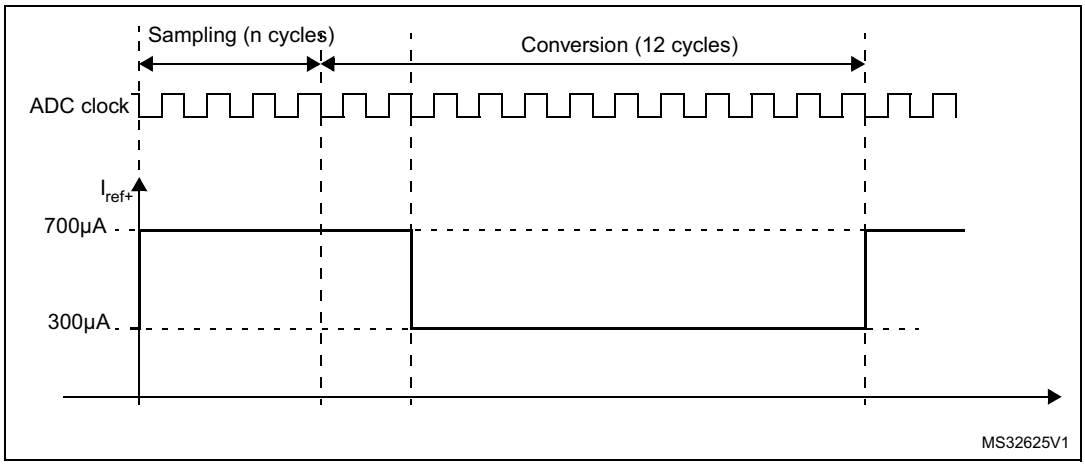


Table 57. R_{AIN} max for f_{ADC} = 16 MHz(1)

Ts (cycles)	Ts (µs)	R_{AIN} max (kohm)			
		Slow channels		Fast channels	
		2.4 V < V_{DDA} < 3.6 V	1.8 V < V_{DDA} < 2.4 V	2.4 V < V_{DDA} < 3.3 V	1.8 V < V_{DDA} < 2.4 V
4	0.25	Not allowed	Not allowed	0.7	Not allowed
9	0.5625	0.8	Not allowed	2.0	1.0
16	1	2.0	0.8	4.0	3.0
24	1.5	3.0	1.8	6.0	4.5
48	3	6.8	4.0	15.0	10.0
96	6	15.0	10.0	30.0	20.0
192	12	32.0	25.0	50.0	40.0
384	24	50.0	50.0	50.0	50.0

1. Guaranteed by design.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 46* or *Figure 47*, depending on whether V_{REF+} is connected to V_{DDA} or not. Good quality ceramic 10 nF capacitors should be used. They should be placed as close as possible to the chip.

9.3.15 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

Functional EMS (electromagnetic susceptibility)

Based on a simple running application on the product (toggling 2 LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electrostatic discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 61000 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 61000 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Prequalification trials:

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Table 58. EMS data

Symbol	Parameter	Conditions		Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{CPU}= 16 MHz, conforms to IEC 61000		2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{CPU} = 16 MHz, conforms to IEC 61000	Using HSI	4A
			Using HSE	2B

Static latch-up

- **LU**: 3 complementary static tests are required on 10 parts to assess the latch-up performance. A supply overvoltage (applied to each power supply pin) and a current injection (applied to each input, output and configurable I/O pin) are performed on each sample. This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.

Table 61. Electrical sensitivities

Symbol	Parameter	Class
LU	Static latch-up class	II

9.4 Thermal characteristics

The maximum chip junction temperature (T_{Jmax}) must never exceed the values given in *Table 18: General operating conditions on page 70*.

The maximum chip-junction temperature, T_{Jmax}, in degree Celsius, may be calculated using the following equation:

$$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$$

Where:

- T_{Amax} is the maximum ambient temperature in °C
- Θ_{JA} is the package junction-to-ambient thermal resistance in °C/W
- P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$)
- P_{INTmax} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.
- $P_{I/Omax}$ represents the maximum power dissipation on output pins
  Where:
  $P_{I/Omax} = \Sigma (V_{OL}*I_{OL}) + \Sigma((V_{DD}-V_{OH})*I_{OH})$,
  taking into account the actual V_{OL}/I_{OL} and V_{OH}/I_{OH} of the I/Os at low and high level in the application.

Table 62. Thermal characteristics(1)

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient LQFP 48 - 7 x 7 mm	65	°C/W
	Thermal resistance junction-ambient UFQFPN 48 - 7 x 7mm	32	
	Thermal resistance junction-ambient WLCSP32	63	
	Thermal resistance junction-ambient LQFP 64 - 10 x 10 mm	48	
	Thermal resistance junction-ambient LQFP 80 - 14 x 14 mm	38	

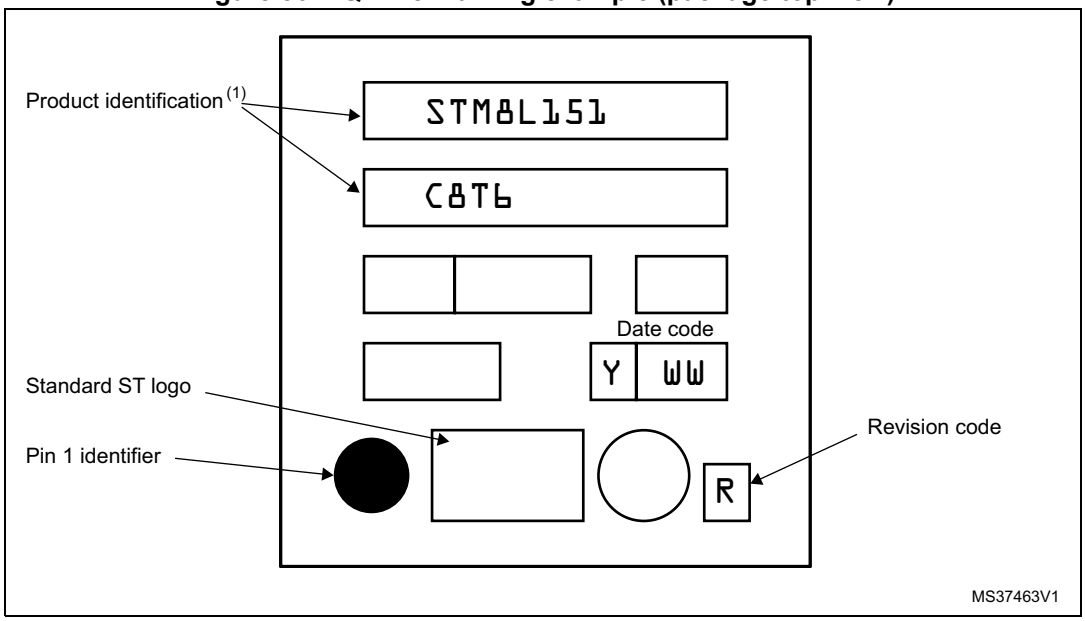
1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 56. LQFP48 marking example (package top view)



1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 68. WLCSP32 recommended PCB design rules

Dimension	Recommended values
Pitch	0.4 mm
Dpad	0.225 mm
Dsm	0.290 mm typical (depending on the solder mask registration tolerance)
Stencil opening	0.250 mm
Stencil thickness	0.100 mm