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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, IR, POR, PWM, WDT
Number of I/O	54
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 28x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8l151r6t6

1 Introduction

This document describes the features, pinout, mechanical data and ordering information for: devices.

- **High-density STM8L15xxx devices:** STM8L151x8 and STM8L152x8 microcontrollers with a Flash memory density of 64 Kbyte.
- **Medium+ density STM8L15xxx devices**: STM8L151R6 and STM8L152R6 microcontrollers with Flash memory density of 32 Kbyte.

For further details on the STMicroelectronics ultra-low-power family please refer to *Section 2.3: Ultra-low-power continuum on page 12*.

For detailed information on device operation and registers, refer to the reference manual (RM0031).

For information on to the Flash program memory and data EEPROM, refer to the programming manual (PM0054).

For information on the debug module and SWIM (single wire interface module), refer to the STM8 SWIM communication protocol and debug module user manual (UM0470).

For information on the STM8 core, refer to the STM8 CPU programming manual (PM0044).

2 Description

The high-density and medium+ density STM8L15xx6/8 ultra-low-power devices feature an enhanced STM8 CPU core providing increased processing power (up to 16 MIPS at 16 MHz) while maintaining the advantages of a CISC architecture with improved code density, a 24-bit linear addressing space and an optimized architecture for low-power operations.

The family includes an integrated debug module with a hardware interface (SWIM) which allows non-intrusive in-application debugging and ultrafast Flash programming.

All high-density and medium+ density STM8L15xx6/8 microcontrollers feature embedded data EEPROM and low-power low-voltage single-supply program Flash memory.

The devices incorporate an extensive range of enhanced I/Os and peripherals, a 12-bit ADC, two DACs, two comparators, a real-time clock, four 16-bit timers, one 8-bit timer, as well as standard communication interfaces such as two SPIs, an I^2C interface, and three USARTs. A 8x40 or 4x44-segment LCD is available on the STM8L152x8 devices. The modular design of the peripheral set allows the same peripherals to be found in different ST microcontroller families including 32-bit families. This makes any transition to a different family very easy, and simplified even more by the use of a common set of development tools.

3.12 System configuration controller and routing interface

The system configuration controller provides the capability to remap some alternate functions on different I/O ports. TIM4 and ADC1 DMA channels can also be remapped.

The highly flexible routing interface allows application software to control the routing of different I/Os to the TIM1 timer input captures. It also controls the routing of internal analog signals to ADC1, COMP1, COMP2, DAC1 and the internal reference voltage V_{REFINT}. It also provides a set of registers for efficiently managing the charge transfer acquisition sequence (see *Section 3.13: Touch sensing*).

3.13 Touch sensing

The high-density and medium+ density STM8L15xx6/8 devices provide a simple solution for adding capacitive sensing functionality to any application. Capacitive sensing technology is able to detect finger presence near an electrode which is protected from direct touch by a dielectric (for example glass or plastic). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists of charging the electrode capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. In the high-density and medium+ density STM8L15xx6/8 devices, the acquisition sequence is managed by software and it involves analog I/O groups and the routing interface.

Reliable touch sensing solution can be quickly and easily implemented using the free STM8 touch sensing firmware library.

3.14 Timers

The high-density and medium+ density STM8L15xx6/8 devices contain one advanced control timer (TIM1), three 16-bit general purpose timers (TIM2,TIM3 and TIM5) and one 8-bit basic timer (TIM4).

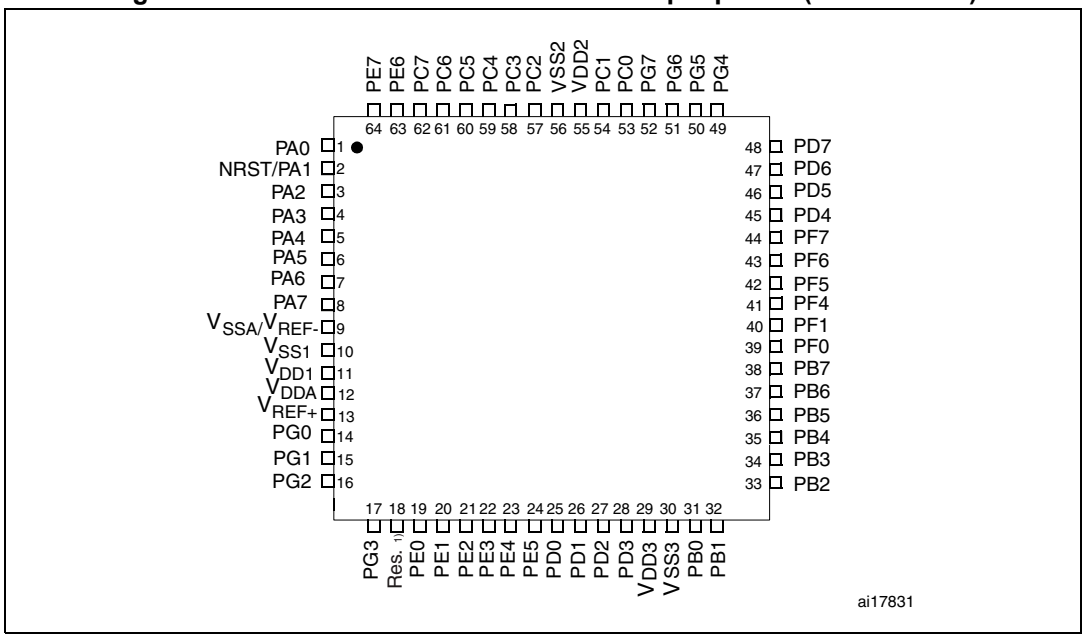
All the timers can be served by DMA1.

Table 3 compares the features of the advanced control, general-purpose and basic timers.

Table 3. Timer feature comparison

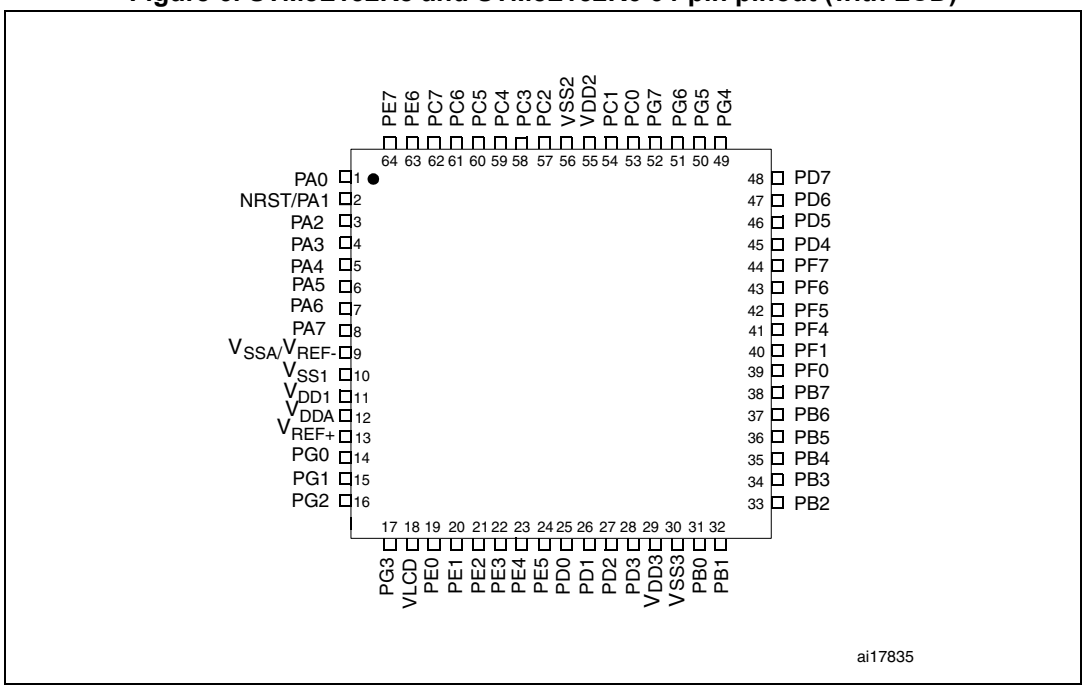
Timer	Counter resolution	Counter type	Prescaler factor	DMA1 request generation	Capture/compare channels	Complementary outputs
TIM1	16-bit	up/down	Any integer from 1 to 65536	Yes	3 + 1	3
TIM2			Any power of 2 from 1 to 128		2	None
TIM3						
TIM5						
TIM4	8-bit	up	Any power of 2 from 1 to 32768		0	

Figure 5. STM8L151R8 and STM8L151R6 64-pin pinout (without LCD)



1. Pin 18 is reserved and must be tied to V_{DD}.
2. The above figure shows the package top view.

Figure 6. STM8L152R8 and STM8L152R6 64-pin pinout (with LCD)



1. The above figure shows the package top view.

Table 5. High-density and medium+ density STM8L15x pin description (continued)

Pin number				Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP80	LQFP64	UFQFPN48 and LQFP48	WLCSP32				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
48	-	-	-	V_{SS4}	S	-	-	-	-	-	-	-	IOs ground voltage	
47	-	-	-	V_{DD4}	S	-	-	-	-	-	-	-	IOs supply voltage	

1. At power-up, the PA1/NRST pin is a reset input pin with pull-up. To be used as a general purpose pin (PA1), it can be configured only as output push-pull, not as output open-drain nor as a general purpose input. Refer to Section *Configuring NRST/PA1 pin as general purpose output* in the STM8L15xxx and STM8L16xxx reference manual (RM0031).
2. [ ] Alternate function remapping option (if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).
3. Available on STM8L152x6/8 devices only.
4. Even if this I/O is not available on the device pin, it is considered as active and must be configured to input pull up or output mode by software to avoid spurious behavior and increased consumption.
5. A pull-up is applied to PB0 and PB4 during the reset phase. These two pins are input floating after reset release.
6. In the 5 V tolerant I/Os, the protection diode to V_{DD} is not implemented.
7. In the open-drain output column, 'T' defines a true open-drain I/O (P-buffer, weak pull-up and protection diode to V_{DD} are not implemented).
8. Available on STM8L152xx devices only. On STM8L151xx devices it is reserved and must be tied to V_{DD}.
9. The PA0 pin is in input pull-up during the reset phase and after reset release.
10. High Sink LED driver capability available on PA0.

Note: Slope control of all GPIO pins can be programmed except true open drain pins and by default is limited to 2 MHz.

System configuration options

As shown in *Table 5: High-density and medium+ density STM8L15x pin description*, some alternate functions can be remapped on different I/O ports by programming one of the two remapping registers described in the "Routing interface (RI) and system configuration controller" section in the STM8L05xxx, STM8L15xxx and STM8L16xxx reference manual (RM0031).

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 516A	RTC	RTC_CALRH	Calibration register high	0x00(1)
0x00 516B		RTC_CALRL	Calibration register low	0x00(1)
0x00 516C		RTC_TCR1	Tamper control register 1	0x00(1)
0x00 516D		RTC_TCR2	Tamper control register 2	0x00(1)
0x00 516E to 0x00 518A	Reserved area			
0x00 5190	CSSLSE	CSSLSE_CSR	CSS on LSE control and status register	0x00(1)
0x00 519A to 0x00 51FF	Reserved area			
0x00 5200	SPI1	SPI1_CR1	SPI1 control register 1	0x00
0x00 5201		SPI1_CR2	SPI1 control register 2	0x00
0x00 5202		SPI1_ICR	SPI1 interrupt control register	0x00
0x00 5203		SPI1_SR	SPI1 status register	0x02
0x00 5204		SPI1_DR	SPI1 data register	0x00
0x00 5205		SPI1_CRCPR	SPI1 CRC polynomial register	0x07
0x00 5206		SPI1_RXCRCR	SPI1 Rx CRC register	0x00
0x00 5207		SPI1_TXCRCR	SPI1 Tx CRC register	0x00
0x00 5208 to 0x00 520F	Reserved area (8 byte)			
0x00 5210	I2C1	I2C1_CR1	I2C1 control register 1	0x00
0x00 5211		I2C1_CR2	I2C1 control register 2	0x00
0x00 5212		I2C1_FREQR	I2C1 frequency register	0x00
0x00 5213		I2C1_OARL	I2C1 own address register low	0x00
0x00 5214		I2C1_OARH	I2C1 own address register high	0x00
0x00 5215		I2C1_OARH	I2C1 own address register for dual mode	0x00
0x00 5216		I2C1_DR	I2C1 data register	0x00
0x00 5217		I2C1_SR1	I2C1 status register 1	0x00
0x00 5218		I2C1_SR2	I2C1 status register 2	0x00
0x00 5219		I2C1_SR3	I2C1 status register 3	0x0X
0x00 521A		I2C1_ITR	I2C1 interrupt control register	0x00
0x00 521B		I2C1_CCRL	I2C1 clock control register low	0x00
0x00 521C		I2C1_CCRH	I2C1 clock control register high	0x00
0x00 521D		I2C1_TRISER	I2C1 TRISE register	0x02
0x00 521E		I2C1_PECR	I2C1 packet error checking register	0x00

Table 9. General hardware register map (continued)

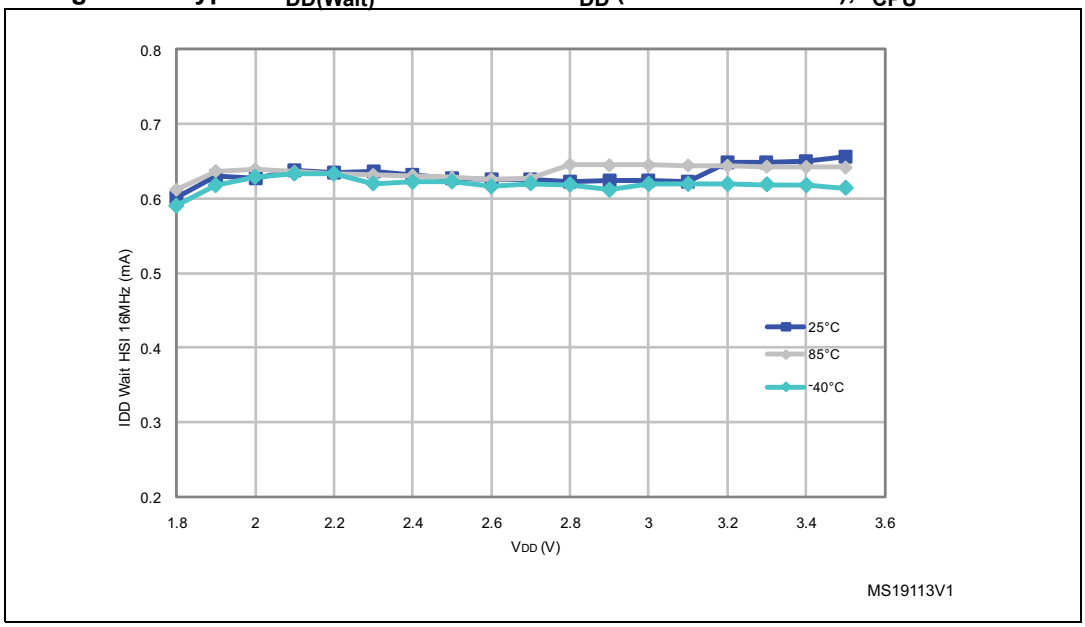
Address	Block	Register label	Register name	Reset status
0x00 5386 to 0x00 5387	Reserved area (2 byte)			
0x00 5388	DAC	DAC_CH1RDHRH	DAC channel 1 right aligned data holding register high	0x00
0x00 5389		DAC_CH1RDHRL	DAC channel 1 right aligned data holding register low	0x00
0x00 538A to 0x00 538B	Reserved area (2 byte)			
0x00 538C	DAC	DAC_CH1LDHRH	DAC channel 1 left aligned data holding register high	0x00
0x00 538D	DAC	DAC_CH1LDHRL	DAC channel 1 left aligned data holding register low	0x00
0x00 538E to 0x00 538F	Reserved area (2 byte)			
0x00 5390	DAC	DAC_CH1DHR8	DAC channel 1 8-bit data holding register	0x00
0x00 5391 to 0x00 5393	Reserved area (3 byte)			
0x00 5394	DAC	DAC_CH2RDHRH	DAC channel 2 right aligned data holding register high	0x00
0x00 5395		DAC_CH2RDHRL	DAC channel 2 right aligned data holding register low	0x00
0x00 5396 to 0x00 5397	Reserved area (2 byte)			
0x00 5398	DAC	DAC_CH2LDHRH	DAC channel 2 left aligned data holding register high	0x00
0x00 5399		DAC_CH2LDHRL	DAC channel 2 left aligned data holding register low	0x00
0x00 539A to 0x00 539B	Reserved area (2 byte)			
0x00 539C	DAC	DAC_CH2DHR8	DAC channel 2 8-bit data holding register	0x00
0x00 539D to 0x00 539F	Reserved area (3 byte)			
0x00 53A0	DAC	DAC_DCH1RDHRH	DAC channel 1 right aligned data holding register high	0x00
0x00 53A1		DAC_DCH1RDHRL	DAC channel 1 right aligned data holding register low	0x00
0x00 53A2 to 0x00 53AB	Reserved area (3 byte)			

In the following table, data are based on characterization results, unless otherwise specified.

Table 21. Total current consumption in Wait mode

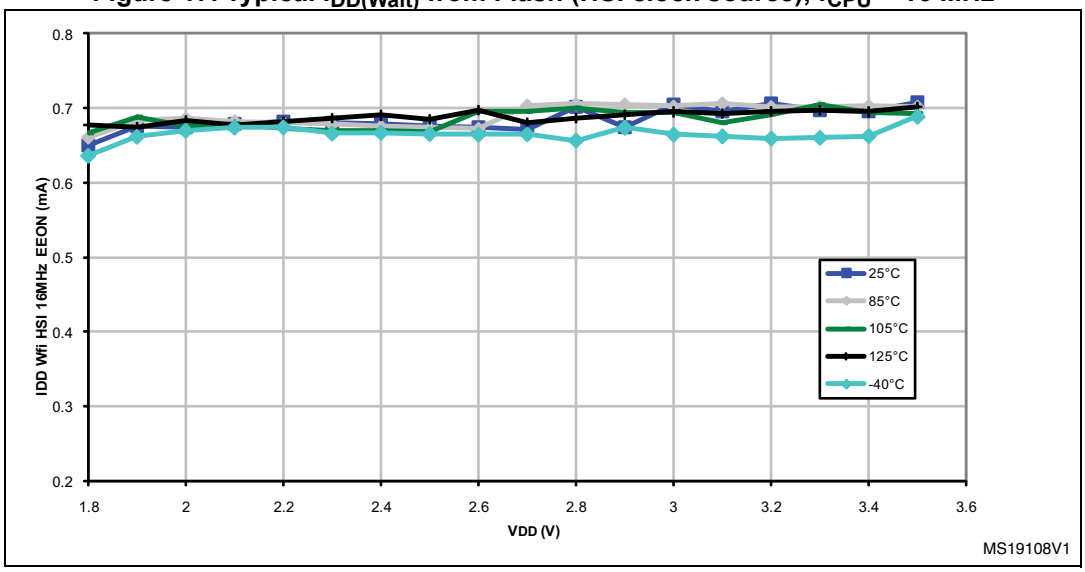
Symbol	Parameter	Conditions[1]			Typ	Max				Unit
						55°C	85 °C (2)	105 °C (3)	125 °C (4)	
$I_{DD(Wait)}$	Supply current in Wait mode	CPU not clocked, all peripherals OFF, code executed from RAM with Flash in I_{DDQ} mode,[5] V_{DD} from 1.65 V to 3.6 V	HSI	f_{CPU} = 125 kHz	0.21	0.29	0.33	0.36	0.43	mA
				f_{CPU} = 1 MHz	0.25	0.33	0.37	0.4	0.47	
				f_{CPU} = 4 MHz	0.32	0.4	0.44	0.47	0.54	
				f_{CPU} = 8 MHz	0.42	0.496	0.54	0.56	0.64	
				f_{CPU} = 16 MHz	0.66	0.736	0.78[6]	0.8[6]	0.88[6]	
			HSE external clock (f_{CPU}=f_{HSE}) (7)	f_{CPU} = 125 kHz	0.19	0.21	0.3	0.35	0.41	
				f_{CPU} = 1 MHz	0.2	0.23	0.32	0.36	0.43	
				f_{CPU} = 4 MHz	0.27	0.3	0.39	0.43	0.5	
				f_{CPU} = 8 MHz	0.37	0.4	0.49	0.53	0.6	
				f_{CPU} = 16 MHz	0.63	0.66	0.75[6]	0.79[6]	0.86[6]	
			LSI	f_{CPU} = f_{LSI}	0.028	0.037	0.039	0.044	0.054	
			LSE[8] external clock (32.768 kHz)	f_{CPU} = f_{LSE}	0.027	0.035	0.038	0.042	0.051	

Figure 16. Typical $I_{DD(Wait)}$ from RAM vs. V_{DD} (HSI clock source), f_{CPU} = 16 MHz



1. Typical current consumption measured with code executed from RAM.

Figure 17. Typical $I_{DD(Wait)}$ from Flash (HSI clock source), f_{CPU} = 16 MHz



1. Typical current consumption measured with code executed from Flash.

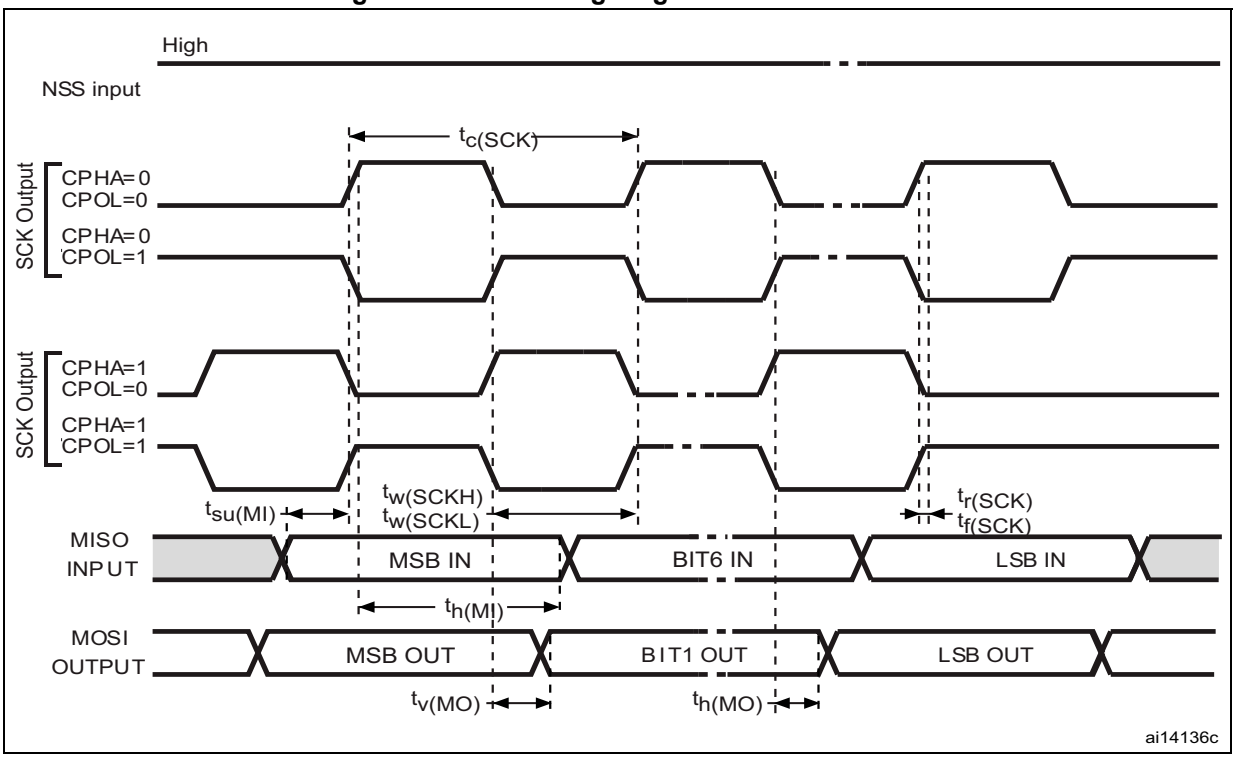
Flash memory

Table 36. Flash program and data EEPROM memory

Symbol	Parameter	Conditions	Min.	Typ.	Max. (1)	Unit
V_{DD}	Operating voltage (all modes, read/write/erase)	f_{SYSCLK} = 16 MHz	1.65		3.6	V
t_{prog}	Programming time for 1 or 128 bytes (block) erase/write cycles (on programmed byte)	-	-	6	-	ms
	Programming time for 1 to 128 bytes (block) write cycles (on erased byte)	-	-	3	-	
I_{prog}	Programming/ erasing consumption	T_A=+25 °C, V_{DD} = 3.0 V	-	0.7	-	mA
		T_A=+25 °C, V_{DD} = 1.8 V	-		-	
t_{RET} (2)	Data retention (program memory) after 10000 erase/write cycles at T_A=-40 to +85 °C (6 suffix)	T_{RET}=+85 °C	30(1)	-	-	years
	Data retention (program memory) after 10000 erase/write cycles at T_A=-40 to +125 °C (3 suffix)	T_{RET}=+125 °C	5(1)	-	-	
	Data retention (data memory) after 300000 erase/write cycles at T_A=-40 to +85 °C (6 suffix)	T_{RET}=+85 °C	30(1)	-	-	
	Data retention (data memory) after 300000 erase/write cycles at T_A=-40 to +125 °C (3 suffix)	T_{RET}=+125 °C	5(1)	-	-	
N_{RW} (3)	Erase/write cycles (program memory)	T_A=-40 to +85 °C (6 suffix), T_A=-40 to +105 °C (7 suffix) or T_A=-40 to +125 °C (3 suffix)	10(1)	-	-	kcycles
	Erase/write cycles (data memory)		300(1) (4)	-	-	

1. Data based on characterization results.
2. Conforming to JEDEC JESD22a117
3. The physical granularity of the memory is 4 bytes, so cycling is performed on 4 bytes even when a write/erase operation addresses a single byte.
4. Data based on characterization performed on the whole data memory.

Figure 41. SPI1 timing diagram - master mode



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Table 49. Comparator 2 characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
V_{DDA}	Analog supply voltage	-	1.65		3.6	V
V_{IN}	Comparator 2 input voltage range	-	0		V_{DDA}	V
t_{START}	Comparator startup time	Fast mode	-	15	20	µs
		Slow mode	-	20	25	
$t_{d\ slow}$	Propagation delay(2) in slow mode	1.65 V ≤ V_{DDA} ≤ 2.7 V	-	1.8	3.5	
		2.7 V ≤ V_{DDA} ≤ 3.6 V	-	2.5	6	
$t_{d\ fast}$	Propagation delay(2) in fast mode	1.65 V ≤ V_{DDA} ≤ 2.7 V	-	0.8	2	
		2.7 V ≤ V_{DDA} ≤ 3.6 V	-	1.2	4	
V_{offset}	Comparator offset error	-	-	±4	±20	mV
$d_{Threshold}/dt$	Threshold voltage temperature coefficient	V_{DDA} = 3.3V T_A = 0 to 50 °C V- = V_{REF+}, 3/4 V_{REF+}, 1/2 V_{REF+}, 1/4 V_{REF+}.	-	15	30	ppm /°C
I_{COMP2}	Current consumption(3)	Fast mode	-	3.5	5	µA
		Slow mode	-	0.5	2	

1. Based on characterization.
2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.
3. Comparator consumption only. Internal reference voltage (necessary for comparator operation) is not included.

Table 53. ADC1 characteristics (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_S	Sampling time	V_{AIN} PF0/1/2/3 fast channels V_{DDA} < 2.4 V	0.43(3)(4)	-	-	µs
		V_{AIN} PF0/1/2/3 fast channels 2.4 V ≤V_{DDA}≤ 3.6 V	0.22(3)(4)	-	-	
		V_{AIN} on slow channels V_{DDA} < 2.4 V	0.86(3)(4)	-	-	
		V_{AIN} on slow channels 2.4 V ≤V_{DDA}≤ 3.6 V	0.41(3)(4)	-	-	
t_{conv}	12-bit conversion time	-	12 + t_S			$1/f_{ADC}$
		16 MHz	1(3)			µs
t_{WKUP}	Wakeup time from OFF state	-	-	-	3	µs
t_{IDLE}(5)	Time before a new conversion	-	-	-	∞	s
$t_{VREFINT}$	Internal reference voltage startup time	-	-	-	refer to *Table 46*	ms

1. The current consumption through V_{REF} is composed of two parameters:
   - one constant (max 300 µA)
   - one variable (max 400 µA), only during sampling time + 2 first conversion pulses.
   So, peak consumption is 300+400 = 700 µA and average consumption is 300 + [(4 sampling + 2) /16] x 400 = 450 µA at 1Msps
2. V_{REF-} must be tied to ground.
3. Minimum sampling and conversion time is reached for maximum R_{AIN}= 0.5 kΩ.
4. Value obtained for continuous conversion on fast channel.
5. The time between 2 conversions, or between ADC ON and the first conversion must be lower than t_{IDLE}.

Figure 43. ADC1 accuracy characteristics

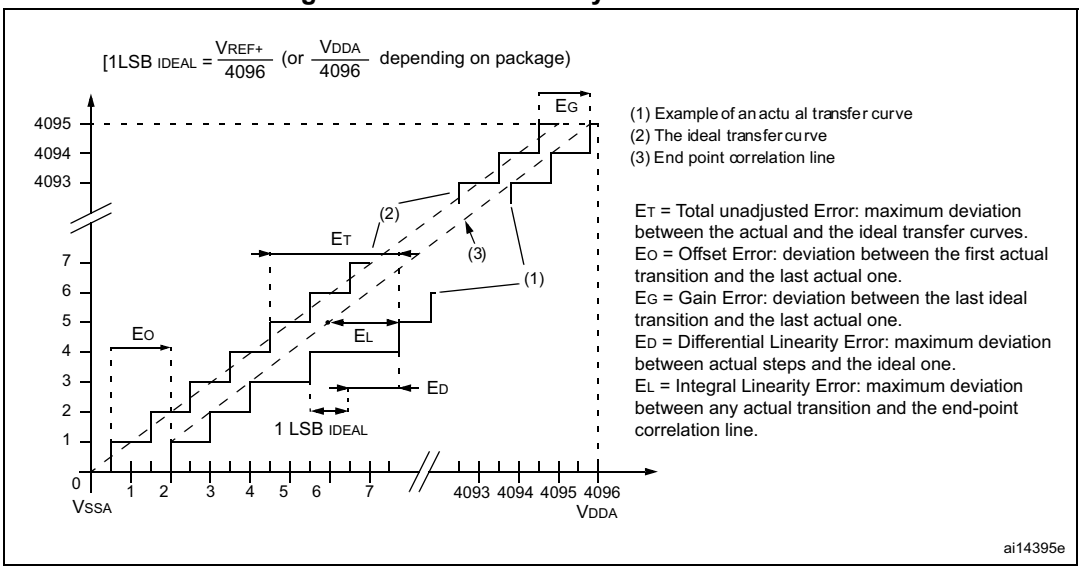
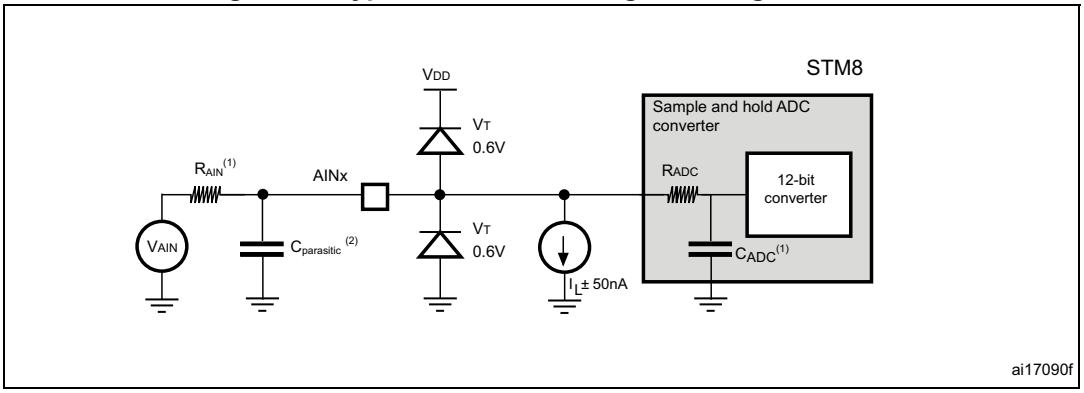


Figure 44. Typical connection diagram using the ADC



1. Refer to *Table 53* for the values of R_{AIN} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

9.3.15 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

Functional EMS (electromagnetic susceptibility)

Based on a simple running application on the product (toggling 2 LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electrostatic discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 61000 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 61000 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Prequalification trials:

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Table 58. EMS data

Symbol	Parameter	Conditions		Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{CPU}= 16 MHz, conforms to IEC 61000		2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{CPU} = 16 MHz, conforms to IEC 61000	Using HSI	4A
			Using HSE	2B

Electromagnetic interference (EMI)

Based on a simple application running on the product (toggling 2 LEDs through the I/O ports), the product is monitored in terms of emission. This emission test is in line with the norm IEC61967-2 which specifies the board and the loading of each pin.

Table 59. EMI data (1)

Symbol	Parameter	Conditions	Monitored frequency band	Max vs.	Unit
				16 MHz	
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = +25 °C, LQFP80 conforming to IEC61967-2	0.1 MHz to 30 MHz	10	dBµV
			30 MHz to 130 MHz	4	
			130 MHz to 1 GHz	1	
			SAE EMI Level	1.5	-

1. Not tested in production.

Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). Two models can be simulated: human body model and charge device model. This test conforms to the JESD22-A114A/C101 or ANSI/ESD STM5.3.1 standards.

Table 60. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Package	Class	Maximum value (1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to JESD22-A414	All	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to ANSI/ESD STM5.3.1	WLCSP32	TBD	TBD	
		T_A = +25 °C, conforming to JESD22-C101	All other	II	500	

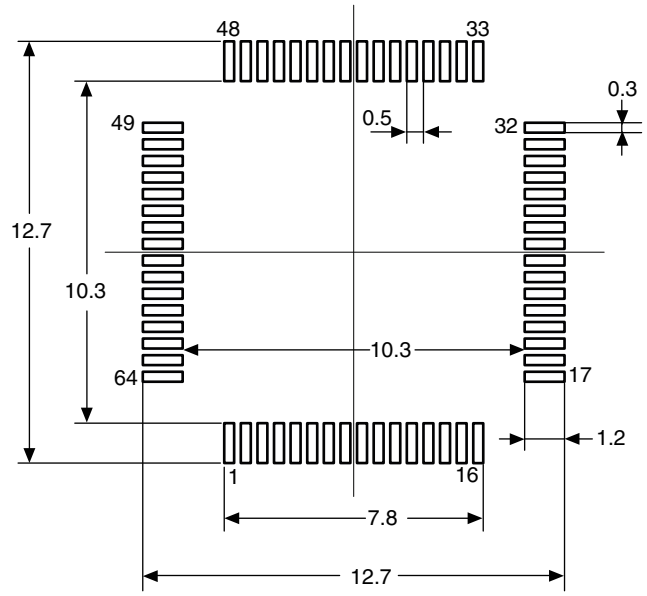
1. Data based on characterization results.

Table 64. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 52. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package recommended footprint



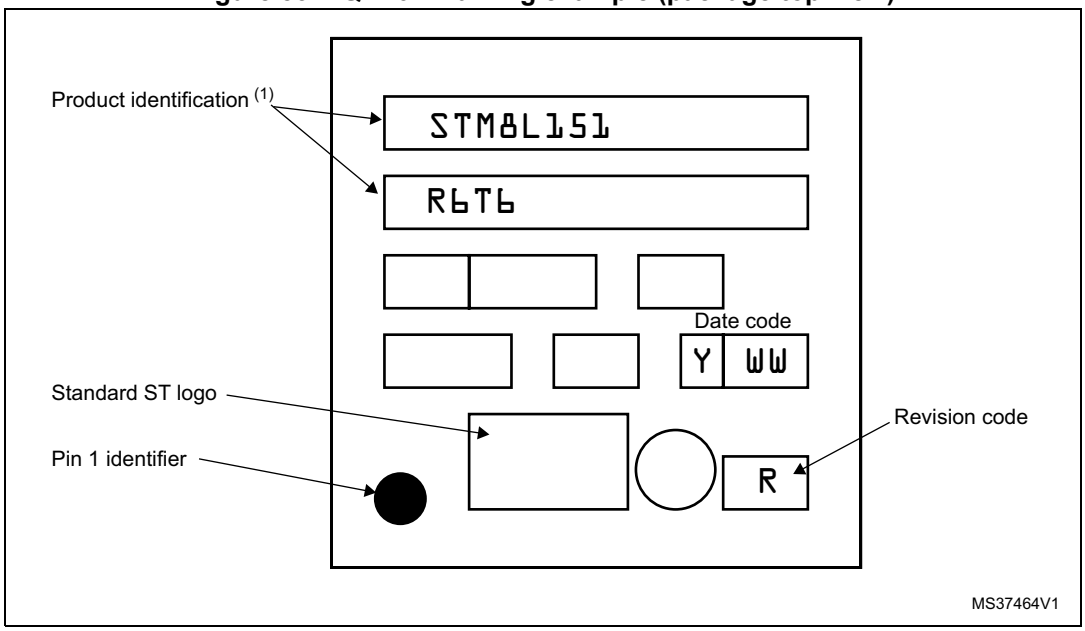
1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 53. LQFP64 marking example (package top view)



1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 65. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

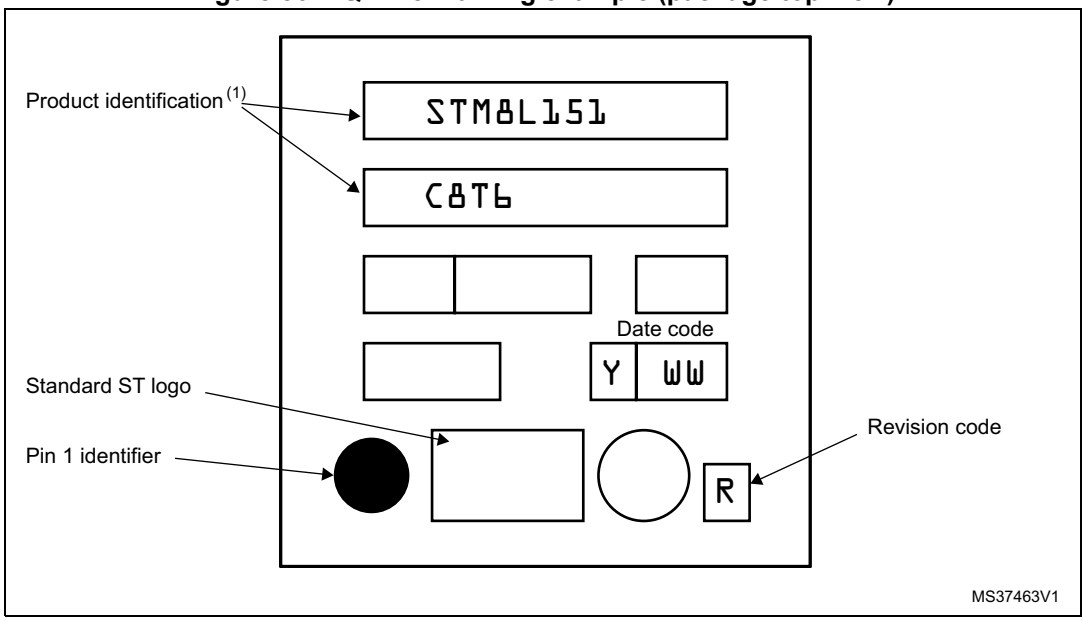
1. Values in inches are converted from mm and rounded to 4 decimal digits.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 56. LQFP48 marking example (package top view)



1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.