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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, IR, POR, PWM, WDT
Number of I/O	54
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 28x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8l151r8t3

2.1 STM8L ultra-low-power 8-bit family benefits

High-density and medium+ density STM8L15xx6/8 devices are part of the STM8L ultra-low-power family providing the following benefits:

- Integrated system
  - Up to 64 Kbyte of high-density embedded Flash program memory
  - Up to 2 Kbyte of data EEPROM
  - Up to 4 Kbyte of RAM
  - Internal high-speed and low-power low speed RC.
  - Embedded reset
- ultra-low-power consumption
  - 1 µA in Active-halt mode
  - Clock gated system and optimized power management
  - Capability to execute from RAM for Low-power wait mode and Low-power run mode
- Advanced features
  - Up to 16 MIPS at 16 MHz CPU clock frequency
  - Direct memory access (DMA) for memory-to-memory or peripheral-to-memory access.
- Short development cycles
  - Application scalability across a common family product architecture with compatible pinout, memory map and modular peripherals.
  - Wide choice of development tools

STM8L ultra-low-power microcontrollers can operate either from 1.8 to 3.6 V (down to 1.65 V at power-down) or from 1.65 to 3.6 V. They are available in the -40 to +85 °C and -40 to +125 °C temperature ranges.

These features make the STM8L ultra-low-power microcontroller families suitable for a wide range of applications:

- Medical and handheld equipment
- Application control and user interface
- PC peripherals, gaming, GPS and sport equipment
- Alarm systems, wired and wireless sensors
- Metering

The devices are offered in five different packages from 32 to 80 pins. Different sets of peripherals are included depending on the device. Refer to *Section 3* for an overview of the complete range of peripherals proposed in this family.

All STM8L ultra-low-power products are based on the same architecture with the same memory mapping and a coherent pinout.

Figure 1 shows the block diagram of the High-density and medium+ density STM8L15xx6/8 families.

3.14.1 16-bit advanced control timer (TIM1)

This is a high-end timer designed for a wide range of control applications. With its complementary outputs, dead-time control and center-aligned PWM capability, the field of applications is extended to motor control, lighting and half-bridge driver.

- 16-bit up, down and up/down autoreload counter with 16-bit prescaler
- 3 independent capture/compare channels (CAPCOM) configurable as input capture, output compare, PWM generation (edge and center aligned mode) and single pulse mode output
- 1 additional capture/compare channel which is not connected to an external I/O
- Synchronization module to control the timer with external signals
- Break input to force timer outputs into a defined state
- 3 complementary outputs with adjustable dead time
- Encoder mode
- Interrupt capability on various events (capture, compare, overflow, break, trigger)

3.14.2 16-bit general purpose timers (TIM2, TIM3, TIM5)

- 16-bit autoreload (AR) up/down-counter
- 7-bit prescaler adjustable to fixed power of 2 ratios (1…128)
- 2 individually configurable capture/compare channels
- PWM mode
- Interrupt capability on various events (capture, compare, overflow, break, trigger)
- Synchronization with other timers or external signals (external clock, reset, trigger and enable)

3.14.3 8-bit basic timer (TIM4)

The 8-bit timer consists of an 8-bit up auto-reload counter driven by a programmable prescaler. It can be used for timebase generation with interrupt generation on timer overflow or for DAC trigger generation.

3.15 Watchdog timers

The watchdog system is based on two independent timers providing maximum security to the applications.

3.15.1 Window watchdog timer

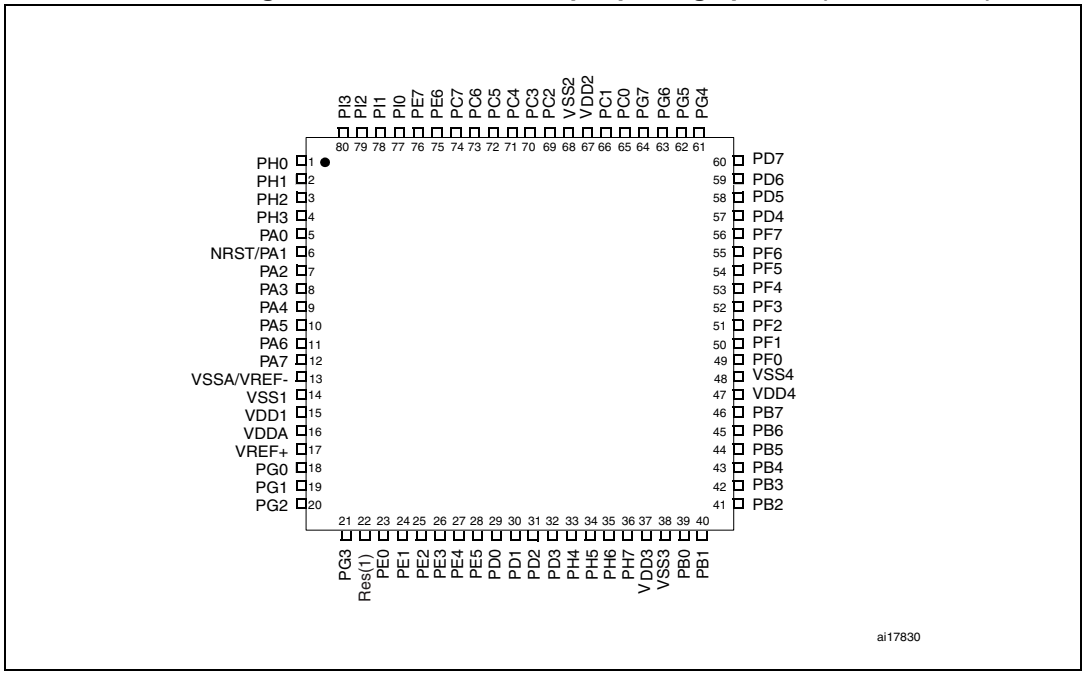
The window watchdog (WWDG) is used to detect the occurrence of a software fault, usually generated by external interferences or by unexpected logical conditions, which cause the application program to abandon its normal sequence.

3.15.2 Independent watchdog timer

The independent watchdog peripheral (IWDG) can be used to resolve processor malfunctions due to hardware or software failures.

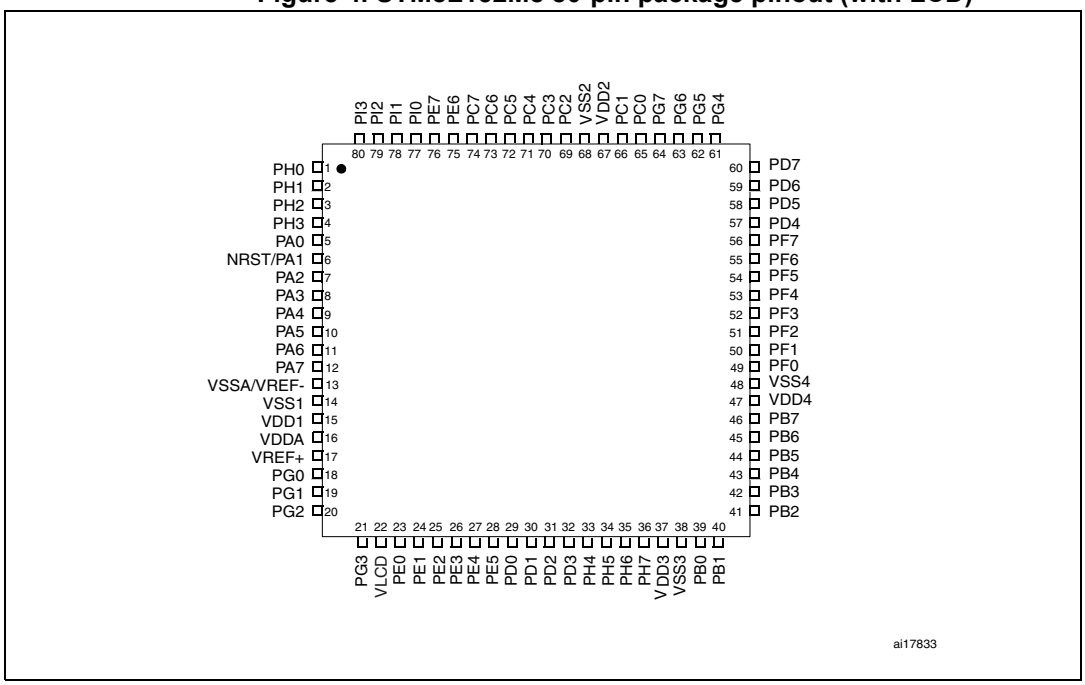
4 Pin description

Figure 3. STM8L151M8 80-pin package pinout (without LCD)



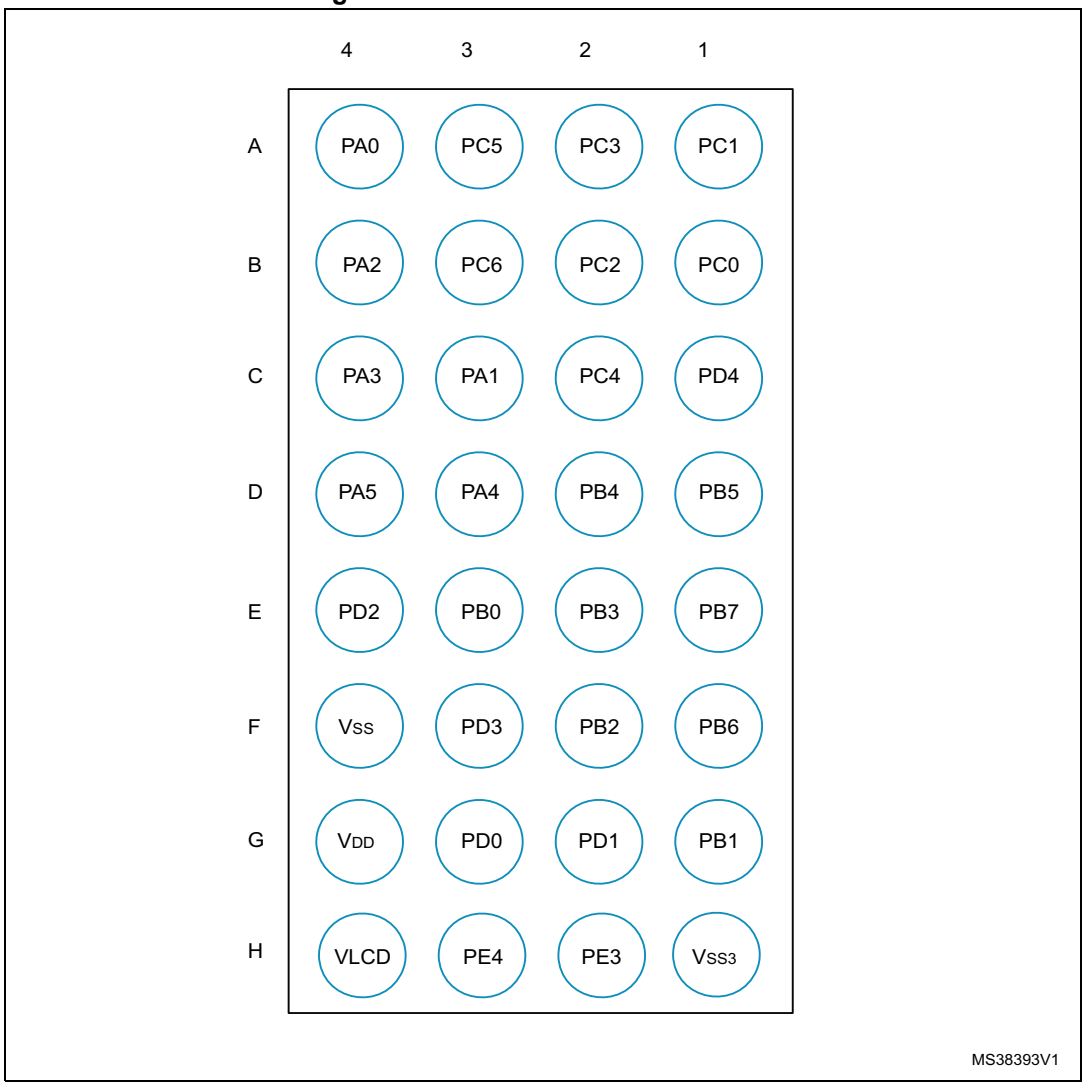
1. Pin 22 is reserved and must be tied to V_{DD}.
2. The above figure shows the package top view.

Figure 4. STM8L152M8 80-pin package pinout (with LCD)



1. The above figure shows the package top view.

Figure 9. STM8L152K8 32-ball ballout



Warning: **For the 32-pin STM8L152K8 devices, some active I/O pins are not bonded out of the package. Effectively, all ports available on 48-pin devices must be considered as active ports also for 32-pin devices - see *Table 5: High-density and medium+ density STM8L15x pin description* for more details. To avoid spurious effects, users have to configure active ports as input pull-up. A small increase in consumption (typ. < 300 µA) may occur during the power up and reset phase until these ports are properly configured.**

Table 5. High-density and medium+ density STM8L15x pin description (continued)

Pin number				Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP80	LQFP64	UFQFPN48 and LQFP48	WLCSP32				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
44	36	-	-	PB5/SPI1_SCK/ LCD_SEG15(3)/ADC1_IN13 / *[COMP1_INP]*	I/O	FT(6)	**X**	X	X	HS	X	X	**Port B5**	SPI1 clock / LCD segment 15 / ADC1_IN13/ *[Comparator 1 positive input]*
-	-	29	D1	PB5/SPI1_SCK/ LCD_SEG15(3)/ADC1_IN13 /DAC_OUT2/ *[COMP1_INP]*	I/O	FT(6)	**X**	X	X	HS	X	X	**Port B5**	[SPI1 clock] / LCD segment 15 / ADC1_IN13 / DAC channel 2 output/ *[Comparator 1 positive input]*
45	37	-	-	PB6/SPI1_MOSI/ LCD_SEG16(3)/ADC1_IN12 /*[COMP1_INP]*	I/O	FT(6)	**X**	X	X	HS	X	X	**Port B6**	SPI1 master out/slave in/ LCD segment 16 / ADC1_IN12/ *[Comparator 1 positive input]*
-	-	30	F1	PB6/SPI1_MOSI/ LCD_SEG16(3)/ADC1_IN12 /DAC_OUT2/*[COMP1_INP]*	I/O	FT(6)	**X**	X	X	HS	X	X	**Port B6**	SPI1 master out/ slave in / LCD segment 16 / ADC1_IN12 / DAC channel 2 output/*[Comparator 1 positive input]*
46	38	31	E1	PB7/SPI1_MISO/ LCD_SEG17(3)/ ADC1_IN11/*[COMP1_INP]*	I/O	FT(6)	**X**	X	X	HS	X	X	**Port B7**	SPI1 master in- slave out/ LCD segment 17 / ADC1_IN11/*[Comparator 1 positive input]*
65	53	37	B1	PC0/I2C1_SDA	I/O	FT(6)	**X**	-	X		T(7)		**Port C0**	I2C1 data
66	54	38	A1	PC1/I2C1_SCL	I/O	FT(6)	**X**	-	X		T(7)		**Port C1**	I2C1 clock
69	57	41	B2	PC2/USART1_RX/ LCD_SEG22/ADC1_IN6/ *[COMP1_INP]* /VREFINT	I/O	FT(6)	**X**	X	X	HS	X	X	**Port C2**	USART1 receive / LCD segment 22 / ADC1_IN6/ *[Comparator 1 positive input]* /Internal reference voltage output
-	-	42	A2	PC3/USART1_TX/ LCD_SEG23(3)/ ADC1_IN5	I/O	FT(6)	**X**	X	X	HS	X	X	**Port C3**	USART1 transmit / LCD segment 23 / ADC1_IN5

Table 5. High-density and medium+ density STM8L15x pin description (continued)

Pin number				Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP80	LQFP64	UFQFPN48 and LQFP48	WLCSP32				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
-	-	46	-(4)	PC7/LCD_SEG25(3)/ ADC1_IN3/USART3_CK/ *[COMP2_INM]* / *[COMP1_INP]* / *[LCD_COM5]*	I/O	FT(6)	**X**	X	X	HS	X	X	**Port C7**	LCD segment 25 /ADC1_IN3/ USART3 synchronous clock/ *[Comparator 2 negative input]* / *[Comparator 1 positive input]*/ *[LCD_COM5]*(3)
29	25	20	G3	PD0/TIM3_CH2/ *[ADC1_TRIG]*(2)/ LCD_SEG7(3)/ADC1_IN22/ *[COMP2_INP]*	I/O	FT(6)	**X**	X	X	HS	X	X	**Port D0**	Timer 3 - channel 2 / *[ADC1_Trigger]* / LCD segment 7 / ADC1_IN22 / *[Comparator 2 positive input]*
30	26	21	G2	PD1/TIM3_ETR/ LCD_COM3(3)/ADC1_IN21/ *[COMP1_INP]*// *[COMP2_INP]*	I/O	FT(6)	**X**	X	X	HS	X	X	**Port D1**	Timer 3 - trigger / LCD_COM3 / ADC1_IN21 / *[Comparator 1 positive input]* /*[Comparator 2 positive input]*
31	27	22	E4	PD2/TIM1_CH1 /LCD_SEG8(3)/ADC1_IN20/ *[COMP1_INP]*	I/O	FT(6)	**X**	X	X	HS	X	X	**Port D2**	Timer 1 - channel 1 / LCD segment 8 / ADC1_IN20/ *[Comparator 1 positive input]*
32	28	23	F3	PD3/ TIM1_ETR/ LCD_SEG9(3)/ ADC1_IN19/ *[COMP1_INP]*	I/O	FT(6)	**X**	X	X	HS	X	X	**Port D3**	Timer 1 - trigger / LCD segment 9 / ADC1_IN19/ *[Comparator 1 positive input]*
57	45	-	-	PD4/TIM1_CH2 /LCD_SEG18(3)/ ADC1_IN10/ *[COMP1_INP]*	I/O	FT(6)	**X**	X	X	HS	X	X	**Port D4**	Timer 1 - channel 2 / LCD segment 18 / ADC1_IN10/ *[Comparator 1 positive input]*
-	-	33	C1	PD4/TIM1_CH2 /LCD_SEG18(3)/ ADC1_IN10/SPI2_MISO/ *[COMP1_INP]*	I/O	FT(6)	**X**	X	X	HS	X	X	**Port D4**	Timer 1 - channel 2 / LCD segment 18 / ADC1_IN10/SPI2 master in/slave out/ *[Comparator 1 positive input]*

Table 5. High-density and medium+ density STM8L15x pin description (continued)

Pin number				Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP80	LQFP64	UFQFPN48 and LQFP48	WLCSP32				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
48	-	-	-	V_{SS4}	S	-	-	-	-	-	-	-	IOs ground voltage	
47	-	-	-	V_{DD4}	S	-	-	-	-	-	-	-	IOs supply voltage	

1. At power-up, the PA1/NRST pin is a reset input pin with pull-up. To be used as a general purpose pin (PA1), it can be configured only as output push-pull, not as output open-drain nor as a general purpose input. Refer to Section *Configuring NRST/PA1 pin as general purpose output* in the STM8L15xxx and STM8L16xxx reference manual (RM0031).
2. [ ] Alternate function remapping option (if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).
3. Available on STM8L152x6/8 devices only.
4. Even if this I/O is not available on the device pin, it is considered as active and must be configured to input pull up or output mode by software to avoid spurious behavior and increased consumption.
5. A pull-up is applied to PB0 and PB4 during the reset phase. These two pins are input floating after reset release.
6. In the 5 V tolerant I/Os, the protection diode to V_{DD} is not implemented.
7. In the open-drain output column, 'T' defines a true open-drain I/O (P-buffer, weak pull-up and protection diode to V_{DD} are not implemented).
8. Available on STM8L152xx devices only. On STM8L151xx devices it is reserved and must be tied to V_{DD}.
9. The PA0 pin is in input pull-up during the reset phase and after reset release.
10. High Sink LED driver capability available on PA0.

Note: Slope control of all GPIO pins can be programmed except true open drain pins and by default is limited to 2 MHz.

System configuration options

As shown in *Table 5: High-density and medium+ density STM8L15x pin description*, some alternate functions can be remapped on different I/O ports by programming one of the two remapping registers described in the "Routing interface (RI) and system configuration controller" section in the STM8L05xxx, STM8L15xxx and STM8L16xxx reference manual (RM0031).

8 Unique ID

STM8 devices feature a 96-bit unique device identifier which provides a reference number that is unique for any device and in any context. The 96 bits of the identifier can never be altered by the user.

The unique device identifier can be read in single bytes and may then be concatenated using a custom algorithm.

The unique device identifier is ideally suited:

- For use as serial numbers
- For use as security keys to increase the code security in the program memory while using and combining this unique ID with software cryptographic primitives and protocols before programming the internal memory.
- To activate secure boot processes

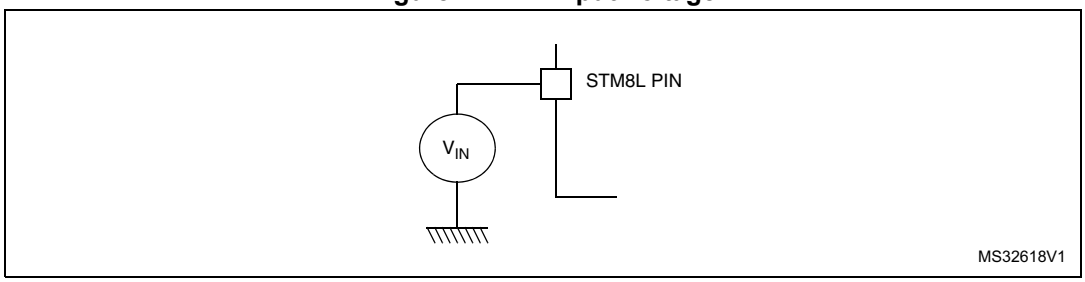
Table 14. Unique ID registers (96 bits)

Address	Content description	Unique ID bits							
		7	6	5	4	3	2	1	0
0x4926	X co-ordinate on the wafer	U_ID[7:0]							
0x4927		U_ID[15:8]							
0x4928	Y co-ordinate on the wafer	U_ID[23:16]							
0x4929		U_ID[31:24]							
0x492A	Wafer number	U_ID[39:32]							
0x492B	Lot number	U_ID[47:40]							
0x492C		U_ID[55:48]							
0x492D		U_ID[63:56]							
0x492E		U_ID[71:64]							
0x492F		U_ID[79:72]							
0x4930		U_ID[87:80]							
0x4931		U_ID[95:88]							

9.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 12*.

Figure 12. Pin input voltage



9.2 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Device mission profile(application conditions)is compliant with JEDEC JESD47 Qualification Standard. Extended mission profiles are available on demand.

Table 15. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD}- V_{SS}	External supply voltage (including V_{DDA})(1)	- 0.3	4.0	V
V_{IN}(2)	Input voltage on true open-drain pins (PC0 and PC1)	V_{SS} - 0.3	V_{DD} + 4.0	
	Input voltage on five-volt tolerant (FT) pins	V_{SS} - 0.3	V_{DD} + 4.0	
	Input voltage on any other pin	V_{SS} - 0.3	4.0	
V_{ESD}	Electrostatic discharge voltage	see *Absolute maximum ratings (electrical sensitivity) on page 122*		

1. All power (V_{DD1}, V_{DD2}, V_{DD3}, V_{DD4}, V_{DDA}) and ground (V_{SS1}, V_{SS2}, V_{SS3}, V_{SS4}, V_{SSA}) pins must always be connected to the external power supply.
2. V_{IN} maximum must always be respected. Refer to *Table 16.* for maximum allowed injected current values.

Table 19. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{PVD0}	PVD threshold 0	Falling edge	1.80	1.84	1.88	V
		Rising edge	1.88	1.94	1.99	
V_{PVD1}	PVD threshold 1	Falling edge	1.98	2.04	2.09	
		Rising edge	2.08	2.14	2.18	
V_{PVD2}	PVD threshold 2	Falling edge	2.2	2.24	2.28	
		Rising edge	2.28	2.34	2.38	
V_{PVD3}	PVD threshold 3	Falling edge	2.39	2.44	2.48	
		Rising edge	2.47	2.54	2.58	
V_{PVD4}	PVD threshold 4	Falling edge	2.57	2.64	2.69	
		Rising edge	2.68	2.74	2.79	
V_{PVD5}	PVD threshold 5	Falling edge	2.77	2.83	2.88	
		Rising edge	2.87	2.94	2.99	
V_{PVD6}	PVD threshold 6	Falling edge	2.97	3.05	3.09	
		Rising edge	3.08	3.15	3.20	
Vhyst	Hysteresis voltage	BOR0 threshold	-	40	-	mV
		All BOR and PVD thresholds excepting BOR0	-	100	-	

1. Data guaranteed by design.
2. Data based on characterization results.

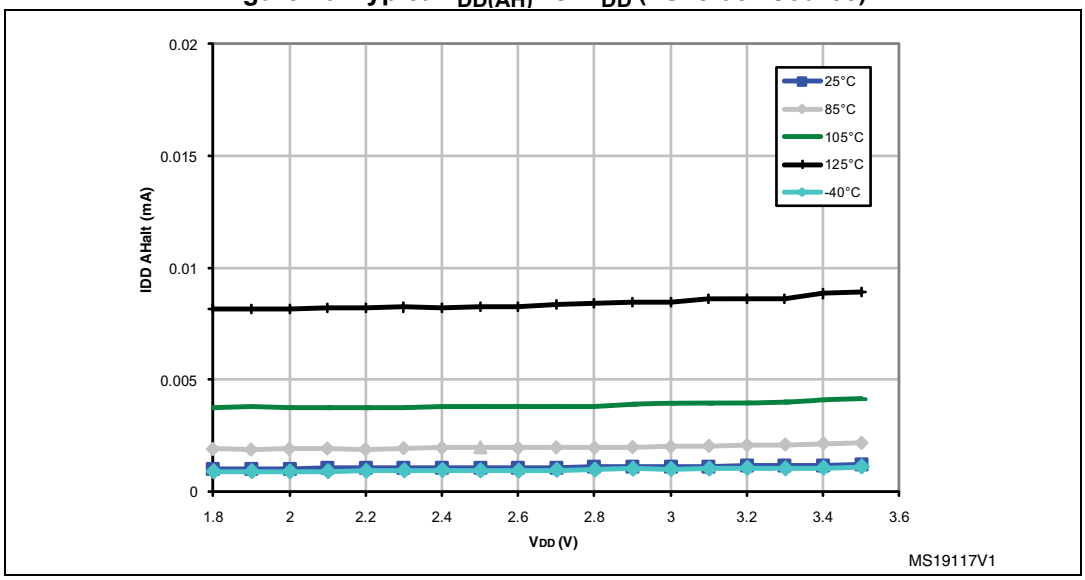
7. RTC enabled. Clock source = LSE
8. Wakeup time until start of interrupt vector fetch.
   The first word of interrupt routine is fetched 4 CPU cycles after t_{WU}.
9. ULP=0 or ULP=1 and FWU=1 in the PWR_CSR2 register.

Table 25. Typical current consumption in Active-halt mode, RTC clocked by LSE external crystal

Symbol	Parameter	Condition(1)		Typ.	Unit
$I_{DD(AH)}$ (2)	Supply current in Active-halt mode	V_{DD} = 1.8 V	LSE	1.2	µA
			LSE/32(3)	0.9	
		V_{DD} = 3 V	LSE	1.4	
			LSE/32(3)	1.1	
		V_{DD} = 3.6 V	LSE	1.6	
			LSE/32(3)	1.3	

1. No floating I/O, unless otherwise specified.
2. Based on measurements on bench with 32.768 kHz external crystal oscillator.
3. RTC clock is LSE divided by 32.

Figure 20. Typical $I_{DD(AH)}$ vs. V_{DD} (LSI clock source)



LSE external clock (LSEBYP=1 in CLK_ECKCR)

The LSE is available on STM8L151xx and STM8L152xx devices only.

Subject to general operating conditions for V_{DD} and T_A.

Table 30. LSE external clock characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{LSE_ext}(1)	External clock source frequency		32.768		kHz
V_{LSEH}(2)	OSC32_IN input pin high level voltage	0.7 x V_{DD}		V_{DD}	V
V_{LSEL}(2)	OSC32_IN input pin low level voltage	V_{SS}		0.3 x V_{DD}	
$C_{in(LSE)}$(1)	OSC32_IN input capacitance		0.6		pF
I_{LEAK_LSE}	OSC32_IN input leakage current			±1	µA

1. Guaranteed by design.
2. Data based on characterization results.

HSE crystal/ceramic resonator oscillator

The HSE clock can be supplied with a 1 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph is based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy...).

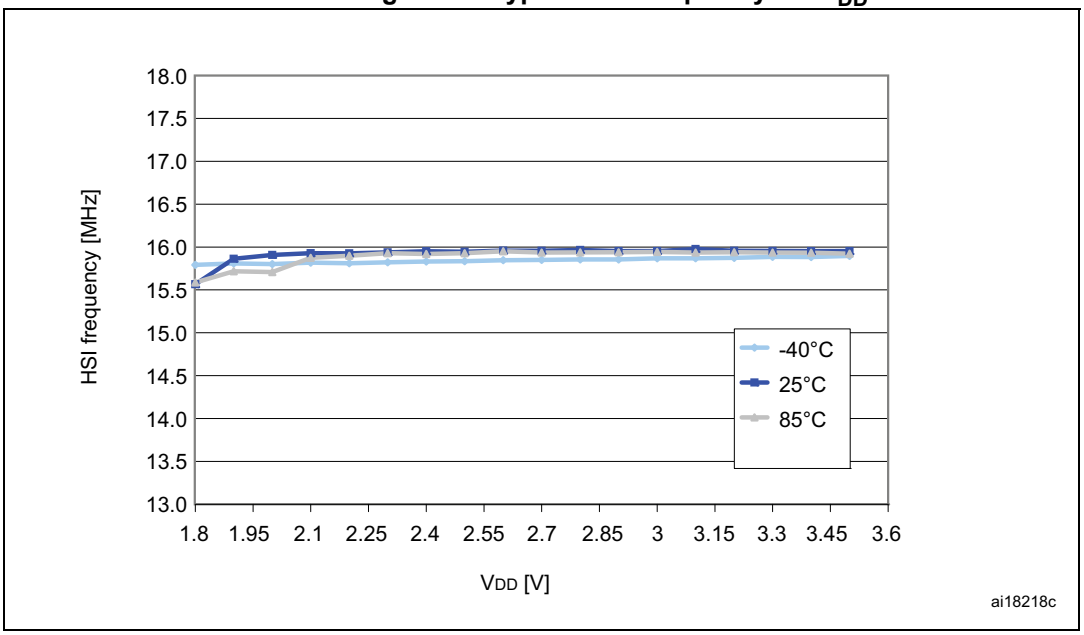
Table 31. HSE oscillator characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{HSE}	High speed external oscillator frequency		1		16	MHz
R_F	Feedback resistor			200		kΩ
C(1)(2)	Recommended load capacitance			20		pF
$I_{DD(HSE)}$	HSE oscillator power consumption	C = 20 pF, f_{OSC} = 16 MHz			2.5 (startup) 0.7 (stabilized)(3)	mA
		C = 10 pF, f_{OSC} =16 MHz			2.5 (startup) 0.46 (stabilized)(3)	
g_m	Oscillator transconductance		3.5(3)			mA/V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabilized		1		ms

1. C=C_{L1}=C_{L2} is approximately equivalent to 2 x crystal C_{LOAD}.
2. The oscillator selection can be optimized in terms of supply current using a high quality resonator with small R_m value. Refer to crystal manufacturer for more details
3. Guaranteed by design.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 16 MHz oscillation. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

4. Guaranteed by design.

Figure 24. Typical HSI frequency vs. V_{DD}



Low speed internal RC oscillator (LSI)

In the following table, data are based on characterization results.

Table 34. LSI oscillator characteristics

Symbol	Parameter	Conditions(1)	Min.	Typ.	Max.	Unit
f_{LSI}	Frequency		26	38	56	kHz
$t_{su(LSI)}$	LSI oscillator wakeup time				200(2)	µs
$D_{(LSI)}$	LSI oscillator frequency drift(3)	0 °C ≤T_A ≤85 °C	-12		11	%

1. V_{DD} = 1.65 V to 3.6 V, T_A = -40 to 125 °C unless otherwise specified.
2. Guaranteed by design.
3. This is a deviation for an individual part, once the initial frequency has been measured.

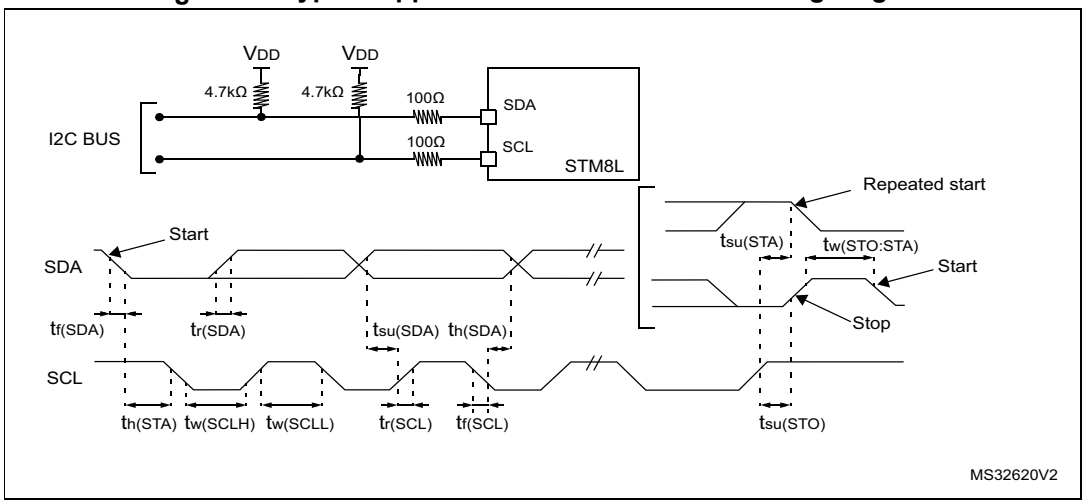
Flash memory

Table 36. Flash program and data EEPROM memory

Symbol	Parameter	Conditions	Min.	Typ.	Max. (1)	Unit
V_{DD}	Operating voltage (all modes, read/write/erase)	f_{SYSCLK} = 16 MHz	1.65		3.6	V
t_{prog}	Programming time for 1 or 128 bytes (block) erase/write cycles (on programmed byte)	-	-	6	-	ms
	Programming time for 1 to 128 bytes (block) write cycles (on erased byte)	-	-	3	-	
I_{prog}	Programming/ erasing consumption	T_A=+25 °C, V_{DD} = 3.0 V	-	0.7	-	mA
		T_A=+25 °C, V_{DD} = 1.8 V	-		-	
t_{RET} (2)	Data retention (program memory) after 10000 erase/write cycles at T_A=-40 to +85 °C (6 suffix)	T_{RET}=+85 °C	30(1)	-	-	years
	Data retention (program memory) after 10000 erase/write cycles at T_A=-40 to +125 °C (3 suffix)	T_{RET}=+125 °C	5(1)	-	-	
	Data retention (data memory) after 300000 erase/write cycles at T_A=-40 to +85 °C (6 suffix)	T_{RET}=+85 °C	30(1)	-	-	
	Data retention (data memory) after 300000 erase/write cycles at T_A=-40 to +125 °C (3 suffix)	T_{RET}=+125 °C	5(1)	-	-	
N_{RW} (3)	Erase/write cycles (program memory)	T_A=-40 to +85 °C (6 suffix), T_A=-40 to +105 °C (7 suffix) or T_A=-40 to +125 °C (3 suffix)	10(1)	-	-	kcycles
	Erase/write cycles (data memory)		300(1) (4)	-	-	

1. Data based on characterization results.
2. Conforming to JEDEC JESD22a117
3. The physical granularity of the memory is 4 bytes, so cycling is performed on 4 bytes even when a write/erase operation addresses a single byte.
4. Data based on characterization performed on the whole data memory.

Figure 42. Typical application with I²C bus and timing diagram



1. Measurement points are done at CMOS levels: 0.3 x V_{DD} and 0.7 x V_{DD}

9.3.13 12-bit DAC characteristics

In the following table, data are guaranteed by design.

Table 50. DAC characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DDA}	Analog supply voltage	-	1.8	-	3.6	V
V_{REF+}	Reference supply voltage	-	1.8	-	V_{DDA}	
I_{VREF}	Current consumption on V_{REF+} supply	V_{REF+} = 3.3 V, no load, middle code (0x800)	-	130	220	µA
		V_{REF+} = 3.3 V, no load, worst code (0x000)	-	220	350	
I_{VDDA}	Current consumption on V_{DDA} supply	V_{DDA} = 3.3 V, no load, middle code (0x800)	-	210	320	
		V_{DDA} = 3.3 V, no load, worst code (0x000)	-	320	520	
T_A	Temperature range		-40	-	125	°C
R_L (1) (2)	Resistive load	DACOUT buffer ON	5	-	-	kΩ
R_O	Output impedance	DACOUT buffer OFF	-	8	10	kΩ
C_L (3)	Capacitive load		-	-	50	pF
DAC_OUT (4)	DAC_OUT voltage	DACOUT buffer ON	0.2	-	V_{DDA} - 0.2	V
		DACOUT buffer OFF	0	-	V_{REF+} -1 LSB	V
$t_{settling}$	Settling time (full scale: for a 12-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches the final value ±1LSB)	$R_L \geq$ 5 kΩ, $C_L \leq$ 50 pF	-	7	12	µs
Update rate	Max frequency for a correct DAC_OUT (@95%) change when small variation of the input code (from code i to i+1LSB).	$R_L \geq$ 5 kΩ, $C_L \leq$ 50 pF	-	-	1	Msps
t_{WAKEUP}	Wakeup time from OFF state. Input code between lowest and highest possible codes.	$R_L \geq$ 5 kΩ, $C_L \leq$ 50 pF	-	9	15	µs
PSRR+	Power supply rejection ratio (to V_{DDA}) (static DC measurement)	$R_L \geq$ 5 kΩ, $C_L \leq$ 50 pF	-	-60	-35	dB

1. Resistive load between DACOUT and GNDA
2. Output on PF0 or PF1
3. Capacitive load at DACOUT pin
4. It gives the output excursion of the DAC

Table 53. ADC1 characteristics (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_S	Sampling time	V_{AIN} PF0/1/2/3 fast channels V_{DDA} < 2.4 V	0.43(3)(4)	-	-	µs
		V_{AIN} PF0/1/2/3 fast channels 2.4 V ≤V_{DDA}≤ 3.6 V	0.22(3)(4)	-	-	
		V_{AIN} on slow channels V_{DDA} < 2.4 V	0.86(3)(4)	-	-	
		V_{AIN} on slow channels 2.4 V ≤V_{DDA}≤ 3.6 V	0.41(3)(4)	-	-	
t_{conv}	12-bit conversion time	-	12 + t_S			$1/f_{ADC}$
		16 MHz	1(3)			µs
t_{WKUP}	Wakeup time from OFF state	-	-	-	3	µs
t_{IDLE}(5)	Time before a new conversion	-	-	-	∞	s
$t_{VREFINT}$	Internal reference voltage startup time	-	-	-	refer to *Table 46*	ms

1. The current consumption through V_{REF} is composed of two parameters:
   - one constant (max 300 µA)
   - one variable (max 400 µA), only during sampling time + 2 first conversion pulses.
   So, peak consumption is 300+400 = 700 µA and average consumption is 300 + [(4 sampling + 2) /16] x 400 = 450 µA at 1Msps
2. V_{REF-} must be tied to ground.
3. Minimum sampling and conversion time is reached for maximum R_{AIN}= 0.5 kΩ.
4. Value obtained for continuous conversion on fast channel.
5. The time between 2 conversions, or between ADC ON and the first conversion must be lower than t_{IDLE}.

9.3.15 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

Functional EMS (electromagnetic susceptibility)

Based on a simple running application on the product (toggling 2 LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electrostatic discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 61000 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 61000 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Prequalification trials:

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Table 58. EMS data

Symbol	Parameter	Conditions		Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{CPU}= 16 MHz, conforms to IEC 61000		2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{CPU} = 16 MHz, conforms to IEC 61000	Using HSI	4A
			Using HSE	2B

Table 67. WLCSP32 - 32-ball, 1.913 x 3.329 mm, 0.4 mm pitch wafer level chip scale package mechanical data(1)

Symbol	millimeters			inches(2)		
	Min	Typ	Max	Min	Typ	Max
A	0.525	0.555	0.585	0.0207	0.0219	0.0230
A1	-	0.175	-	-	0.0069	-
A2	-	0.380	-	-	0.0150	-
A3(3)	-	0.025	-	-	0.0010	-
b(4)	0.220	0.250	0.280	0.0087	0.0098	0.0110
D	1.878	1.913	1.948	0.0739	0.0753	0.0767
E	3.294	3.329	3.364	0.1297	0.1311	0.1324
e	-	0.400	-	-	0.0157	-
e1	-	1.200	-	-	0.0472	-
e2	-	2.800	-	-	0.1102	-
F	-	0.3565	-	-	0.0140	-
G	-	0.2645	-	-	0.0104	-
aaa	-	-	0.100	-	-	0.0039
bbb	-	-	0.100	-	-	0.0039
ccc	-	-	0.100	-	-	0.0039
ddd	-	-	0.050	-	-	0.0020
eee	-	-	0.050	-	-	0.0020

1. Preliminary data.
2. Values in inches are converted from mm and rounded to 4 decimal digits.
3. Back side coating.
4. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

Figure 61. WLCSP32 - 32-ball, 1.913 x 3.329 mm, 0.4 mm pitch wafer level chip scale package recommended footprint