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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, IR, POR, PWM, WDT
Number of I/O	54
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 28x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8l151r8t6

3.12 System configuration controller and routing interface

The system configuration controller provides the capability to remap some alternate functions on different I/O ports. TIM4 and ADC1 DMA channels can also be remapped.

The highly flexible routing interface allows application software to control the routing of different I/Os to the TIM1 timer input captures. It also controls the routing of internal analog signals to ADC1, COMP1, COMP2, DAC1 and the internal reference voltage V_{REFINT}. It also provides a set of registers for efficiently managing the charge transfer acquisition sequence (see *Section 3.13: Touch sensing*).

3.13 Touch sensing

The high-density and medium+ density STM8L15xx6/8 devices provide a simple solution for adding capacitive sensing functionality to any application. Capacitive sensing technology is able to detect finger presence near an electrode which is protected from direct touch by a dielectric (for example glass or plastic). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists of charging the electrode capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. In the high-density and medium+ density STM8L15xx6/8 devices, the acquisition sequence is managed by software and it involves analog I/O groups and the routing interface.

Reliable touch sensing solution can be quickly and easily implemented using the free STM8 touch sensing firmware library.

3.14 Timers

The high-density and medium+ density STM8L15xx6/8 devices contain one advanced control timer (TIM1), three 16-bit general purpose timers (TIM2,TIM3 and TIM5) and one 8-bit basic timer (TIM4).

All the timers can be served by DMA1.

Table 3 compares the features of the advanced control, general-purpose and basic timers.

Table 3. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA1 request generation	Capture/compare channels	Complementary outputs
TIM1	16-bit	up/down	Any integer from 1 to 65536	Yes	3 + 1	3
TIM2			Any power of 2 from 1 to 128		2	None
TIM3						
TIM5						
TIM4	8-bit	up	Any power of 2 from 1 to 32768		0	

It is clocked by the internal LSI RC clock source, and thus stays active even in case of a CPU clock failure.

3.16 Beeper

The beeper function outputs a signal on the BEEP pin for sound generation. The signal is in the range of 1, 2 or 4 kHz.

3.17 Communication interfaces

3.17.1 SPI

The serial peripheral interfaces (SPI1 and SPI2) provide half/ full duplex synchronous serial communication with external devices.

- Maximum speed: 8 Mbit/s ($f_{SYSCLK}/2$) both for master and slave
- Full duplex synchronous transfers
- Simplex synchronous transfers on 2 lines with a possible bidirectional data line
- Master or slave operation - selectable by hardware or software
- Hardware CRC calculation
- Slave/master selection input pin

Note: SPI1 and SPI2 can be served by the DMA1 Controller.

3.17.2 I^2C

The I^2C bus interface (I2C1) provides multi-master capability, and controls all I²C bus-specific sequencing, protocol, arbitration and timing.

- Master, slave and multi-master capability
- Standard mode up to 100 kHz and fast speed modes up to 400 kHz.
- 7-bit and 10-bit addressing modes.
- SMBus 2.0 and PMBus support
- Hardware CRC calculation

Note: I^2C1 can be served by the DMA1 Controller.

Table 5. High-density and medium+ density STM8L15x pin description (continued)

Pin number				Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP80	LQFP64	UFQFPN48 and LQFP48	WLCSP32				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
44	36	-	-	PB5/SPI1_SCK/ LCD_SEG15(3)/ADC1_IN13 / *[COMP1_INP]*	I/O	FT(6)	**X**	X	X	HS	X	X	**Port B5**	SPI1 clock / LCD segment 15 / ADC1_IN13/ *[Comparator 1 positive input]*
-	-	29	D1	PB5/SPI1_SCK/ LCD_SEG15(3)/ADC1_IN13 /DAC_OUT2/ *[COMP1_INP]*	I/O	FT(6)	**X**	X	X	HS	X	X	**Port B5**	[SPI1 clock] / LCD segment 15 / ADC1_IN13 / DAC channel 2 output/ *[Comparator 1 positive input]*
45	37	-	-	PB6/SPI1_MOSI/ LCD_SEG16(3)/ADC1_IN12 /*[COMP1_INP]*	I/O	FT(6)	**X**	X	X	HS	X	X	**Port B6**	SPI1 master out/slave in/ LCD segment 16 / ADC1_IN12/ *[Comparator 1 positive input]*
-	-	30	F1	PB6/SPI1_MOSI/ LCD_SEG16(3)/ADC1_IN12 /DAC_OUT2/*[COMP1_INP]*	I/O	FT(6)	**X**	X	X	HS	X	X	**Port B6**	SPI1 master out/ slave in / LCD segment 16 / ADC1_IN12 / DAC channel 2 output/*[Comparator 1 positive input]*
46	38	31	E1	PB7/SPI1_MISO/ LCD_SEG17(3)/ ADC1_IN11/*[COMP1_INP]*	I/O	FT(6)	**X**	X	X	HS	X	X	**Port B7**	SPI1 master in- slave out/ LCD segment 17 / ADC1_IN11/*[Comparator 1 positive input]*
65	53	37	B1	PC0/I2C1_SDA	I/O	FT(6)	**X**	-	X		T(7)		**Port C0**	I2C1 data
66	54	38	A1	PC1/I2C1_SCL	I/O	FT(6)	**X**	-	X		T(7)		**Port C1**	I2C1 clock
69	57	41	B2	PC2/USART1_RX/ LCD_SEG22/ADC1_IN6/ *[COMP1_INP]* /VREFINT	I/O	FT(6)	**X**	X	X	HS	X	X	**Port C2**	USART1 receive / LCD segment 22 / ADC1_IN6/ *[Comparator 1 positive input]* /Internal reference voltage output
-	-	42	A2	PC3/USART1_TX/ LCD_SEG23(3)/ ADC1_IN5	I/O	FT(6)	**X**	X	X	HS	X	X	**Port C3**	USART1 transmit / LCD segment 23 / ADC1_IN5

Table 5. High-density and medium+ density STM8L15x pin description (continued)

Pin number				Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP80	LQFP64	UFQFPN48 and LQFP48	WLCSP32				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
-	-	46	-(4)	PC7/LCD_SEG25(3)/ ADC1_IN3/USART3_CK/ *[COMP2_INM]* / *[COMP1_INP]* / *[LCD_COM5]*	I/O	FT(6)	**X**	X	X	HS	X	X	**Port C7**	LCD segment 25 /ADC1_IN3/ USART3 synchronous clock/ *[Comparator 2 negative input]* / *[Comparator 1 positive input]*/ *[LCD_COM5]*(3)
29	25	20	G3	PD0/TIM3_CH2/ *[ADC1_TRIG]*(2)/ LCD_SEG7(3)/ADC1_IN22/ *[COMP2_INP]*	I/O	FT(6)	**X**	X	X	HS	X	X	**Port D0**	Timer 3 - channel 2 / *[ADC1_Trigger]* / LCD segment 7 / ADC1_IN22 / *[Comparator 2 positive input]*
30	26	21	G2	PD1/TIM3_ETR/ LCD_COM3(3)/ADC1_IN21/ *[COMP1_INP]*// *[COMP2_INP]*	I/O	FT(6)	**X**	X	X	HS	X	X	**Port D1**	Timer 3 - trigger / LCD_COM3 / ADC1_IN21 / *[Comparator 1 positive input]* /*[Comparator 2 positive input]*
31	27	22	E4	PD2/TIM1_CH1 /LCD_SEG8(3)/ADC1_IN20/ *[COMP1_INP]*	I/O	FT(6)	**X**	X	X	HS	X	X	**Port D2**	Timer 1 - channel 1 / LCD segment 8 / ADC1_IN20/ *[Comparator 1 positive input]*
32	28	23	F3	PD3/ TIM1_ETR/ LCD_SEG9(3)/ ADC1_IN19/ *[COMP1_INP]*	I/O	FT(6)	**X**	X	X	HS	X	X	**Port D3**	Timer 1 - trigger / LCD segment 9 / ADC1_IN19/ *[Comparator 1 positive input]*
57	45	-	-	PD4/TIM1_CH2 /LCD_SEG18(3)/ ADC1_IN10/ *[COMP1_INP]*	I/O	FT(6)	**X**	X	X	HS	X	X	**Port D4**	Timer 1 - channel 2 / LCD segment 18 / ADC1_IN10/ *[Comparator 1 positive input]*
-	-	33	C1	PD4/TIM1_CH2 /LCD_SEG18(3)/ ADC1_IN10/SPI2_MISO/ *[COMP1_INP]*	I/O	FT(6)	**X**	X	X	HS	X	X	**Port D4**	Timer 1 - channel 2 / LCD segment 18 / ADC1_IN10/SPI2 master in/slave out/ *[Comparator 1 positive input]*

Table 8. I/O port hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 500F	Port D	PD_ODR	Port D data output latch register	0x00
0x00 5010		PD_IDR	Port D input pin value register	0xXX
0x00 5011		PD_DDR	Port D data direction register	0x00
0x00 5012		PD_CR1	Port D control register 1	0x00
0x00 5013		PD_CR2	Port D control register 2	0x00
0x00 5014	Port E	PE_ODR	Port E data output latch register	0x00
0x00 5015		PE_IDR	Port E input pin value register	0xXX
0x00 5016		PE_DDR	Port E data direction register	0x00
0x00 5017		PE_CR1	Port E control register 1	0x00
0x00 5018		PE_CR2	Port E control register 2	0x00
0x00 5019	Port F	PF_ODR	Port F data output latch register	0x00
0x00 501A		PF_IDR	Port F input pin value register	0xXX
0x00 501B		PF_DDR	Port F data direction register	0x00
0x00 501C		PF_CR1	Port F control register 1	0x00
0x00 501D		PF_CR2	Port F control register 2	0x00
0x00 501E	Port G	PG_ODR	Port F data output latch register	0x00
0x00 501F		PG_IDR	Port G input pin value register	0xXX
0x00 5020		PG_DDR	Port G data direction register	0x00
0x00 5021		PG_CR1	Port G control register 1	0x00
0x00 5022		PG_CR2	Port G control register 2	0x00
0x00 5023	Port H	PH_ODR	Port H data output latch register	0x00
0x00 5024		PH_IDR	Port H input pin value register	0xXX
0x00 5025		PH_DDR	Port H data direction register	0x00
0x00 5026		PH_CR1	Port H control register 1	0x00
0x00 5027		PH_CR2	Port H control register 2	0x00
0x00 5028	Port I	PI_ODR	Port I data output latch register	0x00
0x00 5029		PI_IDR	Port I input pin value register	0xXX
0x00 502A		PI_DDR	Port I data direction register	0x00
0x00 502B		PI_CR1	Port I control register 1	0x00
0x00 502C		PI_CR2	Port I control register 2	0x00

Table 9. General hardware register map

Address	Block	Register label	Register name	Reset status
0x00 502E to 0x00 5049	Reserved area (28 byte)			
0x00 5050	Flash	FLASH_CR1	Flash control register 1	0x00
0x00 5051		FLASH_CR2	Flash control register 2	0x00
0x00 5052		FLASH _PUKR	Flash program memory unprotection key register	0x00
0x00 5053		FLASH _DUKR	Data EEPROM unprotection key register	0x00
0x00 5054		FLASH _IAPSR	Flash in-application programming status register	0x00
0x00 5055 to 0x00 506F	Reserved area (27 byte)			
0x00 5070	DMA1	DMA1_GCSR	DMA1 global configuration & status register	0xFC
0x00 5071		DMA1_GIR1	DMA1 global interrupt register 1	0x00
0x00 5072 to 0x00 5074		Reserved area (3 byte)		
0x00 5075		DMA1_C0CR	DMA1 channel 0 configuration register	0x00
0x00 5076		DMA1_C0SPR	DMA1 channel 0 status & priority register	0x00
0x00 5077		DMA1_C0NDTR	DMA1 number of data to transfer register (channel 0)	0x00
0x00 5078		DMA1_C0PARH	DMA1 peripheral address high register (channel 0)	0x52
0x00 5079		DMA1_C0PARL	DMA1 peripheral address low register (channel 0)	0x00
0x00 507A		Reserved area (1 byte)		
0x00 507B		DMA1_C0M0ARH	DMA1 memory 0 address high register (channel 0)	0x00
0x00 507C		DMA1_C0M0ARL	DMA1 memory 0 address low register (channel 0)	0x00
0x00 507D to 0x00 507E		Reserved area (2 byte)		
0x00 507F		DMA1_C1CR	DMA1 channel 1 configuration register	0x00
0x00 5080		DMA1_C1SPR	DMA1 channel 1 status & priority register	0x00
0x00 5081		DMA1_C1NDTR	DMA1 number of data to transfer register (channel 1)	0x00
0x00 5082		DMA1_C1PARH	DMA1 peripheral address high register (channel 1)	0x52
0x00 5083	DMA1	DMA1_C1PARL	DMA1 peripheral address low register (channel 1)	0x00

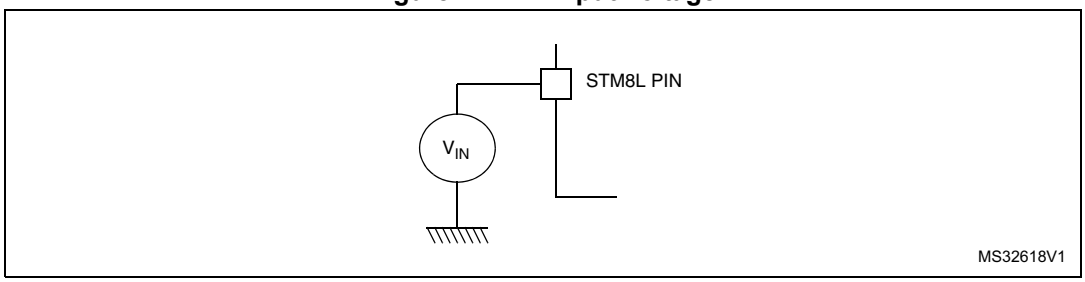
Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 53AC	DAC	DAC_DORH	DAC data output register high	0x00
0x00 53AD		DAC_DORL	DAC data output register low	0x00
0x00 53A2		DAC_DCH2RDHRH	DAC channel 2 right aligned data holding register high	0x00
0x00 53A3		DAC_DCH2RDHRL	DAC channel 2 right aligned data holding register low	0x00
0x00 53A4		DAC_DCH1LDHRH	DAC channel 1left aligned data holding register high	0x00
0x00 53A5		DAC_DCH1LDHRL	DAC channel 1left aligned data holding register low	0x00
0x00 53A6		DAC_DCH2LDHRH	DAC channel 2 left aligned data holding register high	0x00
0x00 53A7		DAC_DCH2LDHRL	DAC channel 2 left aligned data holding register low	0x00
0x00 53A8		DAC_DCH1DHR8	DAC channel 1 8-bit mode data holding register	0x00
0x00 53A9		DAC_DCH2DHR8	DAC channel 2 8-bit mode data holding register	0x00
0x00 53AA to 0x00 53AB	Reserved area (2 byte)			
0x00 53AC	DAC	DAC_CH1DORH Reset value	DAC channel 1 data output register high	0x00
0x00 53AD		DAC_CH1DORL Reset value	DAC channel 1 data output register low	0x00
0x00 53AE to 0x00 53AF	Reserved area (2 byte)			
0x00 53B0	DAC	DAC_CH2DORH Reset value	DAC channel 2 data output register high	0x00
0x00 53B1		DAC_CH2DORL Reset value	DAC channel 2 data output register low	0x00
0x00 53B2 to 0x00 53BF	Reserved area			
0x00 53C0	SPI2	SPI2_CR1	SPI2 control register 1	0x00
0x00 53C1		SPI2_CR2	SPI2 control register 2	0x00
0x00 53C2		SPI2_ICR	SPI2 interrupt control register	0x00
0x00 53C3		SPI2_SR	SPI2 status register	0x02
0x00 53C4		SPI2_DR	SPI2 data register	0x00
0x00 53C5		SPI2_CRCPR	SPI2 CRC polynomial register	0x07
0x00 53C6		SPI2_RXCRCR	SPI2 Rx CRC register	0x00
0x00 53C7		SPI2_TXCRCR	SPI2 Tx CRC register	0x00

9.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 12*.

Figure 12. Pin input voltage



9.2 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Device mission profile(application conditions)is compliant with JEDEC JESD47 Qualification Standard. Extended mission profiles are available on demand.

Table 15. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD}- V_{SS}	External supply voltage (including V_{DDA})(1)	- 0.3	4.0	V
V_{IN}(2)	Input voltage on true open-drain pins (PC0 and PC1)	V_{SS} - 0.3	V_{DD} + 4.0	
	Input voltage on five-volt tolerant (FT) pins	V_{SS} - 0.3	V_{DD} + 4.0	
	Input voltage on any other pin	V_{SS} - 0.3	4.0	
V_{ESD}	Electrostatic discharge voltage	see *Absolute maximum ratings (electrical sensitivity) on page 122*		

1. All power (V_{DD1}, V_{DD2}, V_{DD3}, V_{DD4}, V_{DDA}) and ground (V_{SS1}, V_{SS2}, V_{SS3}, V_{SS4}, V_{SSA}) pins must always be connected to the external power supply.
2. V_{IN} maximum must always be respected. Refer to *Table 16.* for maximum allowed injected current values.

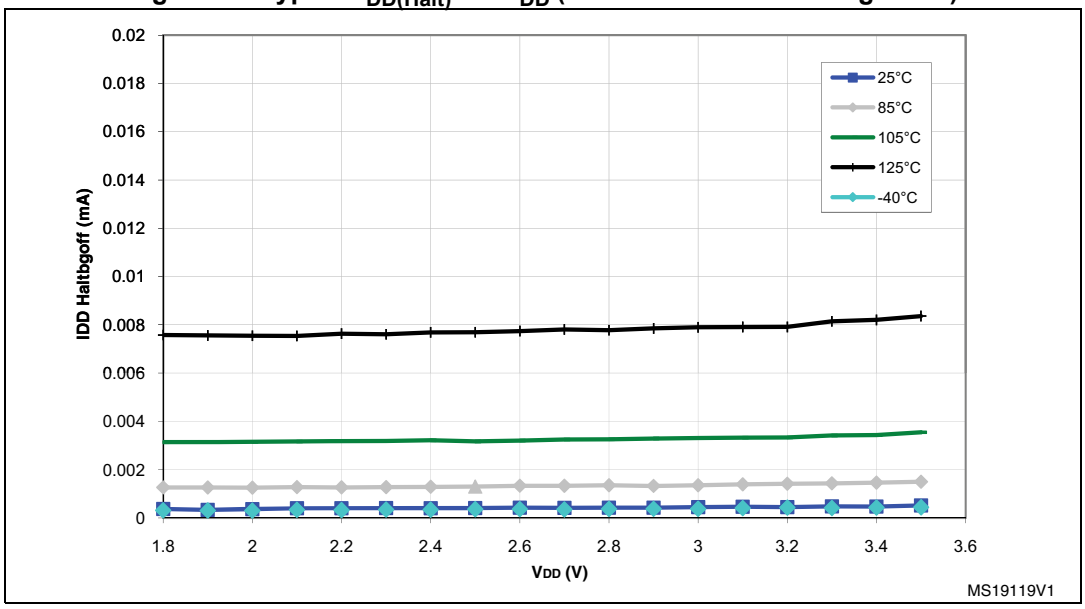
In the following table, data are based on characterization results, unless otherwise specified.

Table 26. Total current consumption and timing in Halt mode at V_{DD} = 1.65 to 3.6 V

Symbol	Parameter	Condition(1)	Typ.	Max.	Unit
$I_{DD(Halt)}$	Supply current in Halt mode (Ultra-low-power ULP bit =1 in the PWR_CSR2 register)	T_A = -40 °C to 25 °C	400	1600(2)	nA
		T_A = 55 °C	810	2400	
		T_A = 85 °C	1600	4500(2)	
		T_A = 105 °C	2900	7700(2)	
		T_A = 125 °C	5.6	18(2)	µA
$I_{DD(WUHalt)}$	Supply current during wakeup time from Halt mode (using HSI)		2.4		mA
$t_{WU\_HSI(Halt)}$(3)(4)	Wakeup time from Halt to Run mode (using HSI)		4.7	7	µs
$t_{WU\_LSI(Halt)}$(3)(4)	Wakeup time from Halt mode to Run mode (using LSI)		150		µs

1. T_A = -40 to 125 °C, no floating I/O, unless otherwise specified
2. Tested in production
3. ULP=0 or ULP=1 and FWU=1 in the PWR_CSR2 register
4. Wakeup time until start of interrupt vector fetch.
   The first word of interrupt routine is fetched 4 CPU cycles after t_{WU}

Figure 21. Typical $I_{DD(Halt)}$ vs. V_{DD} (internal reference voltage OFF)



Current consumption of on-chip peripherals

Table 27. Peripheral current consumption

Symbol	Parameter		Typ. V_{DD} = 3.0 V	Unit
$I_{DD(TIM1)}$	TIM1 supply current(1)		10	µA/MHz
$I_{DD(TIM2)}$	TIM2 supply current (1)		7	
$I_{DD(TIM3)}$	TIM3 supply current (1)		7	
$I_{DD(TIM5)}$	TIM5 supply current (1)		7	
$I_{DD(TIM4)}$	TIM4 timer supply current (1)		3	
$I_{DD(USART1)}$	USART1 supply current (2)		5	
$I_{DD(USART2)}$	USART2 supply current (2)		5	
$I_{DD(USART3)}$	USART3 supply current (2)		5	
$I_{DD(SPI1)}$	SPI1 supply current (2)		3	
$I_{DD(SPI2)}$	SPI2 supply current (2)		3	
$I_{DD(I2C1)}$	I^2C1 supply current (2)		4	
$I_{DD(DMA1)}$	DMA1 supply current(2)		3	
$I_{DD(WWDG)}$	WWDG supply current(2)		1	
$I_{DD(ALL)}$	Peripherals ON(3)		63	
$I_{DD(ADC1)}$	ADC1 supply current(4)		1500	µA
$I_{DD(DAC)}$	DAC supply current(5)		370	
$I_{DD(COMP1)}$	Comparator 1 supply current(6)		0.160	
$I_{DD(COMP2)}$	Comparator 2 supply current(6)	Slow mode	2	
		Fast mode	5	
$I_{DD(PVD/BOR)}$	Power voltage detector and brownout Reset unit supply current (7)		2.6	
$I_{DD(BOR)}$	Brownout Reset unit supply current (7)		2.4	
$I_{DD(IDWDG)}$	Independent watchdog supply current	including LSI supply current	0.45	
		excluding LSI supply current	0.05	

1. Data based on a differential I_{DD} measurement between all peripherals OFF and a timer counter running at 16 MHz. The CPU is in Wait mode in both cases. No IC/OC programmed, no I/O pins toggling. Not tested in production.
2. Data based on a differential I_{DD} measurement between the on-chip peripheral in reset configuration and not clocked and the on-chip peripheral when clocked and not kept under reset. The CPU is in Wait mode in both cases. No I/O pins toggling. Not tested in production.
3. Peripherals listed above the $I_{DD(ALL)}$ parameter ON: TIM1, TIM2, TIM3, TIM4, TIM5, USART1, USART2, USART3, SPI1, SPI2, I2C1, DMA1, WWDG.
4. Data based on a differential I_{DD} measurement between ADC in reset configuration and continuous ADC conversion.

5. Data based on a differential I_{DD} measurement between DAC in reset configuration and continuous DAC conversion of V_{DD} /2. Floating DAC output.
6. Data based on a differential I_{DD} measurement between COMP1 or COMP2 in reset configuration and COMP1 or COMP2 enabled with static inputs. Supply current of internal reference voltage excluded.
7. Including supply current of internal reference voltage.

Table 28. Current consumption under external reset

Symbol	Parameter	Conditions		Typ.	Unit
$I_{DD(RST)}$	Supply current under external reset (1)	PB1/PB3/PA5 pins are externally tied to V_{DD}	V_{DD} = 1.8 V	48	µA
			V_{DD} = 3 V	80	
			V_{DD} = 3.6 V	95	

1. All pins except PA0, PB0 and PB4 are floating under reset. PA0, PB0 and PB4 are configured with pull-up under reset. PB1, PB3 and PA5 must be tied externally under reset to avoid the consumption due to their schmitt trigger.

9.3.4 Clock and timing characteristics

HSE external clock (HSEBYP = 1 in CLK_ECKCR)

Subject to general operating conditions for V_{DD} and T_A.

Table 29. HSE external clock characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{HSE_ext} (1)	External clock source frequency		1		16	MHz
V_{HSEH}	OSC_IN input pin high level voltage		0.7 x V_{DD}		V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}		0.3 x V_{DD}	
$C_{in(HSE)}$ (1)	OSC_IN input capacitance			2.6		pF
I_{LEAK_HSE}	OSC_IN input leakage current	$V_{SS} < V_{IN} < V_{DD}$			±1	µA

1. Guaranteed by design.

Flash memory

Table 36. Flash program and data EEPROM memory

Symbol	Parameter	Conditions	Min.	Typ.	Max. (1)	Unit
V_{DD}	Operating voltage (all modes, read/write/erase)	f_{SYSCLK} = 16 MHz	1.65		3.6	V
t_{prog}	Programming time for 1 or 128 bytes (block) erase/write cycles (on programmed byte)	-	-	6	-	ms
	Programming time for 1 to 128 bytes (block) write cycles (on erased byte)	-	-	3	-	
I_{prog}	Programming/ erasing consumption	T_A=+25 °C, V_{DD} = 3.0 V	-	0.7	-	mA
		T_A=+25 °C, V_{DD} = 1.8 V	-		-	
t_{RET} (2)	Data retention (program memory) after 10000 erase/write cycles at T_A=-40 to +85 °C (6 suffix)	T_{RET}=+85 °C	30(1)	-	-	years
	Data retention (program memory) after 10000 erase/write cycles at T_A=-40 to +125 °C (3 suffix)	T_{RET}=+125 °C	5(1)	-	-	
	Data retention (data memory) after 300000 erase/write cycles at T_A=-40 to +85 °C (6 suffix)	T_{RET}=+85 °C	30(1)	-	-	
	Data retention (data memory) after 300000 erase/write cycles at T_A=-40 to +125 °C (3 suffix)	T_{RET}=+125 °C	5(1)	-	-	
N_{RW} (3)	Erase/write cycles (program memory)	T_A=-40 to +85 °C (6 suffix), T_A=-40 to +105 °C (7 suffix) or T_A=-40 to +125 °C (3 suffix)	10(1)	-	-	kcycles
	Erase/write cycles (data memory)		300(1) (4)	-	-	

1. Data based on characterization results.
2. Conforming to JEDEC JESD22a117
3. The physical granularity of the memory is 4 bytes, so cycling is performed on 4 bytes even when a write/erase operation addresses a single byte.
4. Data based on characterization performed on the whole data memory.

Figure 26. Typical V_{IL} and V_{IH} vs. V_{DD} (standard I/Os)

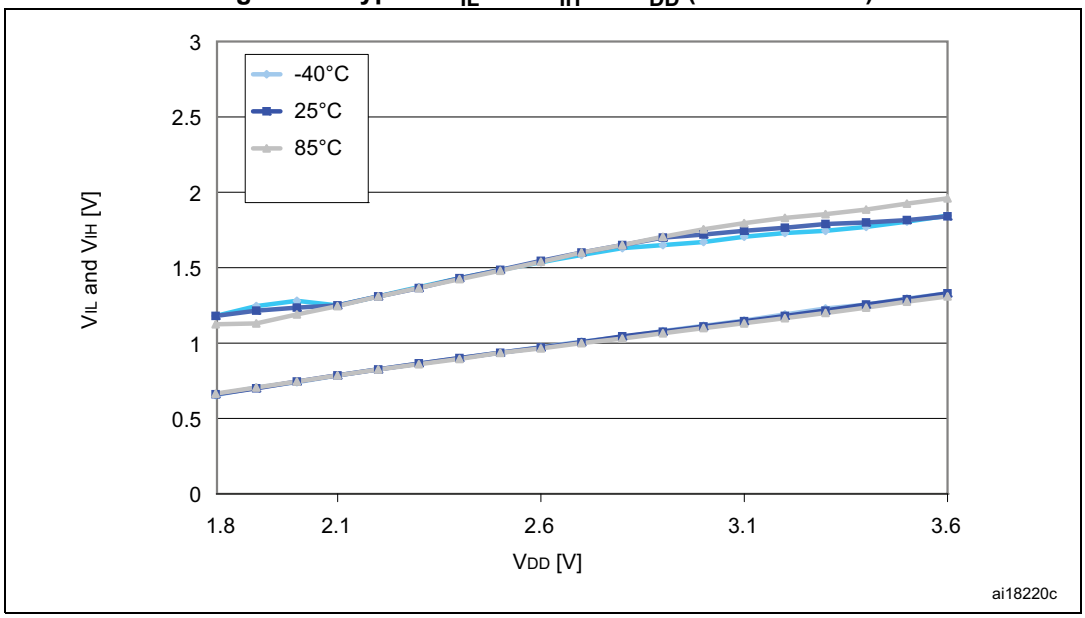


Figure 27. Typical V_{IL} and V_{IH} vs. V_{DD} (true open drain I/Os)

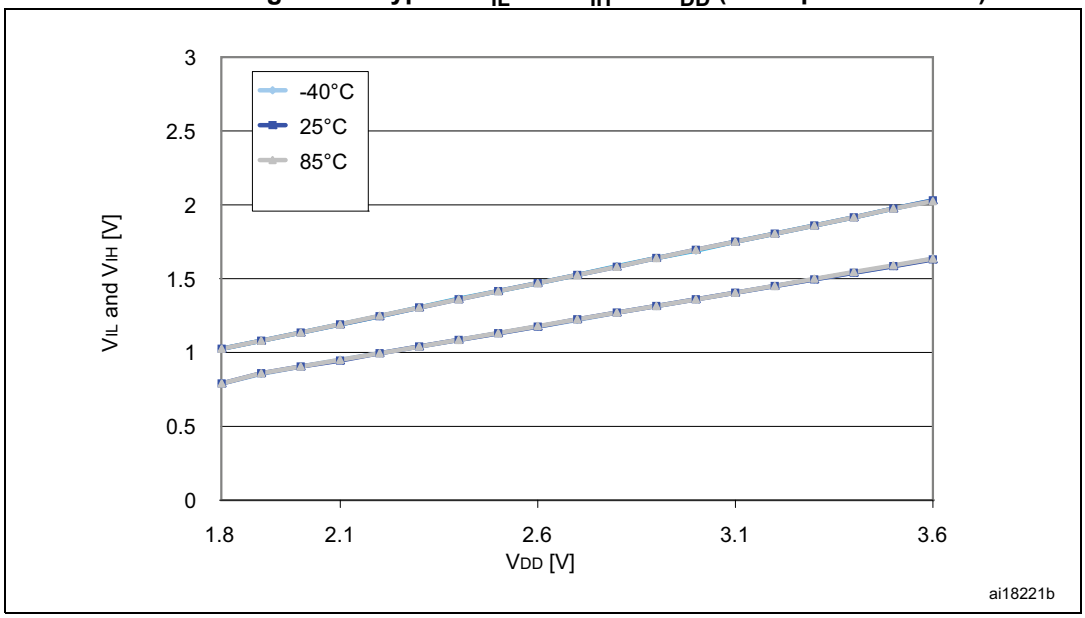


Figure 28. Typical pull-up resistance R_{PU} vs. V_{DD} with $V_{IN}=V_{SS}$

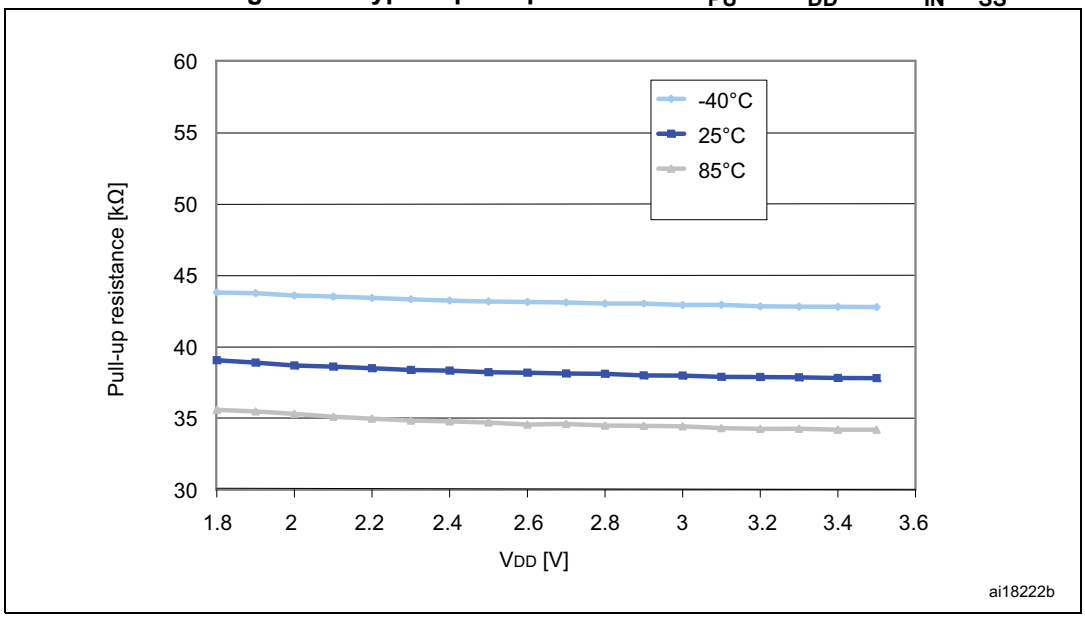
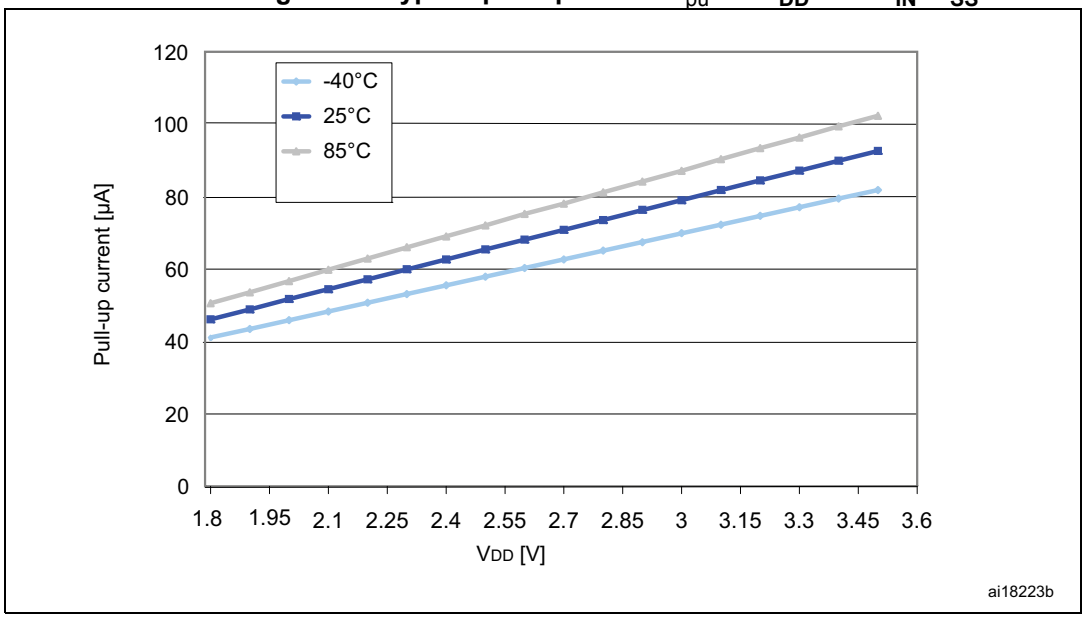


Figure 29. Typical pull-up current I_{pu} vs. V_{DD} with $V_{IN}=V_{SS}$



Output driving current

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Figure 30. Typical V_{OL} @ V_{DD} = 3.0 V (high sink ports)

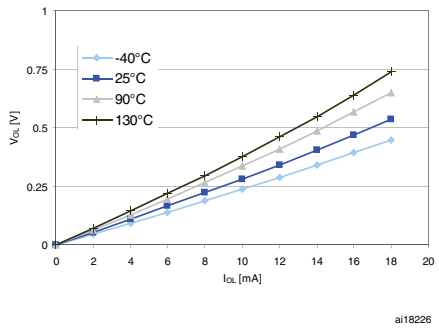


Figure 31. Typical V_{OL} @ V_{DD} = 1.8 V (high sink ports)

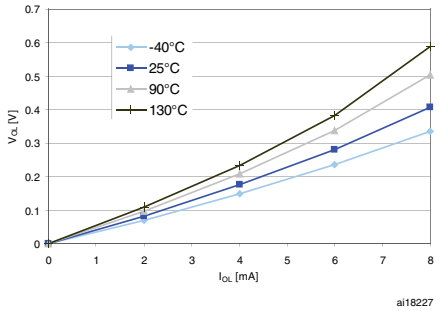


Figure 32. Typical V_{OL} @ V_{DD} = 3.0 V (true open drain ports)

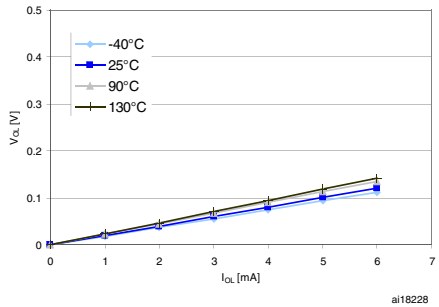


Figure 33. Typical V_{OL} @ V_{DD} = 1.8 V (true open drain ports)

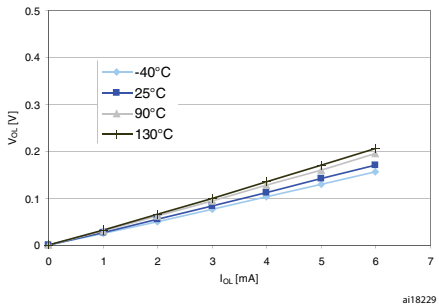


Figure 34. Typical V_{DD} - V_{OH} @ V_{DD} = 3.0 V (high sink ports)

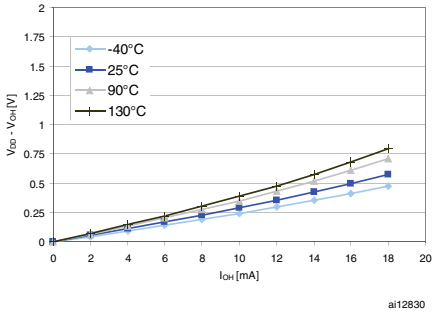
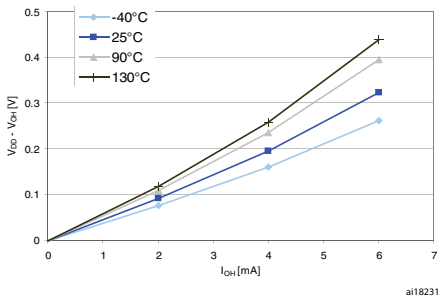


Figure 35. Typical V_{DD} - V_{OH} @ V_{DD} = 1.8 V (high sink ports)



NRST pin

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 42. $\overline{\text{NRST}}$ pin characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{IL(NRST)}$	NRST input low level voltage (1)	-	V_{SS}	-	0.8	V
$V_{IH(NRST)}$	NRST input high level voltage (1)	-	1.4	-	V_{DD}	
$V_{OL(NRST)}$	NRST output low level voltage (1)	I_{OL} = 2 mA 2.7 V ≤V_{DD} ≤3.6 V	-	-	0.4	
		I_{OL} = 1.5 mA V_{DD} < 2.7 V	-	-		
V_{HYST}	NRST input hysteresis(3)	-	10%V_{DD}(2)	-	-	mV
$R_{PU(NRST)}$	NRST pull-up equivalent resistor(1)	-	30	45	60	kΩ
$V_{F(NRST)}$	NRST input filtered pulse (3)	-		-	50	ns
$V_{NF(NRST)}$	NRST input not filtered pulse (3)	-	300	-	-	

1. Data based on characterization results.
2. 200 mV min.
3. Data guaranteed by design.

Figure 36. Typical NRST pull-up resistance R_{PU} vs. V_{DD}

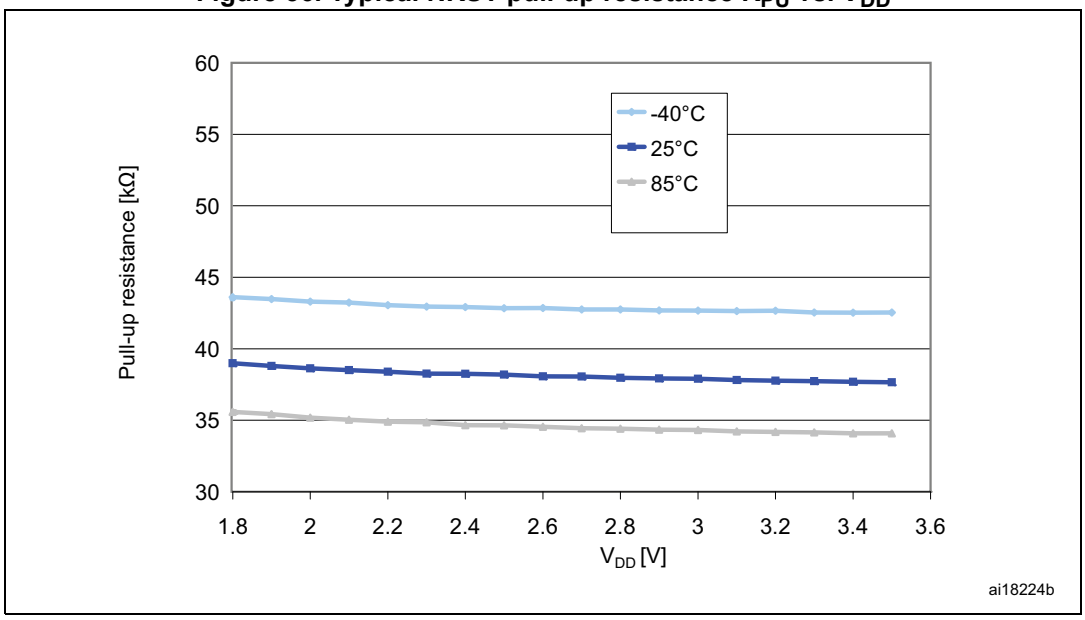
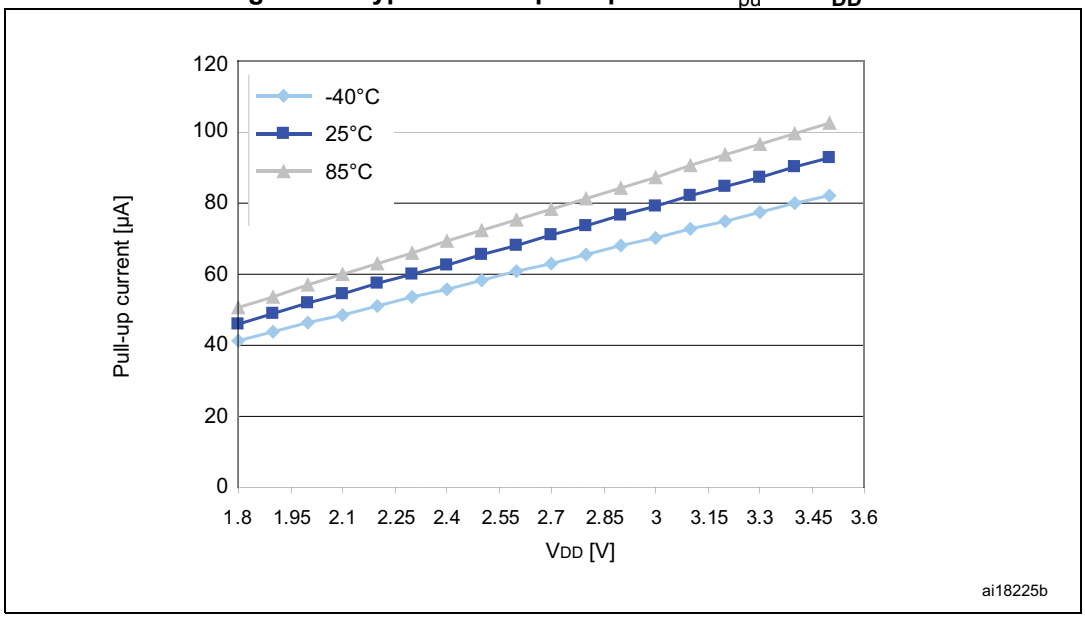
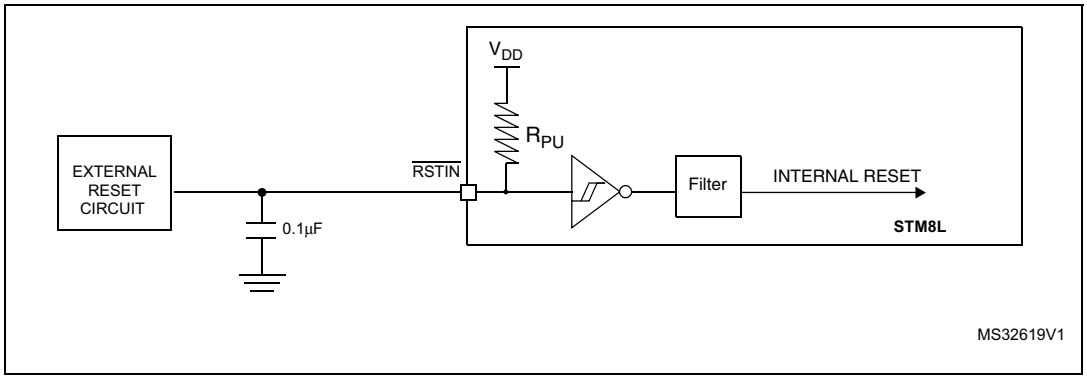


Figure 37. Typical NRST pull-up current I_{pu} vs. V_{DD}



The reset network shown in *Figure 38* protects the device against parasitic resets. The user must ensure that the level on the NRST pin can go below the V_{IL} max. level specified in *Table 42*. Otherwise the reset is not taken into account internally. For power consumption-sensitive applications, the capacity of the external reset capacitor can be reduced to limit the charge/discharge current. If the NRST signal is used to reset the external circuitry, the user must pay attention to the charge/discharge time of the external capacitor to meet the reset timing conditions of the external devices. The minimum recommended capacity is 10 nF.

Figure 38. Recommended NRST pin configuration



9.3.9 LCD controller (STM8L152x6/8 only)

In the following table, data are guaranteed by design.

Table 45. LCD characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{LCD}	LCD external voltage	-		3.6	V
V_{LCD0}	LCD internal reference voltage 0	-	2.6	-	
V_{LCD1}	LCD internal reference voltage 1	-	2.7	-	
V_{LCD2}	LCD internal reference voltage 2	-	2.8	-	
V_{LCD3}	LCD internal reference voltage 3	-	3.0	-	
V_{LCD4}	LCD internal reference voltage 4	-	3.1	-	
V_{LCD5}	LCD internal reference voltage 5	-	3.2	-	
V_{LCD6}	LCD internal reference voltage 6	-	3.4	-	
V_{LCD7}	LCD internal reference voltage 7	-	3.5	-	
C_{EXT}	V_{LCD} external capacitance	0.1	1	2	µF
I_{DD}	Supply current(1) at V_{DD} = 1.8 V	-	3	-	µA
	Supply current(1) at V_{DD} = 3 V	-	3	-	
R_{HN}(2)	High value resistive network (low drive)	-	6.6	-	MΩ
R_{LN}(3)	Low value resistive network (high drive)	-	240	-	kΩ
V_{33}	Segment/Common higher level voltage	-		V_{LCDx}	V
V_{34}	Segment/Common 3/4 level voltage	-	$3/4V_{LCDx}$	-	
V_{23}	Segment/Common 2/3 level voltage	-	$2/3V_{LCDx}$	-	
V_{12}	Segment/Common 1/2 level voltage	-	$1/2V_{LCDx}$	-	
V_{13}	Segment/Common 1/3 level voltage	-	$1/3V_{LCDx}$	-	
V_{14}	Segment/Common 1/4 level voltage	-	$1/4V_{LCDx}$	-	
V_0	Segment/Common lowest level voltage	0	-	-	

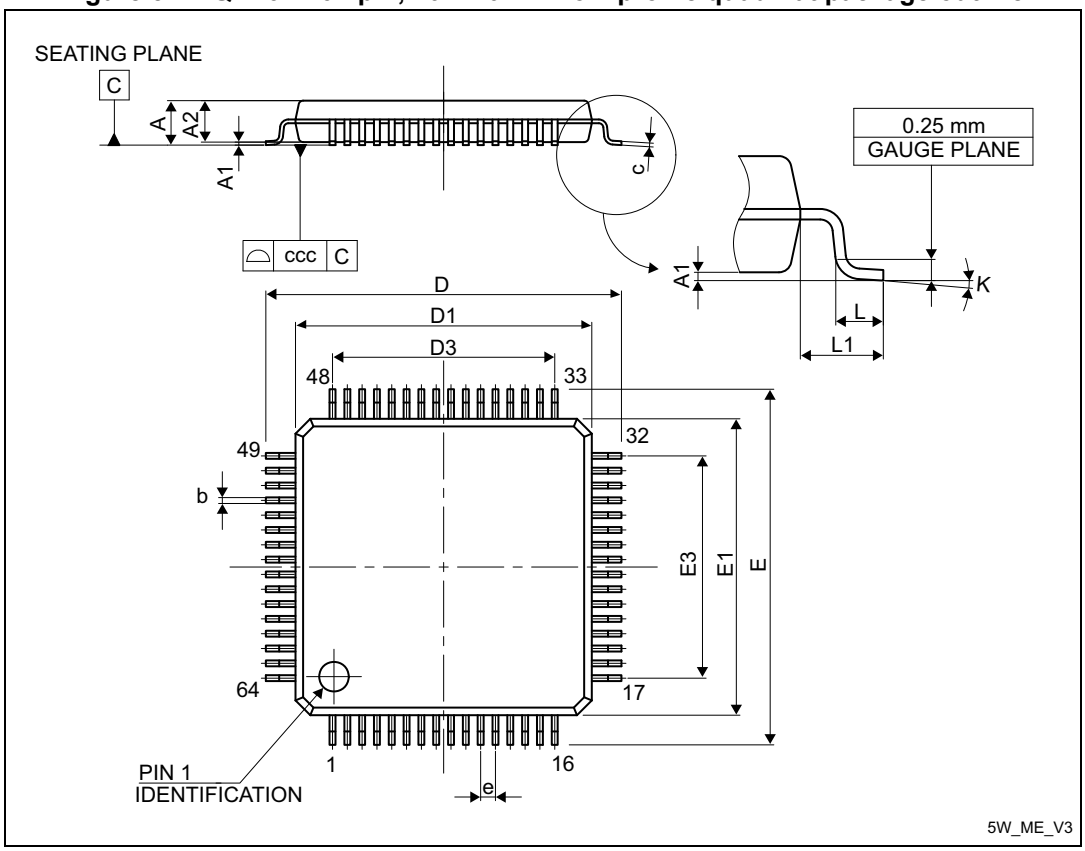
1. LCD enabled with 3 V internal booster (LCD_CR1 = 0x08), 1/4 duty, 1/3 bias, division ratio= 64, all pixels active, no LCD connected.
2. R_{HN} is the total high value resistive network.
3. R_{LN} is the total low value resistive network.

VLCD external capacitor (STM8L152x6/8 only)

The application can achieve a stabilized LCD reference voltage by connecting an external capacitor C_{EXT} to the V_{LCD} pin. C_{EXT} is specified in *Table 45*.

10.2 LQFP64 package information

Figure 51. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 64. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data

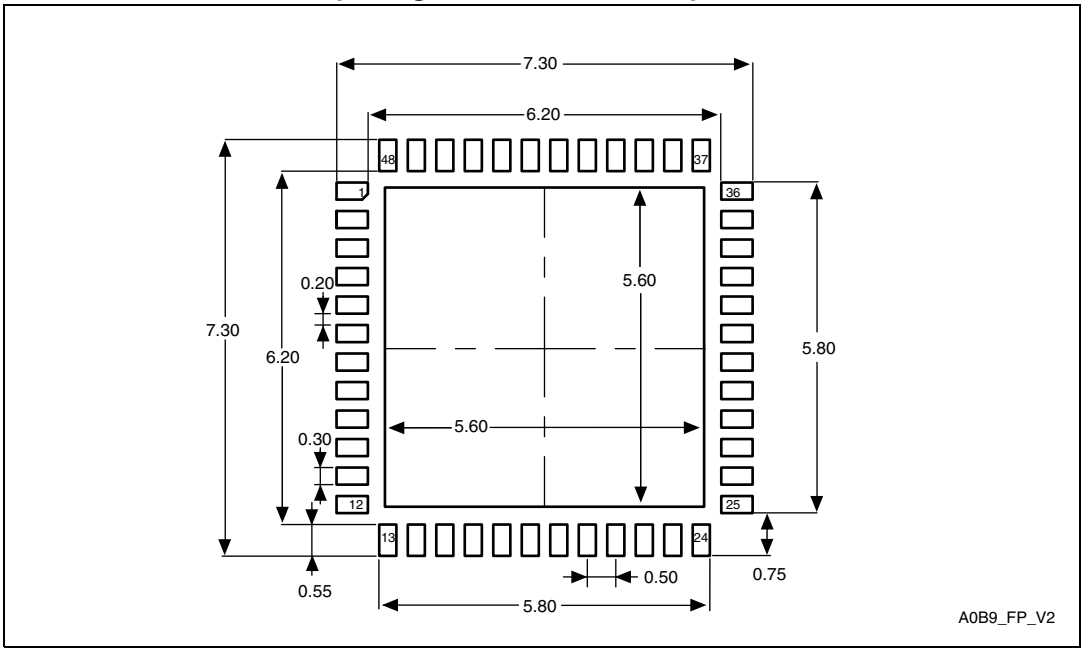
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-

Table 66. UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
D	6.900	7.000	7.100	0.2717	0.2756	0.2795
E	6.900	7.000	7.100	0.2717	0.2756	0.2795
D2	5.500	5.600	5.700	0.2165	0.2205	0.2244
E2	5.500	5.600	5.700	0.2165	0.2205	0.2244
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 58. UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package recommended footprint



1. Dimensions are expressed in millimeters.