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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, IR, POR, PWM, WDT
Number of I/O	54
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 28x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8l151r8t6tr

3.6 LCD (Liquid crystal display)

The LCD is only available on STM8L152x6/8 devices.

The liquid crystal display drives up to 8 common terminals and up to 40 segment terminals to drive up to 320 pixels. It can also be configured to drive up to 4 common and 44 segments (up to 176 pixels).

- Internal step-up converter to guarantee contrast control whatever V_{DD}.
- Static 1/2, 1/3, 1/4, 1/8 duty supported.
- Static 1/2, 1/3, 1/4 bias supported.
- Phase inversion to reduce power consumption and EMI.
- Up to 8 pixels which can programmed to blink.
- The LCD controller can operate in Halt mode.

Note: Unnecessary segments and common pins can be used as general I/O pins.

3.7 Memories

The high-density and medium+ density STM8L15xx6/8 devices have the following main features:

- Up to 4 Kbyte of RAM
- The non-volatile memory is divided into three arrays:
  - Up to 64 Kbyte of medium-density embedded Flash program memory
  - Up to 2 Kbyte of Data EEPROM
  - Option bytes.

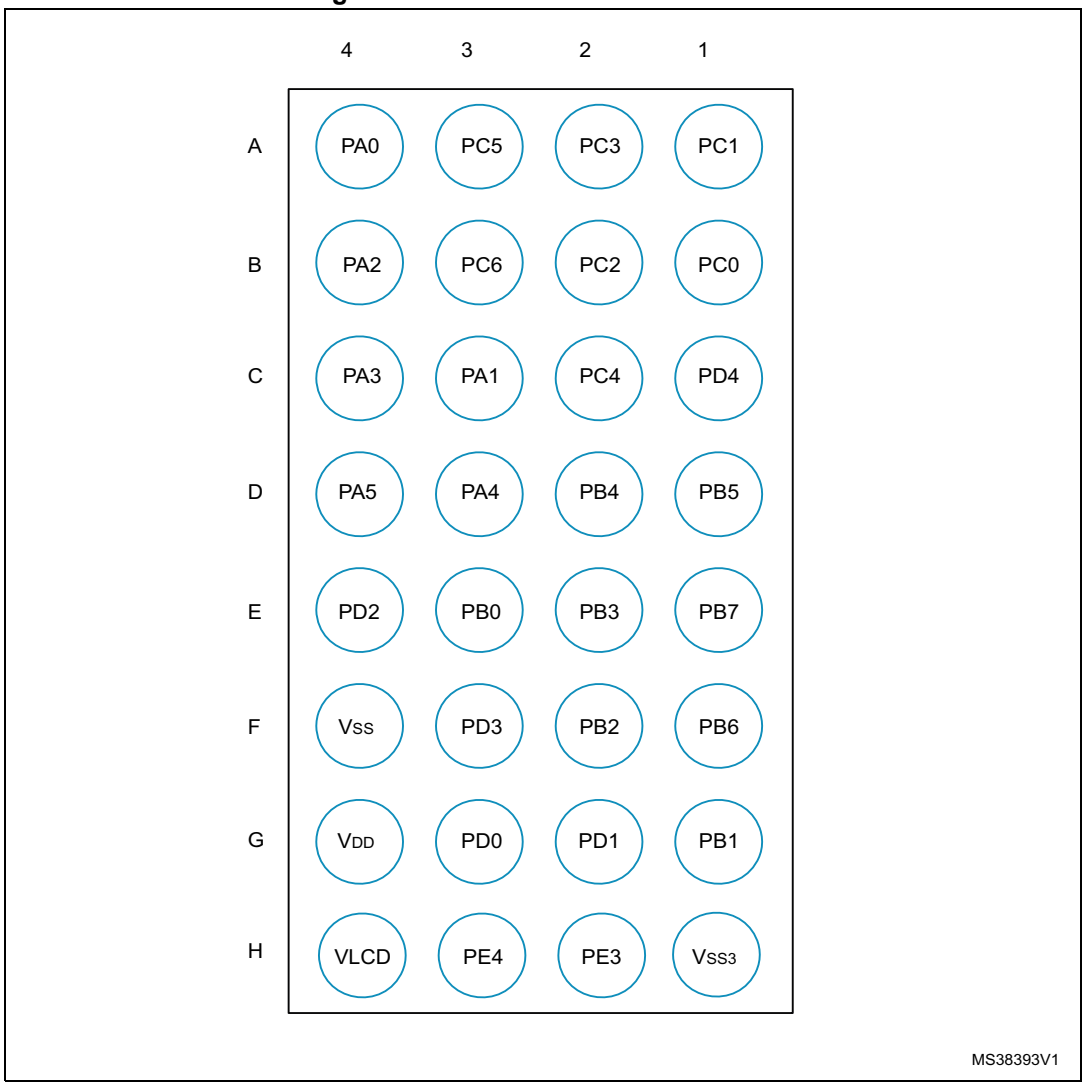
The EEPROM embeds the error correction code (ECC) feature. It supports the read-while-write (RWW): it is possible to execute the code from the program matrix while programming/erasing the data matrix.

The option byte protects part of the Flash program memory from write and readout piracy.

3.8 DMA

A 4-channel direct memory access controller (DMA1) offers a memory-to-memory and peripherals-from/to-memory transfer capability. The 4 channels are shared between the following IPs with DMA capability: ADC1, DAC1,DAC2, I2C1, SPI1, SPI2, USART1, USART2, USART3, and the 5 Timers.

Figure 9. STM8L152K8 32-ball ballout



Warning: **For the 32-pin STM8L152K8 devices, some active I/O pins are not bonded out of the package. Effectively, all ports available on 48-pin devices must be considered as active ports also for 32-pin devices - see *Table 5: High-density and medium+ density STM8L15x pin description* for more details. To avoid spurious effects, users have to configure active ports as input pull-up. A small increase in consumption (typ. < 300 µA) may occur during the power up and reset phase until these ports are properly configured.**

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5084	Reserved area (1 byte)			
0x00 5085	DMA1	DMA1_C1M0ARH	DMA1 memory 0 address high register (channel 1)	0x00
0x00 5086		DMA1_C1M0ARL	DMA1 memory 0 address low register (channel 1)	0x00
0x00 5087 0x00 5088	Reserved area (2 byte)			
0x00 5089	DMA1	DMA1_C2CR	DMA1 channel 2 configuration register	0x00
0x00 508A		DMA1_C2SPR	DMA1 channel 2 status & priority register	0x00
0x00 508B		DMA1_C2NDTR	DMA1 number of data to transfer register (channel 2)	0x00
0x00 508C		DMA1_C2PARH	DMA1 peripheral address high register (channel 2)	0x52
0x00 508D		DMA1_C2PARL	DMA1 peripheral address low register (channel 2)	0x00
0x00 508E	Reserved area (1 byte)			
0x00 508F		DMA1_C2M0ARH	DMA1 memory 0 address high register (channel 2)	0x00
0x00 5090		DMA1_C2M0ARL	DMA1 memory 0 address low register (channel 2)	0x00
0x00 5091 0x00 5092	Reserved area (2 byte)			
0x00 5093	DMA1	DMA1_C3CR	DMA1 channel 3 configuration register	0x00
0x00 5094		DMA1_C3SPR	DMA1 channel 3 status & priority register	0x00
0x00 5095		DMA1_C3NDTR	DMA1 number of data to transfer register (channel 3)	0x00
0x00 5096		DMA1_C3PARH_ C3M1ARH	DMA1 peripheral address high register (channel 3)	0x40
0x00 5097		DMA1_C3PARL_ C3M1ARL	DMA1 peripheral address low register (channel 3)	0x00
0x00 5098		DMA_C3M0EAR	DMA channel 3 memory 0 extended address register	0x00
0x00 5099		DMA1_C3M0ARH	DMA1 memory 0 address high register (channel 3)	0x00
0x00 509A		DMA1_C3M0ARL	DMA1 memory 0 address low register (channel 3)	0x00
0x00 509B to 0x00 509C	Reserved area (3 byte)			

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5262	TIM2	TIM2_CCR1L	TIM2 capture/compare register 1 low	0x00
0x00 5263		TIM2_CCR2H	TIM2 capture/compare register 2 high	0x00
0x00 5264		TIM2_CCR2L	TIM2 capture/compare register 2 low	0x00
0x00 5265		TIM2_BKR	TIM2 break register	0x00
0x00 5266		TIM2_OISR	TIM2 output idle state register	0x00
0x00 5267 to 0x00 527F	Reserved area (25 byte)			
0x00 5280	TIM3	TIM3_CR1	TIM3 control register 1	0x00
0x00 5281		TIM3_CR2	TIM3 control register 2	0x00
0x00 5282		TIM3_SMCR	TIM3 Slave mode control register	0x00
0x00 5283		TIM3_ETR	TIM3 external trigger register	0x00
0x00 5284		TIM3_DER	TIM3 DMA1 request enable register	0x00
0x00 5285		TIM3_IER	TIM3 interrupt enable register	0x00
0x00 5286		TIM3_SR1	TIM3 status register 1	0x00
0x00 5287		TIM3_SR2	TIM3 status register 2	0x00
0x00 5288		TIM3_EGR	TIM3 event generation register	0x00
0x00 5289		TIM3_CCMR1	TIM3 Capture/Compare mode register 1	0x00
0x00 528A		TIM3_CCMR2	TIM3 Capture/Compare mode register 2	0x00
0x00 528B		TIM3_CCER1	TIM3 Capture/Compare enable register 1	0x00
0x00 528C		TIM3_CNTRH	TIM3 counter high	0x00
0x00 528D		TIM3_CNTRL	TIM3 counter low	0x00
0x00 528E		TIM3_PSCR	TIM3 prescaler register	0x00
0x00 528F		TIM3_ARRH	TIM3 Auto-reload register high	0xFF
0x00 5290		TIM3_ARRL	TIM3 Auto-reload register low	0xFF
0x00 5291		TIM3_CCR1H	TIM3 Capture/Compare register 1 high	0x00
0x00 5292		TIM3_CCR1L	TIM3 Capture/Compare register 1 low	0x00
0x00 5293		TIM3_CCR2H	TIM3 Capture/Compare register 2 high	0x00
0x00 5294		TIM3_CCR2L	TIM3 Capture/Compare register 2 low	0x00
0x00 5295		TIM3_BKR	TIM3 break register	0x00
0x00 5296		TIM3_OISR	TIM3 output idle state register	0x00
0x00 5297 to 0x00 52AF	Reserved area (25 byte)			

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 53C8 to 0x00 53DF	Reserved area			
0x00 53E0	USART2	USART2_SR	USART2 status register	0xC0
0x00 53E1		USART2_DR	USART2 data register	0xXX
0x00 53E2		USART2_BRR1	USART2 baud rate register 1	0x00
0x00 53E3		USART2_BRR2	USART2 baud rate register 2	0x00
0x00 53E4		USART2_CR1	USART2 control register 1	0x00
0x00 53E5		USART2_CR2	USART2 control register 2	0x00
0x00 53E6		USART2_CR3	USART2 control register 3	0x00
0x00 53E7		USART2_CR4	USART2 control register 4	0x00
0x00 53E8		USART2_CR5	USART2 control register 5	0x00
0x00 53E9		USART2_GTR	USART2 guard time register	0x00
0x00 53EA		USART2_PSCR	USART2 prescaler register	0x00
0x00 53EB to 0x00 53EF	Reserved area			
0x00 53F0	USART3	USART3_SR	USART3 status register	0xC0
0x00 53F1		USART3_DR	USART3 data register	0xXX
0x00 53F2		USART3_BRR1	USART3 baud rate register 1	0x00
0x00 53F3		USART3_BRR2	USART3 baud rate register 2	0x00
0x00 53F4		USART3_CR1	USART3 control register 1	0x00
0x00 53F5		USART3_CR2	USART3 control register 2	0x00
0x00 53F6		USART3_CR3	USART3 control register 3	0x00
0x00 53F7		USART3_CR4	USART3 control register 4	0x00
0x00 53F8		USART3_CR5	USART3 control register 5	0x00
0x00 53F9		USART3_GTR	USART3 guard time register	0x00
0x00 53FA		USART3_PSCR	USART3 prescaler register	0x00
0x00 53FB to 0x00 53FF	Reserved area			

9.3.3 Supply current characteristics

Total current consumption

The MCU is placed under the following conditions:

- All I/O pins in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except if explicitly mentioned.

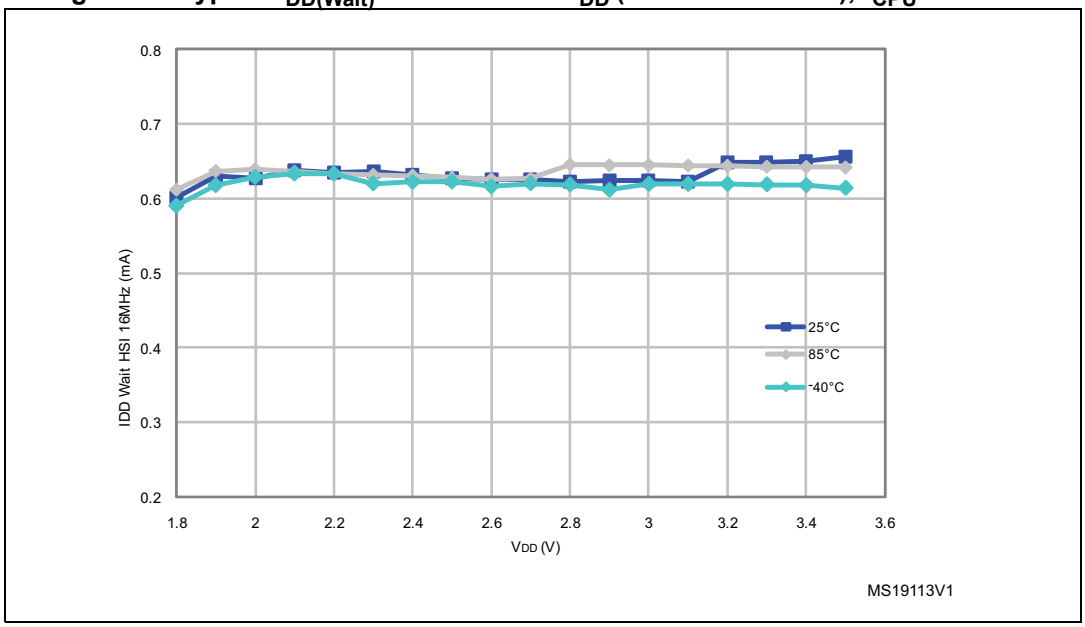
In the following table, data are based on characterization results, unless otherwise specified.

Subject to general operating conditions for V_{DD} and T_A.

Table 20. Total current consumption in Run mode

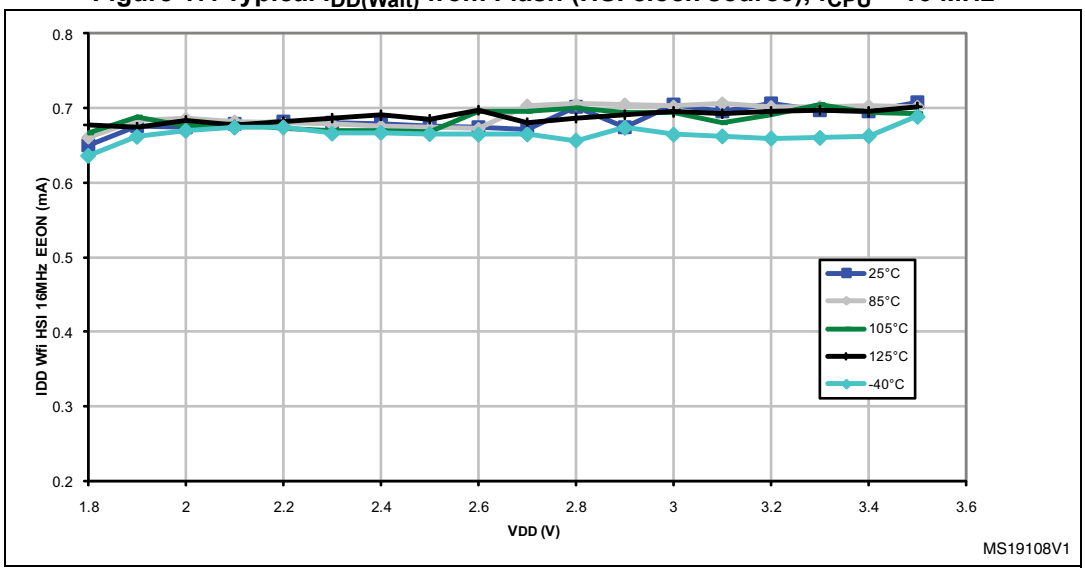
Symbol	Para meter	Conditions(1)			Typ.	Max.				Unit
						55°C	85 °C (2)	105 °C (3)	125 °C (4)	
$I_{DD(RUN)}$	Supply current in run mode (5)	All peripherals OFF, code executed from RAM, V_{DD} from 1.65 V to 3.6 V	HSI RC osc. (16 MHz)(6)	f_{CPU} = 125 kHz	0.22	0.28	0.39	0.47	0.51	mA
				f_{CPU} = 1 MHz	0.32	0.38	0.49	0.57	0.61	
				f_{CPU} = 4 MHz	0.59	0.65	0.76	0.84	0.88	
				f_{CPU} = 8 MHz	0.93	0.99	1.1	1.18	1.22	
				f_{CPU} = 16 MHz	1.62	1.68	1.79(7)	1.87(7)	1.91(7)	
			HSE external clock (f_{CPU}=f_{HSE}) (8)	f_{CPU} = 125 kHz	0.21	0.25	0.35	0.44	0.49	
				f_{CPU} = 1 MHz	0.3	0.34	0.44	0.53	0.58	
				f_{CPU} = 4 MHz	0.57	0.61	0.71	0.8	0.85	
				f_{CPU} = 8 MHz	0.95	0.99	1.09	1.18	1.23	
				f_{CPU} = 16 MHz	1.73	1.77	1.87(7)	1.96(7)	2.01(7)	
			LSI RC osc. (typ. 38 kHz)	f_{CPU} = f_{LSI}	0.029	0.035	0.039	0.044	0.055	
			LSE external clock (32.768 kHz)	f_{CPU} = f_{LSE}	0.028	0.034	0.038	0.042	0.054	

Figure 16. Typical $I_{DD(Wait)}$ from RAM vs. V_{DD} (HSI clock source), f_{CPU} = 16 MHz



1. Typical current consumption measured with code executed from RAM.

Figure 17. Typical $I_{DD(Wait)}$ from Flash (HSI clock source), f_{CPU} = 16 MHz



1. Typical current consumption measured with code executed from Flash.

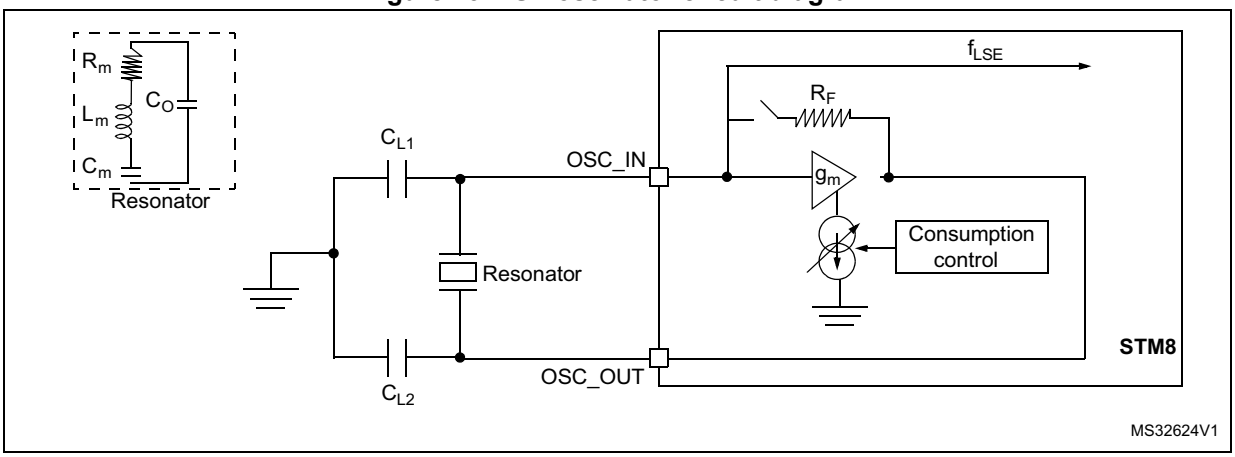
Table 24. Total current consumption and timing in Active-halt mode at V_{DD} = 1.65 V to 3.6 V (continued)

Symbol	Parameter	Conditions[1]			Typ.	Max.	Unit
$I_{DD(AH)}$	Supply current in Active-halt mode	LSE external clock (32.768 kHz) (6)	LCD OFF[7]	T_A = -40 °C to 25 °C	0.54	1.35	µA
				T_A = 55 °C	0.61	1.44	
				T_A = 85 °C	0.91	2.27	
				T_A = 105 °C	2.24	5.42	
				T_A = 125 °C	5.03	12	
			LCD ON (static duty/ external V_{LCD}) [3]	T_A = -40 °C to 25 °C	0.91	2.13	
				T_A = 55 °C	1.05	2.55	
				T_A = 85 °C	1.42	3.65	
				T_A = 105 °C	2.63	6.35	
				T_A = 125 °C	5.24	13.15	
			LCD ON (1/4 duty/ external V_{LCD}) [4]	T_A = -40 °C to 25 °C	1.6	2.84	
				T_A = 55 °C	1.76	4.37	
				T_A = 85 °C	2.14	5.23	
				T_A = 105 °C	3.37	8.5	
				T_A = 125 °C	5.92	15.19	
			LCD ON (1/4 duty/ internal V_{LCD}) [5]	T_A = -40 °C to 25 °C	3.89	9.15	
				T_A = 55 °C	3.89	9.15	
				T_A = 85 °C	4.25	10.49	
				T_A = 105 °C	5.42	16.31	
				T_A = 125 °C	6.58	16.6	
$I_{DD(WUFAH)}$	Supply current during wakeup time from Active-halt mode (using HSI)	-	-	-	2.4	-	mA
$t_{WU\_HSI(AH)}$[8][9]	Wakeup time from Active-halt mode to Run mode (using HSI)	-	-	-	4.7	7	µs
$t_{WU\_LSI(AH)}$[8][9]	Wakeup time from Active-halt mode to Run mode (using LSI)	-	-	-	150	-	µs

1. No floating I/O, unless otherwise specified.
2. RTC enabled. Clock source = LSI
3. RTC enabled, LCD enabled with external V_{LCD} = 3 V, static duty, division ratio = 256, all pixels active, no LCD connected.
4. RTC enabled, LCD enabled with external V_{LCD}, 1/4 duty, 1/3 bias, division ratio = 64, all pixels active, no LCD connected.
5. LCD enabled with internal LCD booster V_{LCD} = 3 V, 1/4 duty, 1/3 bias, division ratio = 64, all pixels active, no LCD connected.
6. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD\ LSE}$) must be added. Refer to *Table 32*

4. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Figure 23. LSE oscillator circuit diagram



Internal clock sources

Subject to general operating conditions for V_{DD}, and T_A.

High speed internal RC oscillator (HSI)

In the following table, data are based on characterization results unless otherwise specified.

Table 33. HSI oscillator characteristics

Symbol	Parameter	Conditions(1)	Min.	Typ.	Max.	Unit
f_{HSI}	Frequency	V_{DD} = 3.0 V		16		MHz
ACC_{HSI}	Accuracy of HSI oscillator (factory calibrated)	V_{DD} = 3.0 V, T_A = 25 °C	-1 (2)		1 (2)	%
		V_{DD} = 3.0 V, 0 °C ≤T_A ≤ 55 °C	-1.5		1.5	%
		V_{DD} = 3.0 V, -10 °C ≤T_A ≤ 70 °C	-2		2	%
		V_{DD} = 3.0 V, -10 °C ≤T_A ≤ 85 °C	-2.5		2	%
		V_{DD} = 3.0 V, -10 °C ≤T_A ≤ 125 °C	-4.5		2	%
		1.65 V ≤V_{DD} ≤ 3.6 V, -40 °C ≤T_A ≤ 125 °C	-4.5		3	%
TRIM	HSI user trimming step(3)	Trimming code ≠ multiple of 16		0.4	0.7	%
		Trimming code = multiple of 16			± 1.5	%
$t_{su(HSI)}$	HSI oscillator setup time (wakeup time)			3.7	6 (4)	µs
$I_{DD(HSI)}$	HSI oscillator power consumption			100	140(4)	µA

1. V_{DD} = 3.0 V, T_A = -40 to 125 °C unless otherwise specified.
2. Tested in production.
3. The trimming step differs depending on the trimming code. It is usually negative on the codes which are multiples of 16 (0x00, 0x10, 0x20, 0x30...0xE0). Refer to the AN3101 “STM8L15x internal RC oscillator calibration” application note for more details.

Figure 26. Typical V_{IL} and V_{IH} vs. V_{DD} (standard I/Os)

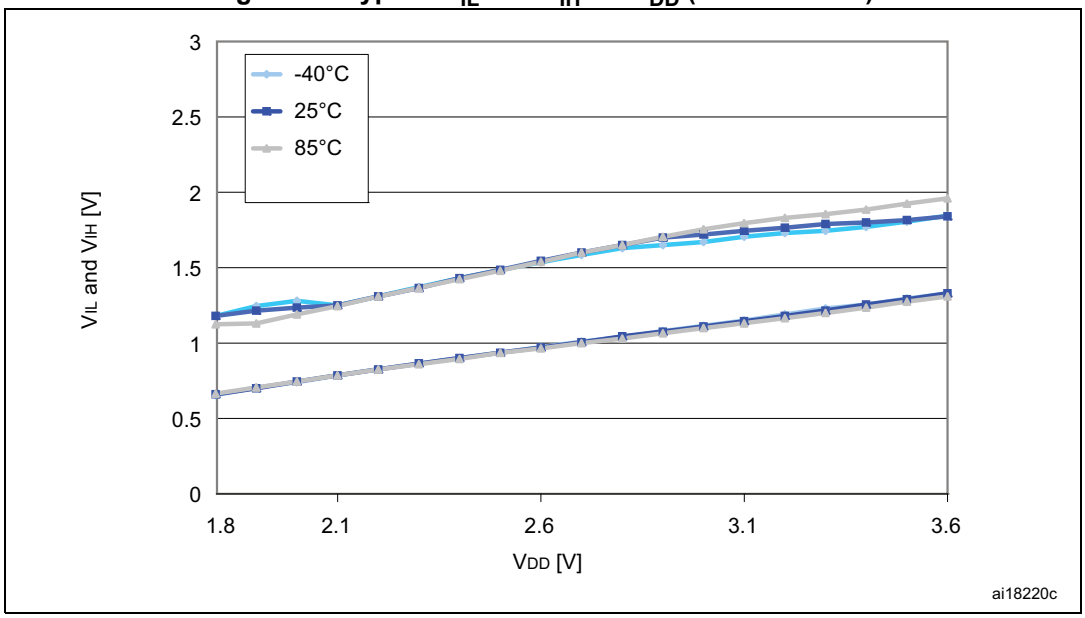


Figure 27. Typical V_{IL} and V_{IH} vs. V_{DD} (true open drain I/Os)

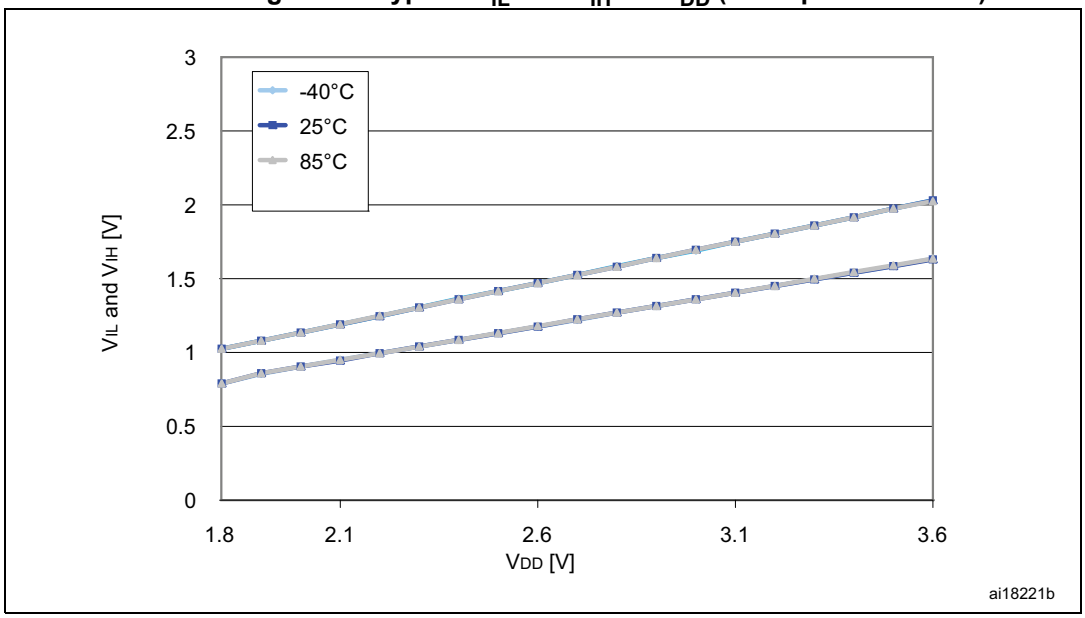


Figure 28. Typical pull-up resistance R_{PU} vs. V_{DD} with $V_{IN}=V_{SS}$

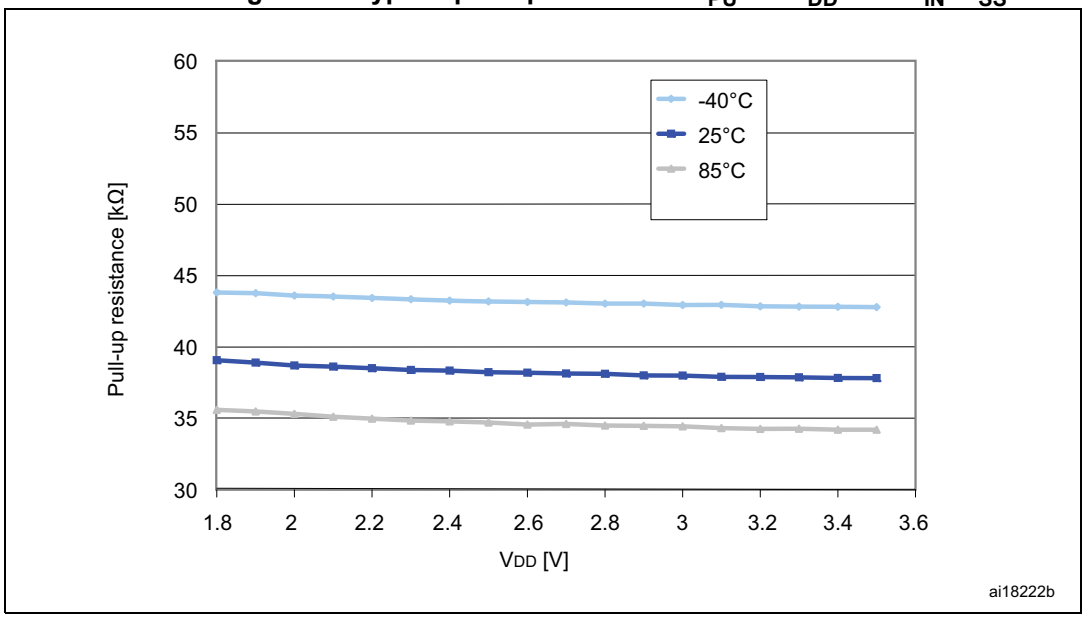
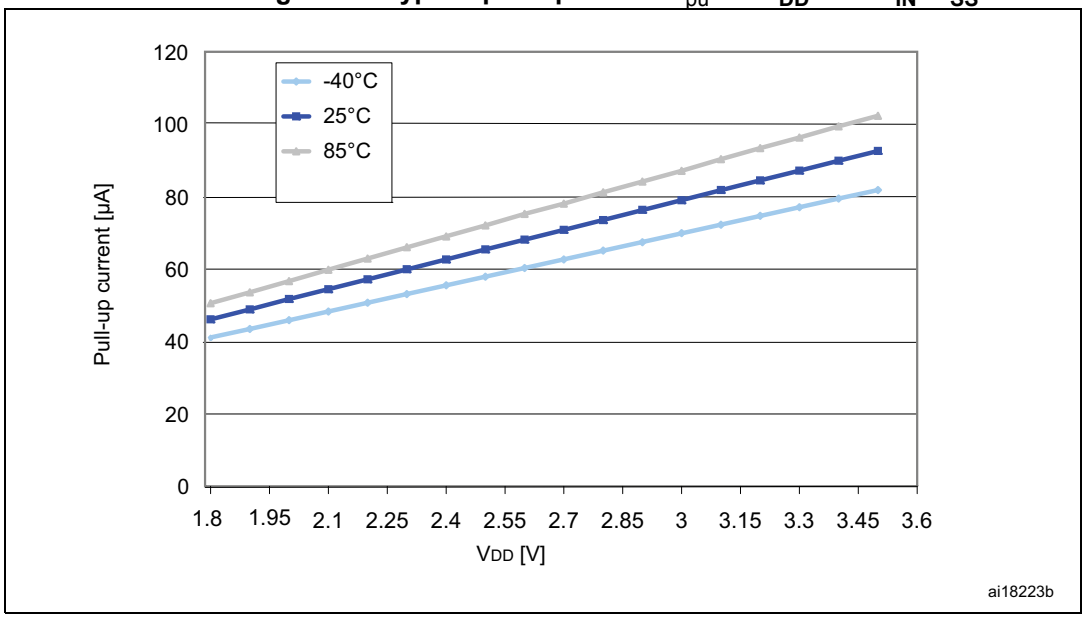


Figure 29. Typical pull-up current I_{pu} vs. V_{DD} with $V_{IN}=V_{SS}$



Output driving current

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 39. Output driving current (high sink ports)

I/O Type	Symbol	Parameter	Conditions	Min.	Max.	Unit
Standard	V_{OL} (1)	Output low level voltage for an I/O pin	I_{IO} = +2 mA, V_{DD} = 3.0 V	-	0.45	V
			I_{IO} = +2 mA, V_{DD} = 1.8 V	-	0.45	
			I_{IO} = +10 mA, V_{DD} = 3.0 V	-	0.7	
	V_{OH} (2)	Output high level voltage for an I/O pin	I_{IO} = -2 mA, V_{DD} = 3.0 V	V_{DD}-0.45	-	
			I_{IO} = -1 mA, V_{DD} = 1.8 V	V_{DD}-0.45	-	
			I_{IO} = -10 mA, V_{DD} = 3.0 V	V_{DD}-0.7	-	

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Table 16* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. The I_{IO} current sourced must always respect the absolute maximum rating specified in *Table 16* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.

Table 40. Output driving current (true open drain ports)

I/O Type	Symbol	Parameter	Conditions	Min.	Max.	Unit
Open drain	V_{OL} (1)	Output low level voltage for an I/O pin	I_{IO} = +3 mA, V_{DD} = 3.0 V	-	0.45	V
			I_{IO} = +1 mA, V_{DD} = 1.8 V	-	0.45	

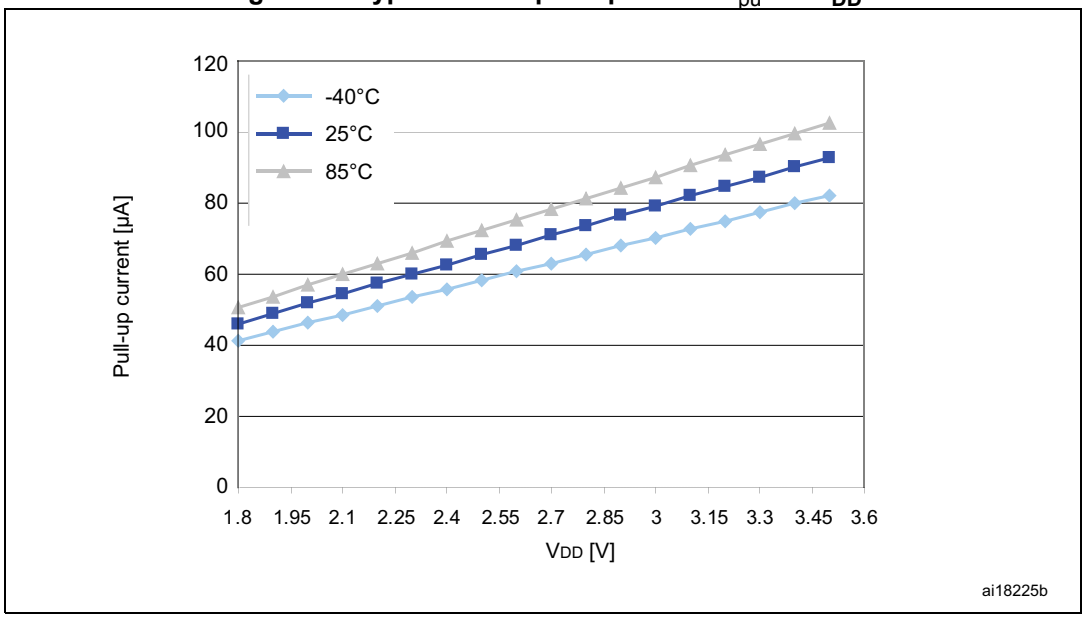
1. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Table 16* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.

Table 41. Output driving current (PA0 with high sink LED driver capability)

I/O Type	Symbol	Parameter	Conditions	Min.	Max.	Unit
IR	V_{OL} (1)	Output low level voltage for an I/O pin	I_{IO} = +20 mA, V_{DD} = 2.0 V	-	0.45	V

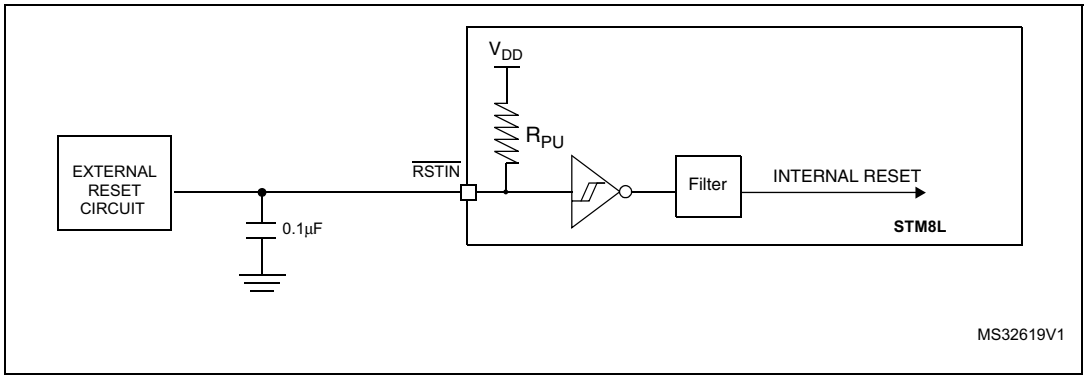
1. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Table 16* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.

Figure 37. Typical NRST pull-up current I_{pu} vs. V_{DD}



The reset network shown in *Figure 38* protects the device against parasitic resets. The user must ensure that the level on the NRST pin can go below the V_{IL} max. level specified in *Table 42*. Otherwise the reset is not taken into account internally. For power consumption-sensitive applications, the capacity of the external reset capacitor can be reduced to limit the charge/discharge current. If the NRST signal is used to reset the external circuitry, the user must pay attention to the charge/discharge time of the external capacitor to meet the reset timing conditions of the external devices. The minimum recommended capacity is 10 nF.

Figure 38. Recommended NRST pin configuration



9.3.9 LCD controller (STM8L152x6/8 only)

In the following table, data are guaranteed by design.

Table 45. LCD characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{LCD}	LCD external voltage	-		3.6	V
V_{LCD0}	LCD internal reference voltage 0	-	2.6	-	
V_{LCD1}	LCD internal reference voltage 1	-	2.7	-	
V_{LCD2}	LCD internal reference voltage 2	-	2.8	-	
V_{LCD3}	LCD internal reference voltage 3	-	3.0	-	
V_{LCD4}	LCD internal reference voltage 4	-	3.1	-	
V_{LCD5}	LCD internal reference voltage 5	-	3.2	-	
V_{LCD6}	LCD internal reference voltage 6	-	3.4	-	
V_{LCD7}	LCD internal reference voltage 7	-	3.5	-	
C_{EXT}	V_{LCD} external capacitance	0.1	1	2	µF
I_{DD}	Supply current(1) at V_{DD} = 1.8 V	-	3	-	µA
	Supply current(1) at V_{DD} = 3 V	-	3	-	
R_{HN}(2)	High value resistive network (low drive)	-	6.6	-	MΩ
R_{LN}(3)	Low value resistive network (high drive)	-	240	-	kΩ
V_{33}	Segment/Common higher level voltage	-		V_{LCDx}	V
V_{34}	Segment/Common 3/4 level voltage	-	$3/4V_{LCDx}$	-	
V_{23}	Segment/Common 2/3 level voltage	-	$2/3V_{LCDx}$	-	
V_{12}	Segment/Common 1/2 level voltage	-	$1/2V_{LCDx}$	-	
V_{13}	Segment/Common 1/3 level voltage	-	$1/3V_{LCDx}$	-	
V_{14}	Segment/Common 1/4 level voltage	-	$1/4V_{LCDx}$	-	
V_0	Segment/Common lowest level voltage	0	-	-	

1. LCD enabled with 3 V internal booster (LCD_CR1 = 0x08), 1/4 duty, 1/3 bias, division ratio= 64, all pixels active, no LCD connected.
2. R_{HN} is the total high value resistive network.
3. R_{LN} is the total low value resistive network.

VLCD external capacitor (STM8L152x6/8 only)

The application can achieve a stabilized LCD reference voltage by connecting an external capacitor C_{EXT} to the V_{LCD} pin. C_{EXT} is specified in *Table 45*.

9.3.11 Temperature sensor

In the following table, data are based on characterization results unless otherwise specified.

Table 47. TS characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{90} (1)	Sensor reference voltage at 90°C ±5 °C,	0.580	0.597	0.614	V
T_L	V_{SENSOR} linearity with temperature	-	±1	±2	°C
Avg_slope(2)	Average slope	1.59	1.62	1.65	mV/°C
$IDD_{(TEMP)}$(2)	Consumption	-	3.4	6	µA
T_{START}(2)(3)	Temperature sensor startup time	-	-	10	µs
T_{S_TEMP}(2)	ADC sampling time when reading the temperature sensor	-	5	10	µs

1. Tested in production at V_{DD} = 3 V ±10 mV. The 8 LSB of the V_{90} ADC conversion result are stored in the TS_Factory_CONV_V90 byte.
2. Guaranteed by design.
3. Defined for ADC output reaching its final value ±1/2LSB.

9.3.12 Comparator characteristics

In the following tables, data are guaranteed by design.

Table 48. Comparator 1 characteristics

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
V_{DDA}	Analog supply voltage		1.65	-	3.6	V
R_{400K}	R_{400K} value	-	-	400	-	kΩ
R_{10K}	R_{10K} value	-	-	10	-	
V_{IN}	Comparator 1 input voltage range	-	0.6	-	V_{DDA}	V
t_{START}	Comparator startup time	-	-	7	10	µs
td	Propagation delay(2)	-	-	3	10	
Voffset	Comparator offset	-	-	±3	±10	mV
$d_{Voffset}/dt$	Comparator offset variation in worst voltage stress conditions	V_{DDA} = 3.6 V V_{IN+} = 0 V V_{IN-} = V_{REFINT} T_A = 25 °C	0	1.5	10	mV/1000 h
I_{COMP1}	Current consumption(3)	-	-	160	260	nA

1. Based on characterization.
2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.
3. Comparator consumption only. Internal reference voltage not included.

In the following table, data based on characterization results.

Table 51. DAC accuracy

Symbol	Parameter	Conditions	Typ.	Max.	Unit
DNL	Differential non linearity(1)	R_L ≥5 kΩ, C_L≤50 pF DACOUT buffer ON(2)	1.5	3	12-bit LSB
		No load DACOUT buffer OFF	1.5	3	
INL	Integral non linearity(3)	R_L ≥5 kΩ, C_L≤ 50 pF DACOUT buffer ON(2)	2	4	
		No load DACOUT buffer OFF	2	4	
Offset	Offset error(4)	R_L ≥5 kΩ, C_L≤ 50 pF DACOUT buffer ON(2)	±10	±25	
		No load DACOUT buffer OFF	±5	±8	
Offset1	Offset error at Code 1 (5)	DACOUT buffer OFF	±1.5	±5	
Gain error	Gain error(6)	R_L ≥5 kΩ, C_L≤ 50 pF DACOUT buffer ON(2)	+0.1/-0.2	+0.2/-0.5	%
		No load DACOUT buffer OFF	+0/-0.2	+0/-0.4	
TUE	Total unadjusted error	R_L ≥5 kΩ, C_L≤ 50 pF DACOUT buffer ON(2)	12	30	12-bit LSB
		No load -DACOUT buffer OFF	8	12	

1. Difference between two consecutive codes - 1 LSB.
2. In 48-pin package devices the DAC2 output buffer must be kept off and no load must be applied on the DAC_OUT2 output.
3. Difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023.
4. Difference between the value measured at Code (0x800) and the ideal value = V_{REF+}/2.
5. Difference between the value measured at Code (0x001) and the ideal value.
6. Difference between the ideal slope of the transfer function and the measured slope computed from Code 0x000 and 0xFFF when buffer is ON, and from Code giving 0.2 V and (V_{DDA} -0.2) V when buffer is OFF.

In the following table, data are guaranteed by design.

Table 52. DAC output on PB4-PB5-PB6(1)

Symbol	Parameter	Conditions	Max	Unit
R_{int}	Internal resistance between DAC output and PB4-PB5-PB6 output	2.7 V < V_{DD} < 3.6 V	1.4	kΩ
		2.4 V < V_{DD} < 3.6 V	1.6	
		2.0 V < V_{DD} < 3.6 V	3.2	
		1.8 V < V_{DD} < 3.6 V	8.2	

1. 32 or 28-pin packages only. The DAC channel can be routed either on PB4, PB5 or PB6 using the routing interface I/O switch registers.

Figure 43. ADC1 accuracy characteristics

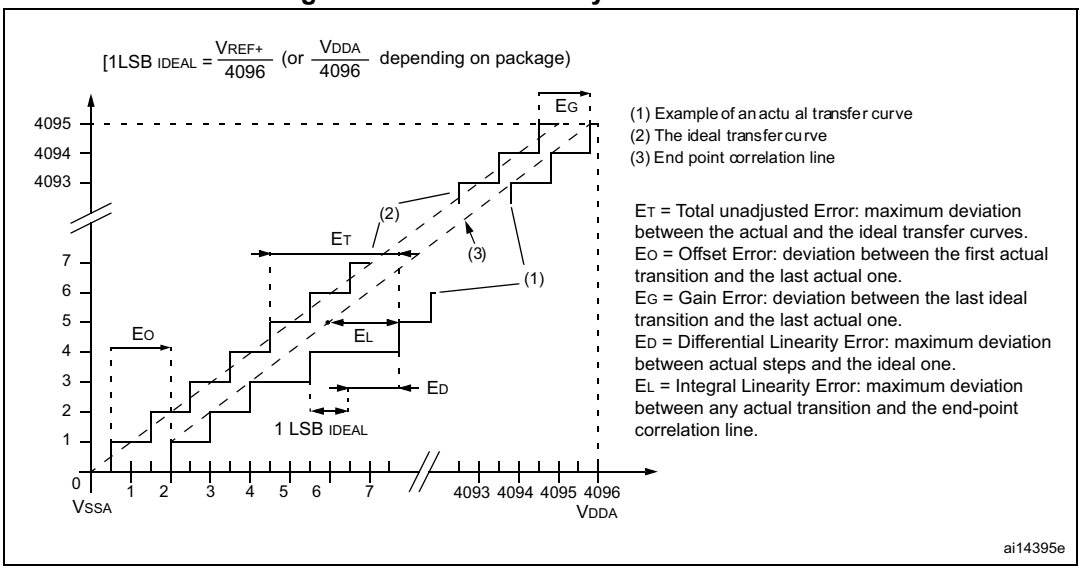
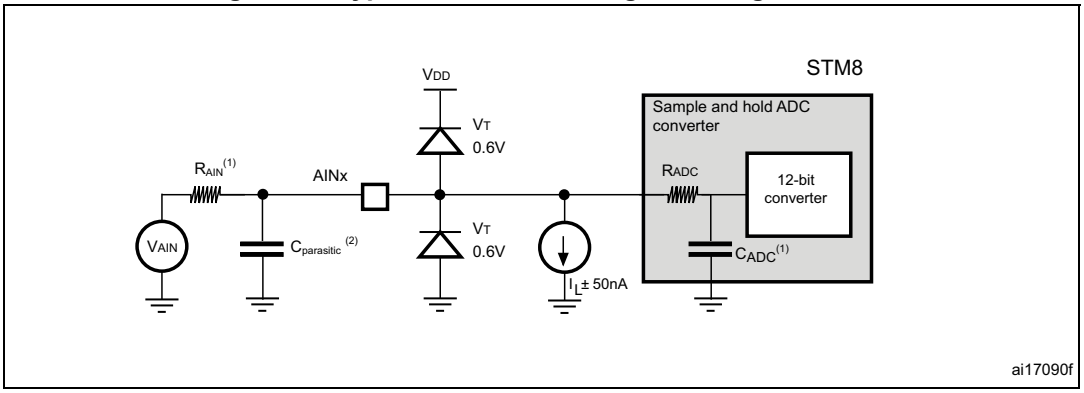


Figure 44. Typical connection diagram using the ADC



1. Refer to *Table 53* for the values of R_{AIN} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

Figure 46. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})

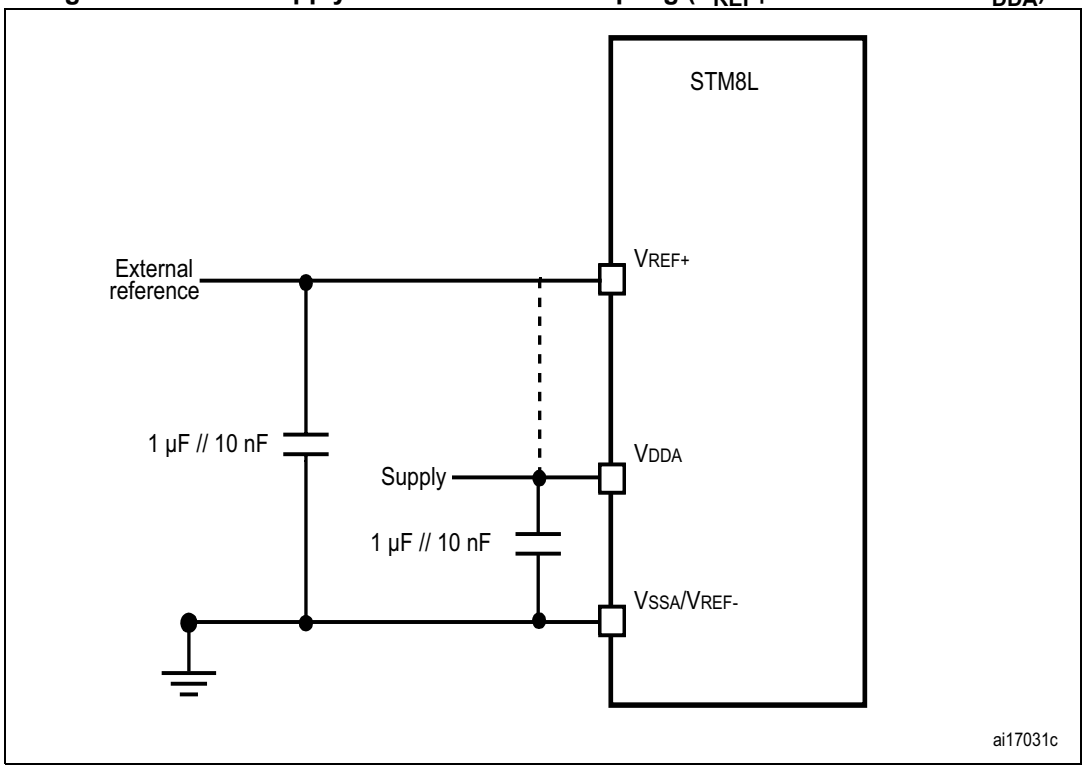
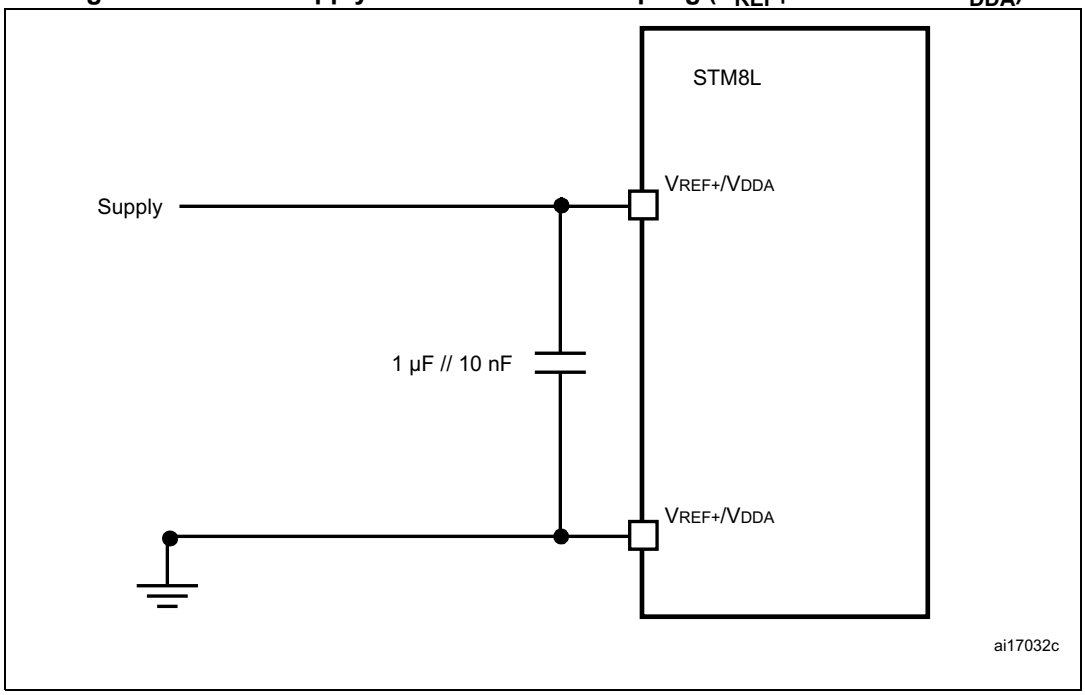


Figure 47. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})

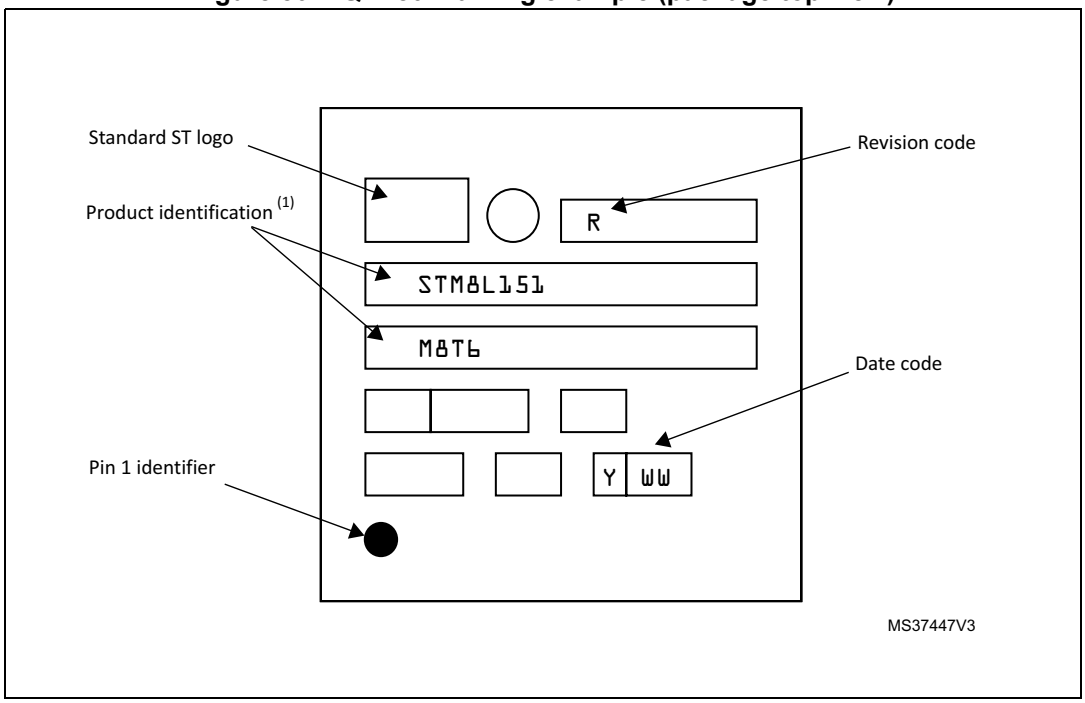


Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 50. LQFP80 marking example (package top view)



1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 70. Document revision history (continued)

Date	Revision	Changes
15-Feb-2017	10	Updated value of feature 12-bit synchronized ADC (number of channels) for STM8L15xK8 on *Table 2: High-density and medium+ density STM8L15xx6/8 low power device features and peripheral counts*.