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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, IR, LCD, POR, PWM, WDT
Number of I/O	41
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 25x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8l152c8t6tr

It is clocked by the internal LSI RC clock source, and thus stays active even in case of a CPU clock failure.

3.16 Beeper

The beeper function outputs a signal on the BEEP pin for sound generation. The signal is in the range of 1, 2 or 4 kHz.

3.17 Communication interfaces

3.17.1 SPI

The serial peripheral interfaces (SPI1 and SPI2) provide half/ full duplex synchronous serial communication with external devices.

- Maximum speed: 8 Mbit/s ($f_{SYSCLK}/2$) both for master and slave
- Full duplex synchronous transfers
- Simplex synchronous transfers on 2 lines with a possible bidirectional data line
- Master or slave operation - selectable by hardware or software
- Hardware CRC calculation
- Slave/master selection input pin

Note: SPI1 and SPI2 can be served by the DMA1 Controller.

3.17.2 I^2C

The I^2C bus interface (I2C1) provides multi-master capability, and controls all I²C bus-specific sequencing, protocol, arbitration and timing.

- Master, slave and multi-master capability
- Standard mode up to 100 kHz and fast speed modes up to 400 kHz.
- 7-bit and 10-bit addressing modes.
- SMBus 2.0 and PMBus support
- Hardware CRC calculation

Note: I^2C1 can be served by the DMA1 Controller.

3.17.3 USART

The USART interfaces (USART1, USART2 and USART3) allow full duplex, asynchronous communications with external devices requiring an industry standard NRZ asynchronous serial data format. It offers a very wide range of baud rates.

- 1 Mbit/s full duplex SCI
- SPI1 emulation
- High precision baud rate generator
- Smartcard emulation
- IrDA SIR encoder decoder
- Single wire half duplex mode

Note: USART1, USART2 and USART3 can be served by the DMA1 Controller.

3.18 Infrared (IR) interface

The high-density and medium+ density STM8L15xx6/8 devices contain an infrared interface which can be used with an IR LED for remote control functions. Two timer output compare channels are used to generate the infrared remote control signals.

3.19 Development support

Development tools

Development tools for the STM8 microcontrollers include:

- The STice emulation system offering tracing and code profiling
- The STVD high-level language debugger including C compiler, assembler and integrated development environment
- The STVP Flash programming software

The STM8 also comes with starter kits, evaluation boards and low-cost in-circuit debugging/programming tools.

Single wire data interface (SWIM) and debug module

The debug module with its single wire data interface (SWIM) permits non-intrusive real-time in-circuit debugging and fast memory programming.

The Single wire interface is used for direct access to the debugging module and memory programming. The interface can be activated in all device operation modes.

The non-intrusive debugging module features a performance close to a full-featured emulator. Beside memory and peripherals, CPU operation can also be monitored in real-time by means of shadow registers.

Bootloader

A bootloader is available to reprogram the Flash memory using the USART1, USART2, USART3 (USARTs in asynchronous mode), SPI1 or SPI2 interfaces. The reference document for the bootloader is *UM0560: STM8 bootloader user manual*.

Table 4. Legend/abbreviation

Type	I= input, O = output, S = power supply	
Level	FT: Five-volt tolerant	
	Output	HS = high sink/source (20 mA)
Port and control configuration	Input	float = floating, wpu = weak pull-up
	Output	T = true open drain, OD = open drain, PP = push pull
Reset state	Bold X (pin state after reset release). Unless otherwise specified, the pin state is the same during the reset phase (i.e. “under reset”) and after internal reset release (i.e. at reset state).	

Table 5. High-density and medium+ density STM8L15x pin description

Pin number				Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP80	LQFP64	UFQFPN48 and LQFP48	WLCSP32				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
1	-	-	-	PH0/LCD SEG 36 (3)	I/O	FT(6)	**X**	X	X	HS	X	X	**Port H0**	LCD segment 36
2	-	-	-	PH1/LCD SEG 37 (3)	I/O	FT(6)	**X**	X	X	HS	X	X	**Port H1**	LCD segment 37
3	-	-	-	PH2/LCD SEG 38 (3)	I/O	FT(6)	**X**	X	X	HS	X	X	**Port H2**	LCD segment 38
4	-	-	-	PH3/LCD SEG 39 (3)	I/O	FT(6)	**X**	X	X	HS	X	X	**Port H3**	LCD segment 39
6	2	2	C3	NRST/PA1(1)	I/O	-	-	**X**		HS	-	X	**Reset**	PA1
7	3	3	B4	PA2/OSC_IN/ *[USART1_TX](2)/ [SPI1_MISO]* (2)	I/O	-	**X**	X	X	HS	X	X	**Port A2**	HSE oscillator input / *[USART1 transmit] / [SPI1 master in- slave out] /*
8	4	4	C4	PA3/OSC_OUT/ *[USART1_RX](2)/[SPI1_MOSI](2)*	I/O	-	**X**	X	X	HS	X	X	**Port A3**	HSE oscillator output / *[USART1 receive]/ [SPI1 master out/slave in]/*
9	5	5	D3	PA4/TIM2_BKIN/ *[TIM2_ETR](2)* LCD_COM0(3)/ADC1_IN2 *[COMP1_INP]*	I/O	FT(6)	**X**	X	X	HS	X	X	**Port A4**	Timer 2 - break input / */[Timer 2 - trigger]* / LCD COM 0 / ADC1 input 2/ *[Comparator 1 positive input]*
10	6	6	D4	PA5/TIM3_BKIN/ *[TIM3_ETR](2)*/ LCD_COM1(3)/ADC1_IN1/ *[COMP1_INP]*	I/O	FT(6)	**X**	X	X	HS	X	X	**Port A5**	Timer 3 - break input / *[Timer 3 - trigger]* / LCD_COM 1 / ADC1 input 1/ *[Comparator 1 positive input]*

Table 5. High-density and medium+ density STM8L15x pin description (continued)

Pin number				Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP80	LQFP64	UFQFPN48 and LQFP48	WLCSP32				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
62	50	-	-	PG5/LCD_SEG33/ SPI2_SCK	I/O	FT(6)	**X**	X	X	HS	X	X	**Port G5**	LCD segment 33 / SPI2 clock
63	51	-	-	PG6/LCD_SEG34/ SPI2_MOSI	I/O	FT(6)	**X**	X	X	HS	X	X	**Port G6**	LCD segment 34 / SPI2 master out- slave in
64	52	-	-	PG7/LCD_SEG35/ SPI2_MISO	I/O	FT(6)	**X**	X	X	HS	X	X	**Port G7**	LCD segment 35 / SPI2 master in- slave out
23	19	14	-(4)	PE0/LCD_SEG1(3)/ TIM5_CH2	I/O	FT(6)	**X**	X	X	HS	X	X	**Port E0**	LCD segment 1/ Timer 5 channel 2
24	20	15	-(4)	PE1/TIM1_CH2N /LCD_SEG2(3)	I/O	FT(6)	**X**	X	X	HS	X	X	**Port E1**	Timer 1 - inverted channel 2 / LCD segment 2
25	21	16	-(4)	PE2/TIM1_CH3N /LCD_SEG3(3)/ *[CCO]*(2)	I/O	FT(6)	**X**	X	X	HS	X	X	**Port E2**	Timer 1 - inverted channel 3 / LCD segment 3 / *[Configurable clock output]*
26	-	-	-	PE3/LCD_SEG4(3)	I/O	FT(6)	**X**	X	X	HS	X	X	**Port E3**	LCD segment 4
-	22	17	H2	PE3/LCD_SEG4(3)/ USART2_RX	I/O	FT(6)	**X**	X	X	HS	X	X	**Port E3**	LCD segment 4/ USART2 receive
27	-	-	-	PE4/LCD_SEG5(3)/ DAC_TRIG1	I/O	FT(6)	**X**	X	X	HS	X	X	**Port E4**	LCD segment 5/ DAC 1 trigger
-	23	18	H3	PE4/LCD_SEG5(3)/ DAC_TRIG2/USART2_TX	I/O	FT(6)	**X**	X	X	HS	X	X	**Port E4**	LCD segment 5/ DAC 2 trigger/ USART2 transmit
28	-	-	-	PE5/LCD_SEG6(3)/ ADC1_IN23/*[COMP1_INP]*/ *[COMP2_INP]*	I/O	FT(6)	**X**	X	X	HS	X	X	**Port E5**	LCD segment 6 / ADC1_IN23/ *[Comparator 1 positive input]* /*[Comparator 2 positive input]*
-	24	19	-(4)	PE5/LCD_SEG6(3)/ ADC1_IN23/*[COMP1_INP]*/ *[COMP2_INP]* / USART2_CK	I/O	FT(6)	**X**	X	X	HS	X	X	**Port E5**	LCD segment 6 / ADC1_IN23/ *[Comparator 1 positive input]* / *[Comparator 2 positive input]* /USART2 synchronous clock

Table 5. High-density and medium+ density STM8L15x pin description (continued)

Pin number				Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP80	LQFP64	UFQFPN48 and LQFP48	WLCSP32				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
-	-	-	G4	$V_{DD1}/V_{DDA}/V_{REF+}$	S	-	-	-	-	-	-	-	Digital power supply / Analog power supply / ADC1 positive voltage reference	
17	13	12	-	V_{REF+}/V_{REF+_DAC}	S	-	-	-	-	-	-	-	ADC1 and DAC1/2 positive voltage reference	
18	14	-	-	PG0/LCD SEG28(3) /USART3_RX/ *[TIM2_BKIN]*	I/O	FT(6)	**X**	X	X	HS	X	X	**Port G0**	LCD segment 28/ USART3 receive / *[Timer 2 - break input]*
19	15	-	-	PG1/LCD SEG29(3) /USART3_TX/ *[TIM3_BKIN]*	I/O	FT(6)	**X**	X	X	HS	X	X	**Port G1**	LCD segment 29/ USART3 transmit / *[Timer 3 -break input]*
20	16	-	-	PG2/LCD_SEG30(3)/ USART3_CK	I/O	FT(6)	**X**	X	X	HS	X	X	**Port G2**	LCD segment 30/ USART 3 synchronous clock
21	17	-	-	PG3/LCD SEG 31 (3)/ *[TIM3_ETR]*	I/O	FT(6)	**X**	X	X	HS	X	X	**Port G3**	LCD segment 31/ *[Timer 3 - trigger]*
33	-	-	-	PH4/USART2_RX	I/O	FT(6)	**X**	X	X	HS	X	X	**Port H4**	USART2 receive
34	-	-	-	PH5/USART2_TX	I/O	FT(6)	**X**	X	X	HS	X	X	**Port H5**	USART2 transmit
35	-	-	-	PH6/USART2_CK/ TIM5_CH1	I/O	FT(6)	**X**	X	X	HS	X	X	**Port H6**	USART2 synchronous clock/ Timer 5 - channel 1
36	-	-	-	PH7/TIM5_CH2	I/O	FT(6)	**X**	X	X	HS	X	X	**Port H7**	Timer 5 - channel 2
-	-	9	F4	V_{SS} /V_{SSA} /V_{REF-}	S	-	-	-	-	-	-	-	I/O ground / Analog ground voltage / ADC1 negative voltage reference	
13	9	-	-	V_{SSA} /V_{REF-}	S	-	-	-	-	-	-	-	Analog ground voltage / ADC1 negative voltage reference	
37	29	-	-	V_{DD3}	S	-	-	-	-	-	-	-	IOs supply voltage	
38	30	-	H1	V_{SS3}	S	-	-	-	-	-	-	-	IOs ground voltage	
5	1	1	A4	PA0(9)/*[USART1_CK]*(2)/ SWIM/BEEP/IR_TIM (10)	I/O		X	**X**	X	HS	X	X	**Port A0**	*[USART1 synchronous clock]*(2)/ SWIM input and output / Beep output / Infrared Timer output
68	56	40	-	V_{SS2}	S	-	-	-	-	-	-	-	IOs ground voltage	
67	55	39	-	V_{DD2}	S	-	-	-	-	-	-	-	IOs supply voltage	

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 53C8 to 0x00 53DF	Reserved area			
0x00 53E0	USART2	USART2_SR	USART2 status register	0xC0
0x00 53E1		USART2_DR	USART2 data register	0xXX
0x00 53E2		USART2_BRR1	USART2 baud rate register 1	0x00
0x00 53E3		USART2_BRR2	USART2 baud rate register 2	0x00
0x00 53E4		USART2_CR1	USART2 control register 1	0x00
0x00 53E5		USART2_CR2	USART2 control register 2	0x00
0x00 53E6		USART2_CR3	USART2 control register 3	0x00
0x00 53E7		USART2_CR4	USART2 control register 4	0x00
0x00 53E8		USART2_CR5	USART2 control register 5	0x00
0x00 53E9		USART2_GTR	USART2 guard time register	0x00
0x00 53EA		USART2_PSCR	USART2 prescaler register	0x00
0x00 53EB to 0x00 53EF	Reserved area			
0x00 53F0	USART3	USART3_SR	USART3 status register	0xC0
0x00 53F1		USART3_DR	USART3 data register	0xXX
0x00 53F2		USART3_BRR1	USART3 baud rate register 1	0x00
0x00 53F3		USART3_BRR2	USART3 baud rate register 2	0x00
0x00 53F4		USART3_CR1	USART3 control register 1	0x00
0x00 53F5		USART3_CR2	USART3 control register 2	0x00
0x00 53F6		USART3_CR3	USART3 control register 3	0x00
0x00 53F7		USART3_CR4	USART3 control register 4	0x00
0x00 53F8		USART3_CR5	USART3 control register 5	0x00
0x00 53F9		USART3_GTR	USART3 guard time register	0x00
0x00 53FA		USART3_PSCR	USART3 prescaler register	0x00
0x00 53FB to 0x00 53FF	Reserved area			

Table 13. Option byte description

Option byte no.	Option description
OPT0	**ROP[7:0]** Memory readout protection (ROP) 0xAA: Disable readout protection (write access via SWIM protocol) Refer to Readout protection section in the STM8L reference manual (RM0031).
OPT1	**UBC[7:0]** Size of the user boot code area UBC[7:0] Size of the user boot code area 0x00: No UBC 0x01: Page 0 reserved for the UBC and write protected. ... 0xFF: Page 0 to 254 reserved for the UBC and write-protected. Refer to User boot code section in the STM8L reference manual (RM0031).
OPT2	**PCODESIZE[7:0]** Size of the proprietary code area 0x00: No proprietary code area 0x01: Page 0 reserved for the proprietary code and read/write protected. ... 0xFF: Page 0 to 254 reserved for the proprietary code and read/write protected. Refer to Proprietary code area (PCODE) section in the STM8L reference manual (RM0031) for more details.
OPT3	**IWDG_HW:** Independent watchdog 0: Independent watchdog activated by software 1: Independent watchdog activated by hardware
	IWDG_HALT: Independent watchdog off in Halt/Active-halt 0: Independent watchdog continues running in Halt/Active-halt mode 1: Independent watchdog stopped in Halt/Active-halt mode
	WWDG_HW: Window watchdog 0: Window watchdog activated by software 1: Window watchdog activated by hardware
	WWDG_HALT: Window window watchdog reset on Halt/Active-halt 0: Window watchdog stopped in Halt mode 1: Window watchdog generates a reset when MCU enters Halt mode
OPT4	**HSECNT**: Number of HSE oscillator stabilization clock cycles 0x00 - 1 clock cycle 0x01 - 16 clock cycles 0x10 - 512 clock cycles 0x11 - 4096 clock cycles
	LSECNT: Number of LSE oscillator stabilization clock cycles 0x00 - 1 clock cycle 0x01 - 16 clock cycles 0x10 - 512 clock cycles 0x11 - 4096 clock cycles

9.3 Operating conditions

Subject to general operating conditions for V_{DD} and T_A.

9.3.1 General operating conditions

Table 18. General operating conditions

Symbol	Parameter	Conditions		Min.	Max.	Unit
f_{SYSCLK}(1)	System clock frequency	1.65 V ≤V_{DD} < 3.6 V		0	16	MHz
V_{DD}	Standard operating voltage	BOR detector disabled (D suffix version)		1.65	3.6	V
		BOR detector enabled		1.8(2)		
V_{DDA}	Analog operating voltage	ADC and DAC not used	Must be at the same potential as V_{DD}	1.65	3.6	V
		ADC or DAC used		1.8	3.6	V
P_D(3)	Power dissipation at T_A= 85 °C for suffix 6 devices	LQFP80		-	526	mW
		LQFP64		-	416	
		UFQFPN48		-	625	
		LQFP48		-	307	
		WLCSP32		-	317	
	Power dissipation at T_A= 125 °C for suffix 3 devices and at T_A= 105 °C for suffix 7 devices	LQFP80		-	131	
		LQFP64		-	104	
		UFQFPN48		-	156	
		LQFP48		-	77	
T_A	Temperature range	1.65 V ≤V_{DD} < 3.6 V (6 suffix version)		-40	85	°C
		1.65 V ≤V_{DD} < 3.6 V (7 suffix version)		-40	105	
		1.65 V ≤V_{DD} < 3.6 V (3 suffix version)		-40	125	
T_J	Junction temperature range	-40 °C ≤T_A < 85 °C (6 suffix version)		-40	105	
		-40 °C ≤ T_A < 105 °C (7 suffix version)		-40	110(4)	
		-40 °C≤ T_A < 125 °C (3 suffix version)		-40	130(4)	

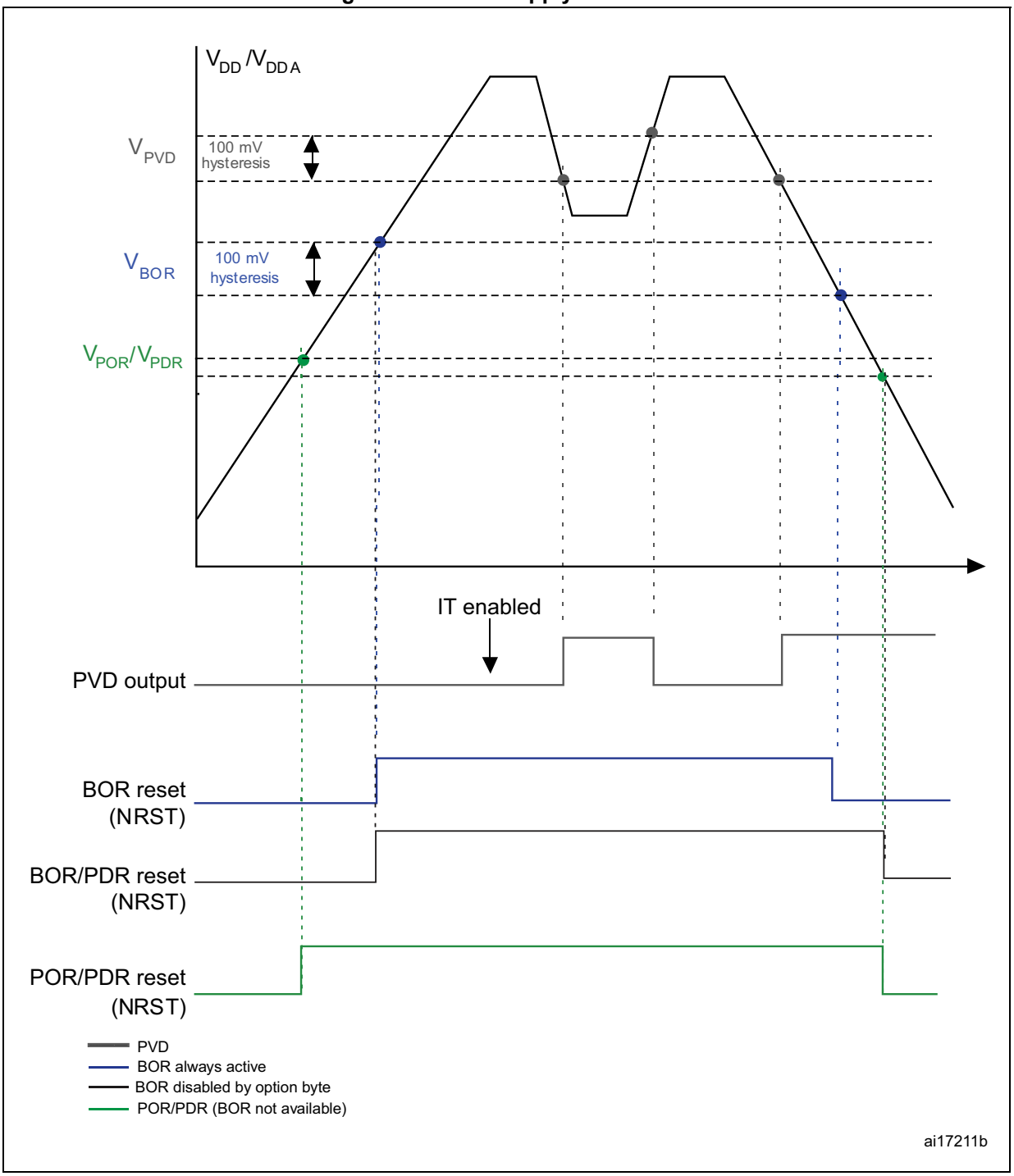
1. $f_{SYSCLK} = f_{CPU}$
2. 1.8 V at power-up, 1.65 V at power-down if BOR is disabled by option byte
3. To calculate $P_{Dmax}(T_A)$, use the formula $P_{Dmax}=(T_{Jmax} - T_A)/\Theta_{JA}$ with T_{Jmax} in this table and Θ_{JA} in “Thermal characteristics” table.
4. T_{Jmax} is given by the test limit. Above this value the product behavior is not guaranteed.

9.3.2 Embedded reset and power control block characteristics

Table 19. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{VDD}	V_{DD} rise time rate	BOR detector enabled	0(1)	-	∞(1)	µs/V
		BOR detector disabled	0(1)	-	1(1)	ms/V
	V_{DD} fall time rate	BOR detector enabled	20(1)	-	∞(1)	µs/V
		BOR detector disabled	Reset below voltage functional range			
t_{TEMP}	Reset release delay	V_{DD} rising BOR detector enabled	-	3	-	ms
		V_{DD} rising BOR detector disabled	-	1	-	
V_{POR}	Power-on reset threshold	Rising edge	1.3(2)	1.5	1.65	V
V_{PDR}	Power-down reset threshold	Falling edge	1.3(2)	1.5	1.65	
V_{BOR0}	Brown-out reset threshold 0 (BOR_TH[2:0]=000)	Falling edge	1.67	1.7	1.74	
		Rising edge	1.69	1.75	1.80	
V_{BOR1}	Brown-out reset threshold 1 (BOR_TH[2:0]=001)	Falling edge	1.87	1.93	1.97	
		Rising edge	1.96	2.04	2.07	
V_{BOR2}	Brown-out reset threshold 2 (BOR_TH[2:0]=010)	Falling edge	2.22	2.3	2.35	
		Rising edge	2.31	2.41	2.44	
V_{BOR3}	Brown-out reset threshold 3 (BOR_TH[2:0]=011)	Falling edge	2.45	2.55	2.60	
		Rising edge	2.54	2.66	2.7	
V_{BOR4}	Brown-out reset threshold 4 (BOR_TH[2:0]=100)	Falling edge	2.68	2.80	2.85	
		Rising edge	2.78	2.90	2.95	

Figure 13. Power supply thresholds



9.3.3 Supply current characteristics

Total current consumption

The MCU is placed under the following conditions:

- All I/O pins in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except if explicitly mentioned.

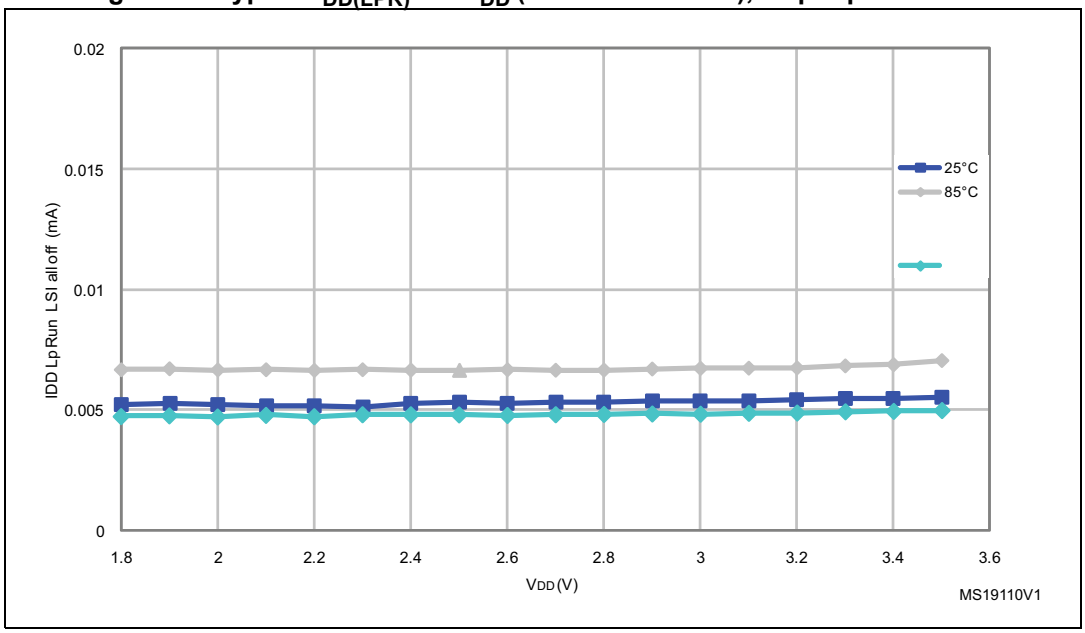
In the following table, data are based on characterization results, unless otherwise specified.

Subject to general operating conditions for V_{DD} and T_A.

Table 20. Total current consumption in Run mode

Symbol	Para meter	Conditions(1)			Typ.	Max.				Unit
						55°C	85 °C (2)	105 °C (3)	125 °C (4)	
$I_{DD(RUN)}$	Supply current in run mode (5)	All peripherals OFF, code executed from RAM, V_{DD} from 1.65 V to 3.6 V	HSI RC osc. (16 MHz)(6)	f_{CPU} = 125 kHz	0.22	0.28	0.39	0.47	0.51	mA
				f_{CPU} = 1 MHz	0.32	0.38	0.49	0.57	0.61	
				f_{CPU} = 4 MHz	0.59	0.65	0.76	0.84	0.88	
				f_{CPU} = 8 MHz	0.93	0.99	1.1	1.18	1.22	
				f_{CPU} = 16 MHz	1.62	1.68	1.79(7)	1.87(7)	1.91(7)	
			HSE external clock (f_{CPU}=f_{HSE}) (8)	f_{CPU} = 125 kHz	0.21	0.25	0.35	0.44	0.49	
				f_{CPU} = 1 MHz	0.3	0.34	0.44	0.53	0.58	
				f_{CPU} = 4 MHz	0.57	0.61	0.71	0.8	0.85	
				f_{CPU} = 8 MHz	0.95	0.99	1.09	1.18	1.23	
				f_{CPU} = 16 MHz	1.73	1.77	1.87(7)	1.96(7)	2.01(7)	
			LSI RC osc. (typ. 38 kHz)	f_{CPU} = f_{LSI}	0.029	0.035	0.039	0.044	0.055	
			LSE external clock (32.768 kHz)	f_{CPU} = f_{LSE}	0.028	0.034	0.038	0.042	0.054	

Figure 18. Typical $I_{DD(LPR)}$ vs. V_{DD} (LSI clock source), all peripherals OFF



5. Data based on a differential I_{DD} measurement between DAC in reset configuration and continuous DAC conversion of V_{DD} /2. Floating DAC output.
6. Data based on a differential I_{DD} measurement between COMP1 or COMP2 in reset configuration and COMP1 or COMP2 enabled with static inputs. Supply current of internal reference voltage excluded.
7. Including supply current of internal reference voltage.

Table 28. Current consumption under external reset

Symbol	Parameter	Conditions		Typ.	Unit
$I_{DD(RST)}$	Supply current under external reset (1)	PB1/PB3/PA5 pins are externally tied to V_{DD}	V_{DD} = 1.8 V	48	µA
			V_{DD} = 3 V	80	
			V_{DD} = 3.6 V	95	

1. All pins except PA0, PB0 and PB4 are floating under reset. PA0, PB0 and PB4 are configured with pull-up under reset. PB1, PB3 and PA5 must be tied externally under reset to avoid the consumption due to their schmitt trigger.

9.3.4 Clock and timing characteristics

HSE external clock (HSEBYP = 1 in CLK_ECKCR)

Subject to general operating conditions for V_{DD} and T_A.

Table 29. HSE external clock characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{HSE_ext} (1)	External clock source frequency		1		16	MHz
V_{HSEH}	OSC_IN input pin high level voltage		0.7 x V_{DD}		V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}		0.3 x V_{DD}	
$C_{in(HSE)}$ (1)	OSC_IN input capacitance			2.6		pF
I_{LEAK_HSE}	OSC_IN input leakage current	$V_{SS} < V_{IN} < V_{DD}$			±1	µA

1. Guaranteed by design.

Table 42. $\overline{\text{NRST}}$ pin characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{IL(NRST)}$	NRST input low level voltage (1)	-	V_{SS}	-	0.8	V
$V_{IH(NRST)}$	NRST input high level voltage (1)	-	1.4	-	V_{DD}	
$V_{OL(NRST)}$	NRST output low level voltage (1)	I_{OL} = 2 mA 2.7 V ≤V_{DD} ≤3.6 V	-	-	0.4	
		I_{OL} = 1.5 mA V_{DD} < 2.7 V	-	-		
V_{HYST}	NRST input hysteresis(3)	-	10%V_{DD}(2)	-	-	mV
$R_{PU(NRST)}$	NRST pull-up equivalent resistor(1)	-	30	45	60	kΩ
$V_{F(NRST)}$	NRST input filtered pulse (3)	-		-	50	ns
$V_{NF(NRST)}$	NRST input not filtered pulse (3)	-	300	-	-	

1. Data based on characterization results.
2. 200 mV min.
3. Data guaranteed by design.

Figure 36. Typical NRST pull-up resistance R_{PU} vs. V_{DD}

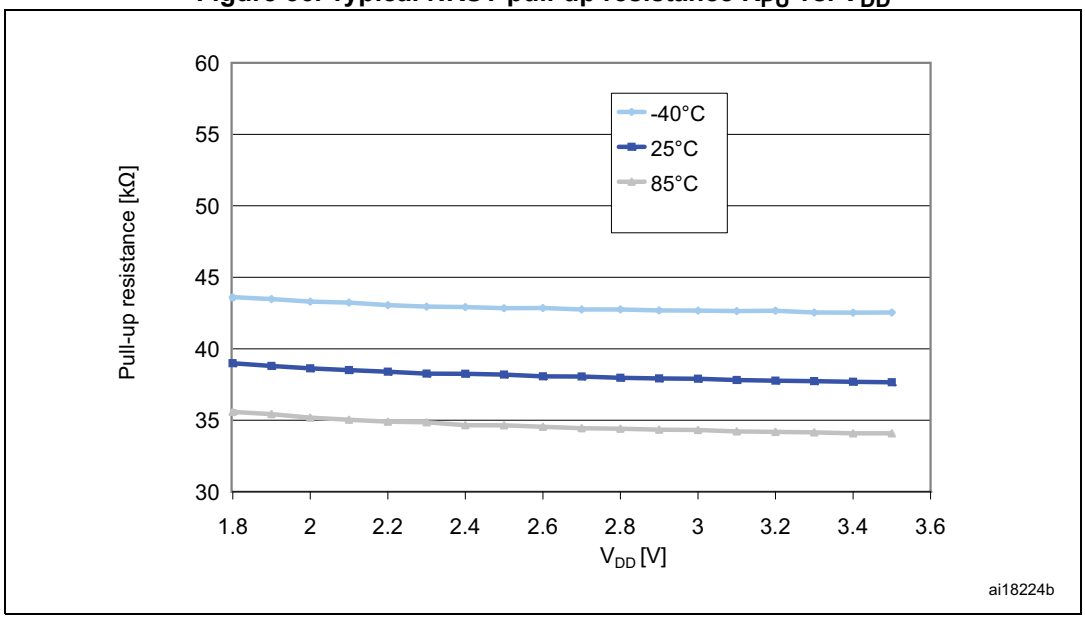
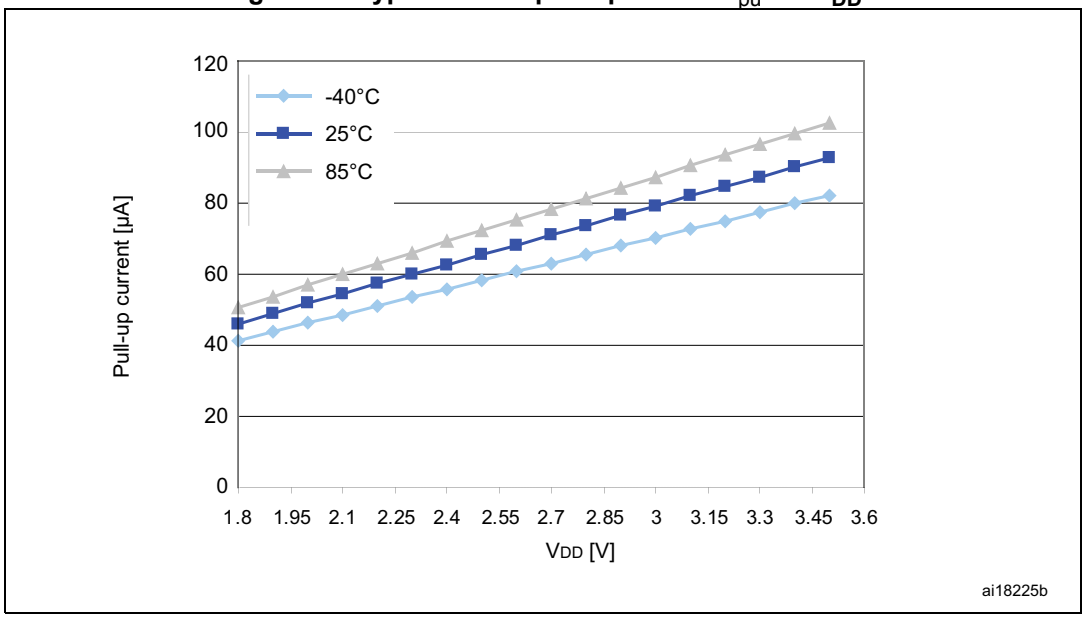


Figure 37. Typical NRST pull-up current I_{pu} vs. V_{DD}



The reset network shown in *Figure 38* protects the device against parasitic resets. The user must ensure that the level on the NRST pin can go below the V_{IL} max. level specified in *Table 42*. Otherwise the reset is not taken into account internally. For power consumption-sensitive applications, the capacity of the external reset capacitor can be reduced to limit the charge/discharge current. If the NRST signal is used to reset the external circuitry, the user must pay attention to the charge/discharge time of the external capacitor to meet the reset timing conditions of the external devices. The minimum recommended capacity is 10 nF.

Figure 38. Recommended NRST pin configuration

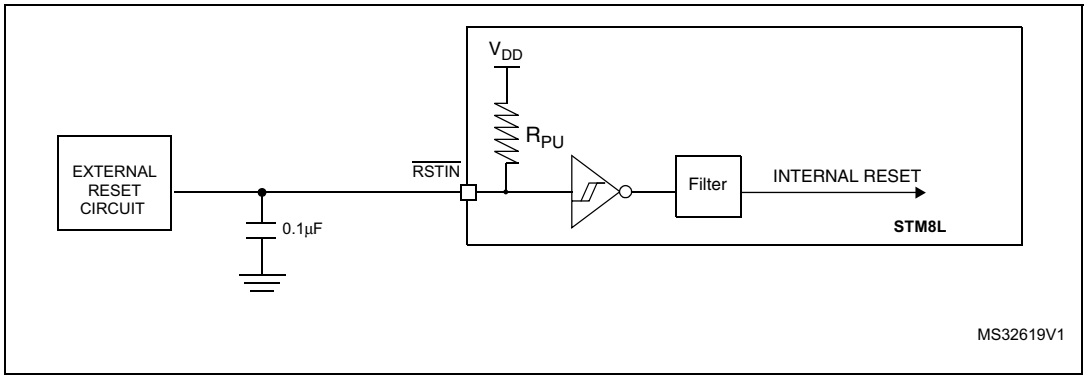
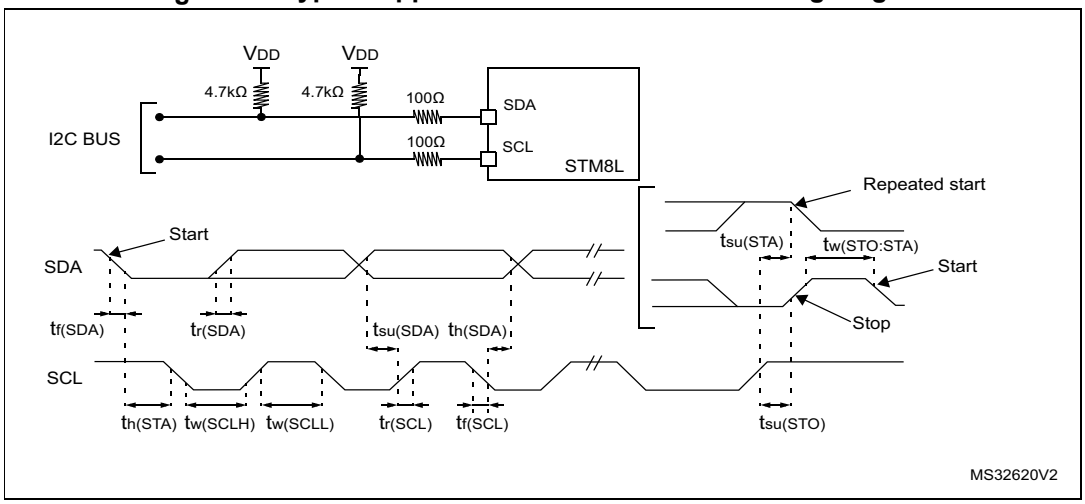


Figure 42. Typical application with I²C bus and timing diagram



1. Measurement points are done at CMOS levels: 0.3 x V_{DD} and 0.7 x V_{DD}

9.3.9 LCD controller (STM8L152x6/8 only)

In the following table, data are guaranteed by design.

Table 45. LCD characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{LCD}	LCD external voltage	-		3.6	V
V_{LCD0}	LCD internal reference voltage 0	-	2.6	-	
V_{LCD1}	LCD internal reference voltage 1	-	2.7	-	
V_{LCD2}	LCD internal reference voltage 2	-	2.8	-	
V_{LCD3}	LCD internal reference voltage 3	-	3.0	-	
V_{LCD4}	LCD internal reference voltage 4	-	3.1	-	
V_{LCD5}	LCD internal reference voltage 5	-	3.2	-	
V_{LCD6}	LCD internal reference voltage 6	-	3.4	-	
V_{LCD7}	LCD internal reference voltage 7	-	3.5	-	
C_{EXT}	V_{LCD} external capacitance	0.1	1	2	µF
I_{DD}	Supply current(1) at V_{DD} = 1.8 V	-	3	-	µA
	Supply current(1) at V_{DD} = 3 V	-	3	-	
R_{HN}(2)	High value resistive network (low drive)	-	6.6	-	MΩ
R_{LN}(3)	Low value resistive network (high drive)	-	240	-	kΩ
V_{33}	Segment/Common higher level voltage	-		V_{LCDx}	V
V_{34}	Segment/Common 3/4 level voltage	-	$3/4V_{LCDx}$	-	
V_{23}	Segment/Common 2/3 level voltage	-	$2/3V_{LCDx}$	-	
V_{12}	Segment/Common 1/2 level voltage	-	$1/2V_{LCDx}$	-	
V_{13}	Segment/Common 1/3 level voltage	-	$1/3V_{LCDx}$	-	
V_{14}	Segment/Common 1/4 level voltage	-	$1/4V_{LCDx}$	-	
V_0	Segment/Common lowest level voltage	0	-	-	

1. LCD enabled with 3 V internal booster (LCD_CR1 = 0x08), 1/4 duty, 1/3 bias, division ratio= 64, all pixels active, no LCD connected.
2. R_{HN} is the total high value resistive network.
3. R_{LN} is the total low value resistive network.

VLCD external capacitor (STM8L152x6/8 only)

The application can achieve a stabilized LCD reference voltage by connecting an external capacitor C_{EXT} to the V_{LCD} pin. C_{EXT} is specified in *Table 45*.

Table 65. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Table 67. WLCSP32 - 32-ball, 1.913 x 3.329 mm, 0.4 mm pitch wafer level chip scale package mechanical data(1)

Symbol	millimeters			inches(2)		
	Min	Typ	Max	Min	Typ	Max
A	0.525	0.555	0.585	0.0207	0.0219	0.0230
A1	-	0.175	-	-	0.0069	-
A2	-	0.380	-	-	0.0150	-
A3(3)	-	0.025	-	-	0.0010	-
b(4)	0.220	0.250	0.280	0.0087	0.0098	0.0110
D	1.878	1.913	1.948	0.0739	0.0753	0.0767
E	3.294	3.329	3.364	0.1297	0.1311	0.1324
e	-	0.400	-	-	0.0157	-
e1	-	1.200	-	-	0.0472	-
e2	-	2.800	-	-	0.1102	-
F	-	0.3565	-	-	0.0140	-
G	-	0.2645	-	-	0.0104	-
aaa	-	-	0.100	-	-	0.0039
bbb	-	-	0.100	-	-	0.0039
ccc	-	-	0.100	-	-	0.0039
ddd	-	-	0.050	-	-	0.0020
eee	-	-	0.050	-	-	0.0020

1. Preliminary data.
2. Values in inches are converted from mm and rounded to 4 decimal digits.
3. Back side coating.
4. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

Figure 61. WLCSP32 - 32-ball, 1.913 x 3.329 mm, 0.4 mm pitch wafer level chip scale package recommended footprint

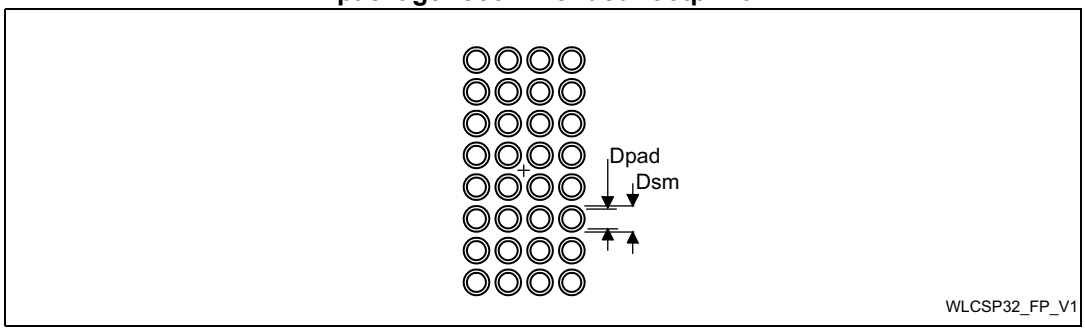


Table 70. Document revision history (continued)

Date	Revision	Changes
03-Apr-2013	5	Updated capacitive sensing channels and “Dynamic consumption” in *Features* Updated LCD feature in *Table 2: High-density and medium+ density STM8L15xx6/8 low power device features and peripheral counts* Updated Halt mode definition in *Section 3.1: Low-power modes* Added *Bootloader* Updated *Section 3.12: System configuration controller and routing interface* Added *Section 3.13: Touch sensing* *Table 5: High-density and medium+ density STM8L15x pin description*: updated NRST/PA1, PI0, PI1, PI2, PE0, PE1, PE2, PF4, PF5, PF6, PF7, footnote *1.* and added *Note:* Updated ‘0x00 502E to 0x00 5049’ reserved area in *Table 9: General hardware register map* Updated reference to SWIM/DEBUG manual in *Section 7: Option bytes* Updated BOR factory default settings to 0x00 in *Table 12: Option byte addresses* Corrected ROP option byte value in *Table 12: Option byte addresses* Added *Figure 45: Maximum dynamic current consumption on VREF+ supply pin during ADC conversion* Updated STABVREFINT max value in *Table 46: Reference voltage characteristics* Updated *Figure 41: SPI1 timing diagram - master mode* Added *Table 57: RAIN max for fADC = 16 MHz* Updated Max DAC_OUT in *Table 50: DAC characteristics* Updated *Section 9.3.12: Comparator characteristics*
31-Jul-2013	6	Added ‘Top view’ footnotes under the pinout figures in *Section 4: Pin description* Updated the PF4-PF7 pins for the LQFP80 in *Table 5: High-density and medium+ density STM8L15x pin description* Updated all packages: Updated *Figure 57: UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline* and *Table 65: LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data* Added *Figure 49: LQFP80 - 80-pin, 14 x 14 mm low-profile quad flat package recommended footprint* Added ‘tape and reel’ in *Table 69: Ordering information scheme*