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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, IR, LCD, POR, PWM, WDT
Number of I/O	54
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 28x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8l152r6t6

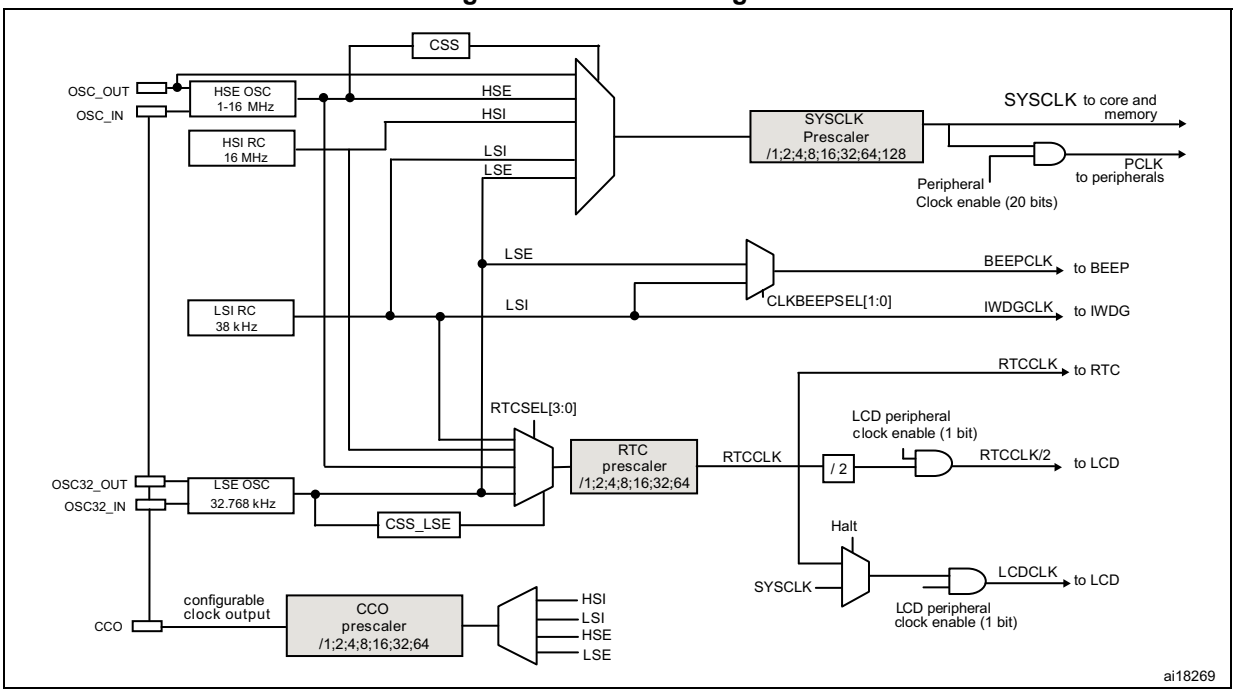
2.2 Device overview

Table 2. High-density and medium+ density STM8L15xx6/8 low power device features and peripheral counts

Features		STM8L15xC8	STM8L15xK8	STM8L15xR8	STM8L15xM8	STM8L15xR6
Flash (Kbyte)		64	64	64	64	32
Data EEPROM (Kbyte)		2	2	2	2	1
RAM (Kbyte)		4	4	4	4	2
LCD		8x24 or 4x28(1)	4x15(1)	8x36 or 4x40(1)	8x40 or 4x44(1)	8x36 or 4x40(1)
Timers	Basic	1 (8-bit)	1 (8-bit)	1 (8-bit)	1 (8-bit)	1 (8-bit)
	General purpose	3 (16-bit)	3 (16-bit)	3 (16-bit)	3 (16-bit)	3 (16-bit)
	Advanced control	1 (16-bit)	1 (16-bit)	1 (16-bit)	1 (16-bit)	1 (16-bit)
Communication interfaces	SPI	2	1	2	2	2
	I2C	1	1	1	1	1
	USART	3	2	3	3	3
GPIOs		41(2)	28(2)	54(2)	68(2)	54(2)
12-bit synchronized ADC (number of channels)		1 (25)	1 (18)	1 (28)	1 (28)	1 (28)
12-Bit DAC Number of channels		2 2	1 1	2 2	2 2	2 2
Comparators (COMP1/COMP2)		2	2	2	2	2
Others		RTC, window watchdog, independent watchdog, 16-MHz and 38-kHz internal RC, 1- to 16-MHz and 32-kHz external oscillator				
CPU frequency		16 MHz				
Operating voltage		1.8 to 3.6 V (down to 1.65 V at power-down) with BOR 1.65 to 3.6 V without BOR				
Operating temperature		–40 to +85 °C / –40 to +105 °C / –40 to +125 °C				
Packages		UFQFPN48 LQFP48	WLCSP32	LQFP64	LQFP80	LQFP64

1. STM8L152x6/8 versions only.
2. The number of GPIOs given in this table includes the NRST/PA1 pin but the application can use the NRST/PA1 pin as general purpose output only (PA1).

Figure 2. Clock tree diagram



3.5 Low-power real-time clock

The real-time clock (RTC) is only available on STM8L151xx and STM8L152xx devices.

The real-time clock (RTC) is an independent binary coded decimal (BCD) timer/counter.

Six byte locations contain the second, minute, hour (12/24 hour), week day, date, month, year, in BCD (binary coded decimal) format. Correction for 28, 29 (leap year), 30, and 31 day months are made automatically. The subsecond field can also be read in binary format.

The calendar can be corrected from 1 to 32767 RTC clock pulses. This allows to make a synchronization to a master clock.

The RTC offers a digital calibration which allows an accuracy of +/-0.5 ppm.

It provides a programmable alarm and programmable periodic interrupts with wakeup from Halt capability.

- Periodic wakeup time using the 32.768 kHz LSE with the lowest resolution (of 61 µs) is from min. 122 µs to max. 3.9 s. With a different resolution, the wakeup time can reach 36 hours
- Periodic alarms based on the calendar can also be generated from LSE period to every year

A clock security system detects a failure on LSE, and can provide an interrupt with wakeup capability. The RTC clock can automatically switch to LSI in case of LSE failure.

The RTC also provides 3 anti-tamper detection pins. This detection embeds a programmable filter and can wakeup the MCU.

3.6 LCD (Liquid crystal display)

The LCD is only available on STM8L152x6/8 devices.

The liquid crystal display drives up to 8 common terminals and up to 40 segment terminals to drive up to 320 pixels. It can also be configured to drive up to 4 common and 44 segments (up to 176 pixels).

- Internal step-up converter to guarantee contrast control whatever V_{DD}.
- Static 1/2, 1/3, 1/4, 1/8 duty supported.
- Static 1/2, 1/3, 1/4 bias supported.
- Phase inversion to reduce power consumption and EMI.
- Up to 8 pixels which can programmed to blink.
- The LCD controller can operate in Halt mode.

Note: Unnecessary segments and common pins can be used as general I/O pins.

3.7 Memories

The high-density and medium+ density STM8L15xx6/8 devices have the following main features:

- Up to 4 Kbyte of RAM
- The non-volatile memory is divided into three arrays:
  - Up to 64 Kbyte of medium-density embedded Flash program memory
  - Up to 2 Kbyte of Data EEPROM
  - Option bytes.

The EEPROM embeds the error correction code (ECC) feature. It supports the read-while-write (RWW): it is possible to execute the code from the program matrix while programming/erasing the data matrix.

The option byte protects part of the Flash program memory from write and readout piracy.

3.8 DMA

A 4-channel direct memory access controller (DMA1) offers a memory-to-memory and peripherals-from/to-memory transfer capability. The 4 channels are shared between the following IPs with DMA capability: ADC1, DAC1,DAC2, I2C1, SPI1, SPI2, USART1, USART2, USART3, and the 5 Timers.

3.9 Analog-to-digital converter

- 12-bit analog-to-digital converter (ADC1) with 28 channels (including 4 fast channel), temperature sensor and internal reference voltage
- Conversion time down to 1 µs with f_{SYSCLK}= 16 MHz
- Programmable resolution
- Programmable sampling time
- Single and continuous mode of conversion
- Scan capability: automatic conversion performed on a selected group of analog inputs
- Analog watchdog: interrupt generation when the converted voltage is outside the programmed threshold
- Triggered by timer

Note: ADC1 can be served by DMA1.

3.10 Digital-to-analog converter

- 12-bit DAC with 2 buffered outputs (two digital signals can be converted into two analog voltage signal outputs)
- Synchronized update capability using timers
- DMA capability for each channel
- External triggers for conversion
- Noise-wave generation
- Triangular-wave generation
- Dual DAC channels with independent or simultaneous conversions
- Input reference voltage V_{REF+} for better resolution

Note: DAC can be served by DMA1.

3.11 Ultra-low-power comparators

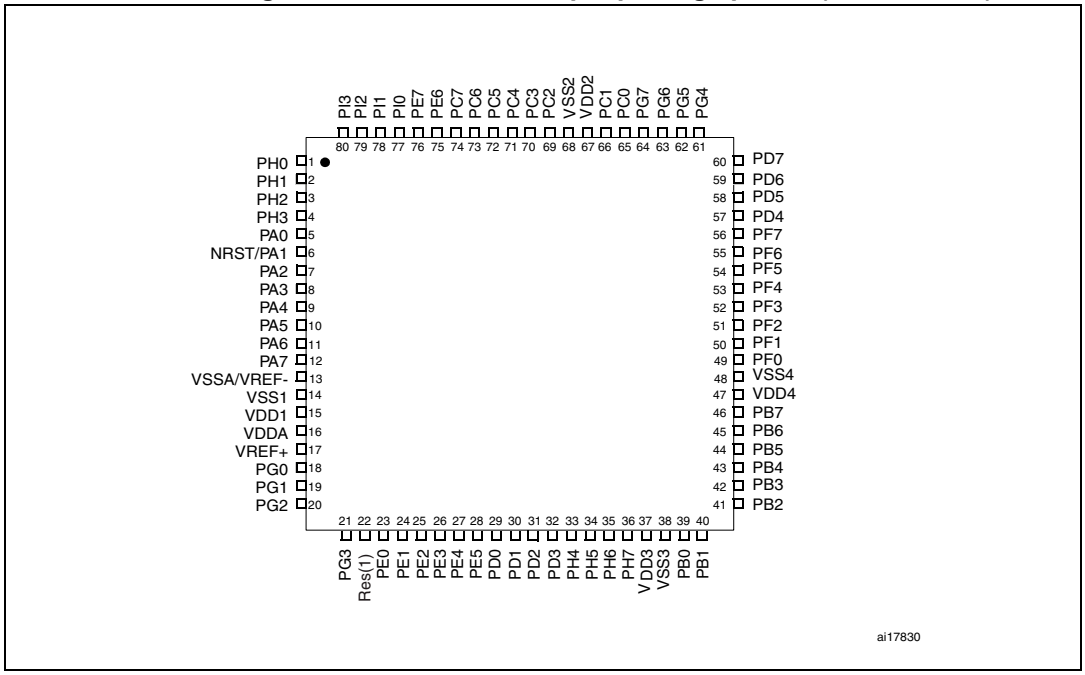
The high-density and medium+ density STM8L15xx6/8 devices embed two comparators (COMP1 and COMP2) sharing the same current bias and voltage reference. The voltage reference can be internal or external (coming from an I/O).

- One comparator with fixed threshold (COMP1).
- One comparator rail to rail with fast or slow mode (COMP2). The threshold can be one of the following:
  - DAC output
  - External I/O
  - Internal reference voltage or internal reference voltage submultiple (1/4, 1/2, 3/4)

The two comparators can be used together to offer a window function. They can wake up from Halt mode.

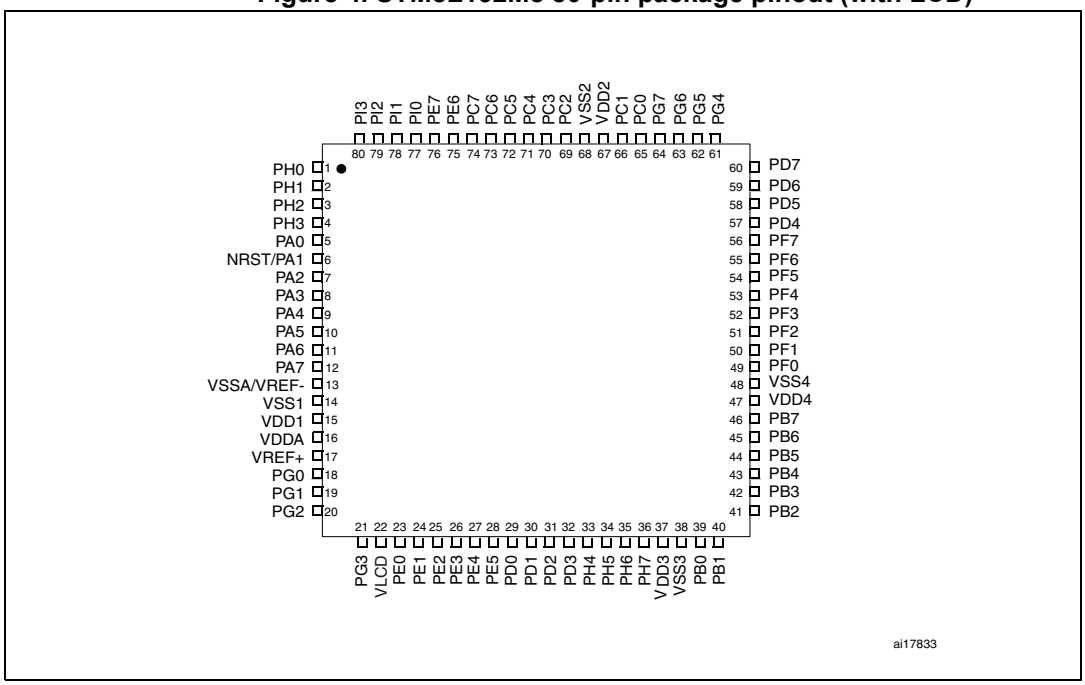
4 Pin description

Figure 3. STM8L151M8 80-pin package pinout (without LCD)



1. Pin 22 is reserved and must be tied to V_{DD}.
2. The above figure shows the package top view.

Figure 4. STM8L152M8 80-pin package pinout (with LCD)



1. The above figure shows the package top view.

In the following table, data are based on characterization results, unless otherwise specified.

Table 22. Total current consumption and timing in Low-power run mode at V_{DD} = 1.65 V to 3.6 V

Symbol	Parameter	Conditions[1]			Typ.	Max.	Unit
$I_{DD(LPR)}$	Supply current in Low-power run mode	LSI RC osc. (at 38 kHz)	all peripherals OFF	T_A = -40 °C to 25 °C	5.86	6.38	µA
				T_A = 55 °C	6.52	7.06	
				T_A = 85 °C	7.68	8.7	
				T_A = 105 °C	10.14	11.77	
				T_A = 125 °C	14.4	18.27	
			with TIM2 active[2]	T_A = -40 °C to 25 °C	6.2	6.73	
				T_A = 55 °C	6.86	7.41	
				T_A = 85 °C	9.71	10.81	
				T_A = 105 °C	13.17	15.39	
				T_A = 125 °C	16.72	21.1	
		LSE [3] external clock (32.768 kHz)	all peripherals OFF	T_A = -40 °C to 25 °C	5.42	5.94	
				T_A = 55 °C	5.9	6.52	
				T_A = 85 °C	6.14	6.8	
				T_A = 105 °C	7.46	8.2	
				T_A = 125 °C	10.25	12.81	
			with TIM2 active [2]	T_A = -40 °C to 25 °C	5.87	6.48	
				T_A = 55 °C	6.44	6.95	
				T_A = 85 °C	6.7	7.65	
				T_A = 105 °C	8.01	9.15	
				T_A = 125 °C	10.62	16.09	

1. No floating I/Os
2. Timer 2 clock enabled and counter running
3. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD\ LSE}$) must be added. Refer to *Table 32*

In the following table, data are based on characterization results, unless otherwise specified.

Table 24. Total current consumption and timing in Active-halt mode at V_{DD} = 1.65 V to 3.6 V

Symbol	Parameter	Conditions[1]			Typ.	Max.	Unit
$I_{DD(AH)}$	Supply current in Active-halt mode	LSI RC (at 38 kHz)	LCD OFF[2]	T_A = -40 °C to 25 °C	0.92	2.25	µA
				T_A = 55 °C	1.32	3.44	
				T_A = 85 °C	1.63	3.87	
				T_A = 105 °C	3	7.94	
				T_A = 125 °C	5.6	13.8	
			LCD ON (static duty/ external V_{LCD}) [3]	T_A = -40 °C to 25 °C	1.56	3.6	
				T_A = 55 °C	1.64	3.8	
				T_A = 85 °C	2.12	5.03	
				T_A = 105 °C	3.34	8.2	
				T_A = 125 °C	5.83	14.4	
			LCD ON (1/4 duty/ external V_{LCD}) [4]	T_A = -40 °C to 25 °C	1.92	4.56	
				T_A = 55 °C	2.1	4.97	
				T_A = 85 °C	2.6	6.14	
				T_A = 105 °C	3.62	8.49	
				T_A = 125 °C	6.1	15.92	
			LCD ON (1/4 duty/ internal V_{LCD}) [5]	T_A = -40 °C to 25 °C	4.2	9.88	
				T_A = 55 °C	4.39	10.32	
				T_A = 85 °C	4.84	11.5	
				T_A = 105 °C	5.98	15	
				T_A = 125 °C	7.21	18.07	

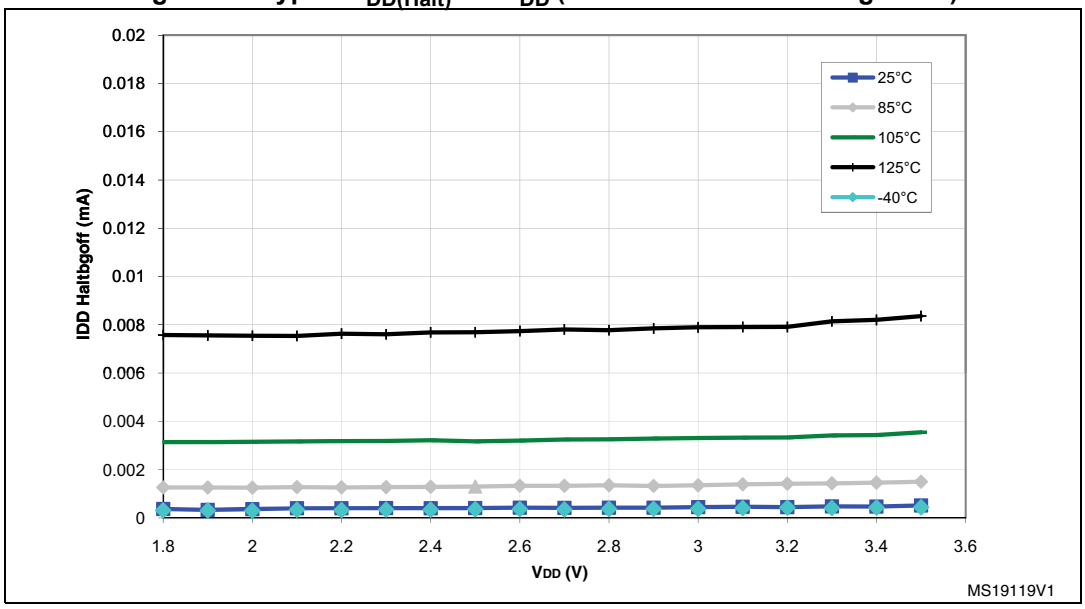
In the following table, data are based on characterization results, unless otherwise specified.

Table 26. Total current consumption and timing in Halt mode at V_{DD} = 1.65 to 3.6 V

Symbol	Parameter	Condition(1)	Typ.	Max.	Unit
$I_{DD(Halt)}$	Supply current in Halt mode (Ultra-low-power ULP bit =1 in the PWR_CSR2 register)	T_A = -40 °C to 25 °C	400	1600(2)	nA
		T_A = 55 °C	810	2400	
		T_A = 85 °C	1600	4500(2)	
		T_A = 105 °C	2900	7700(2)	
		T_A = 125 °C	5.6	18(2)	µA
$I_{DD(WUHalt)}$	Supply current during wakeup time from Halt mode (using HSI)		2.4		mA
$t_{WU\_HSI(Halt)}$(3)(4)	Wakeup time from Halt to Run mode (using HSI)		4.7	7	µs
$t_{WU\_LSI(Halt)}$(3)(4)	Wakeup time from Halt mode to Run mode (using LSI)		150		µs

1. T_A = -40 to 125 °C, no floating I/O, unless otherwise specified
2. Tested in production
3. ULP=0 or ULP=1 and FWU=1 in the PWR_CSR2 register
4. Wakeup time until start of interrupt vector fetch.
   The first word of interrupt routine is fetched 4 CPU cycles after t_{WU}

Figure 21. Typical $I_{DD(Halt)}$ vs. V_{DD} (internal reference voltage OFF)



Current consumption of on-chip peripherals

Table 27. Peripheral current consumption

Symbol	Parameter		Typ. V_{DD} = 3.0 V	Unit
$I_{DD(TIM1)}$	TIM1 supply current(1)		10	µA/MHz
$I_{DD(TIM2)}$	TIM2 supply current (1)		7	
$I_{DD(TIM3)}$	TIM3 supply current (1)		7	
$I_{DD(TIM5)}$	TIM5 supply current (1)		7	
$I_{DD(TIM4)}$	TIM4 timer supply current (1)		3	
$I_{DD(USART1)}$	USART1 supply current (2)		5	
$I_{DD(USART2)}$	USART2 supply current (2)		5	
$I_{DD(USART3)}$	USART3 supply current (2)		5	
$I_{DD(SPI1)}$	SPI1 supply current (2)		3	
$I_{DD(SPI2)}$	SPI2 supply current (2)		3	
$I_{DD(I2C1)}$	I^2C1 supply current (2)		4	
$I_{DD(DMA1)}$	DMA1 supply current(2)		3	
$I_{DD(WWDG)}$	WWDG supply current(2)		1	
$I_{DD(ALL)}$	Peripherals ON(3)		63	
$I_{DD(ADC1)}$	ADC1 supply current(4)		1500	µA
$I_{DD(DAC)}$	DAC supply current(5)		370	
$I_{DD(COMP1)}$	Comparator 1 supply current(6)		0.160	
$I_{DD(COMP2)}$	Comparator 2 supply current(6)	Slow mode	2	
		Fast mode	5	
$I_{DD(PVD/BOR)}$	Power voltage detector and brownout Reset unit supply current (7)		2.6	
$I_{DD(BOR)}$	Brownout Reset unit supply current (7)		2.4	
$I_{DD(IDWDG)}$	Independent watchdog supply current	including LSI supply current	0.45	
		excluding LSI supply current	0.05	

1. Data based on a differential I_{DD} measurement between all peripherals OFF and a timer counter running at 16 MHz. The CPU is in Wait mode in both cases. No IC/OC programmed, no I/O pins toggling. Not tested in production.
2. Data based on a differential I_{DD} measurement between the on-chip peripheral in reset configuration and not clocked and the on-chip peripheral when clocked and not kept under reset. The CPU is in Wait mode in both cases. No I/O pins toggling. Not tested in production.
3. Peripherals listed above the $I_{DD(ALL)}$ parameter ON: TIM1, TIM2, TIM3, TIM4, TIM5, USART1, USART2, USART3, SPI1, SPI2, I2C1, DMA1, WWDG.
4. Data based on a differential I_{DD} measurement between ADC in reset configuration and continuous ADC conversion.

Flash memory

Table 36. Flash program and data EEPROM memory

Symbol	Parameter	Conditions	Min.	Typ.	Max. (1)	Unit
V_{DD}	Operating voltage (all modes, read/write/erase)	f_{SYSCLK} = 16 MHz	1.65		3.6	V
t_{prog}	Programming time for 1 or 128 bytes (block) erase/write cycles (on programmed byte)	-	-	6	-	ms
	Programming time for 1 to 128 bytes (block) write cycles (on erased byte)	-	-	3	-	
I_{prog}	Programming/ erasing consumption	T_A=+25 °C, V_{DD} = 3.0 V	-	0.7	-	mA
		T_A=+25 °C, V_{DD} = 1.8 V	-		-	
t_{RET} (2)	Data retention (program memory) after 10000 erase/write cycles at T_A=-40 to +85 °C (6 suffix)	T_{RET}=+85 °C	30(1)	-	-	years
	Data retention (program memory) after 10000 erase/write cycles at T_A=-40 to +125 °C (3 suffix)	T_{RET}=+125 °C	5(1)	-	-	
	Data retention (data memory) after 300000 erase/write cycles at T_A=-40 to +85 °C (6 suffix)	T_{RET}=+85 °C	30(1)	-	-	
	Data retention (data memory) after 300000 erase/write cycles at T_A=-40 to +125 °C (3 suffix)	T_{RET}=+125 °C	5(1)	-	-	
N_{RW} (3)	Erase/write cycles (program memory)	T_A=-40 to +85 °C (6 suffix), T_A=-40 to +105 °C (7 suffix) or T_A=-40 to +125 °C (3 suffix)	10(1)	-	-	kcycles
	Erase/write cycles (data memory)		300(1) (4)	-	-	

1. Data based on characterization results.
2. Conforming to JEDEC JESD22a117
3. The physical granularity of the memory is 4 bytes, so cycling is performed on 4 bytes even when a write/erase operation addresses a single byte.
4. Data based on characterization performed on the whole data memory.

Table 38. I/O static characteristics

Symbol	Parameter	Conditions(1)	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage(2)	Input voltage on true open-drain pins (PC0 and PC1)	V_{SS}-0.3	-	0.3 x V_{DD}	V
		Input voltage on five-volt tolerant (FT) pins	V_{SS}-0.3	-	0.3 x V_{DD}	
		Input voltage on any other pin	V_{SS}-0.3	-	0.3 x V_{DD}	
V_{IH}	Input high level voltage (2)	Input voltage on true open-drain pins (PC0 and PC1) with V_{DD} < 2 V	0.70 x V_{DD}	-	5.2	V
		Input voltage on true open-drain pins (PC0 and PC1) with $V_{DD} \geq 2$ V		-	5.5	
		Input voltage on five-volt tolerant (FT) pins with V_{DD} < 2 V	0.70 x V_{DD}	-	5.2	
		Input voltage on five-volt tolerant (FT) pins with $V_{DD} \geq 2$ V		-	5.5	
		Input voltage on any other pin	0.70 x V_{DD}	-	V_{DD}+0.3	
V_{hys}	Schmitt trigger voltage hysteresis (3)	Standard I/Os	-	200	-	mV
		True open drain I/Os	-	200	-	
I_{lkg}	Input leakage current (4)	$V_{SS} \leq V_{IN} \leq V_{DD}$ Standard I/Os	-	-	50 (5)	nA
		$V_{SS} \leq V_{IN} \leq V_{DD}$ True open drain I/Os	-	-	200(5)	
		$V_{SS} \leq V_{IN} \leq V_{DD}$ PA0 with high sink LED driver capability	-	-	200(5)	
R_{PU}	Weak pull-up equivalent resistor(2)(6)	$V_{IN}=V_{SS}$	30	45	60	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. V_{DD} = 3.0 V, T_A = -40 to 125 °C unless otherwise specified.
2. Data based on characterization results.
3. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested.
4. The max. value may be exceeded if negative current is injected on adjacent pins.
5. Not tested in production.
6. R_{PU} pull-up equivalent resistor based on a resistive transistor (corresponding I_{PU} current characteristics described in *Figure 29*).

Figure 30. Typical V_{OL} @ V_{DD} = 3.0 V (high sink ports)

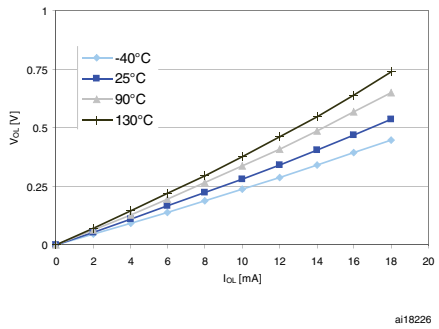


Figure 31. Typical V_{OL} @ V_{DD} = 1.8 V (high sink ports)

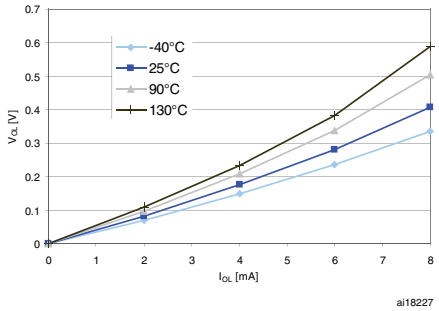


Figure 32. Typical V_{OL} @ V_{DD} = 3.0 V (true open drain ports)

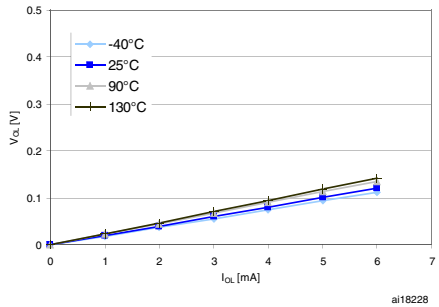


Figure 33. Typical V_{OL} @ V_{DD} = 1.8 V (true open drain ports)

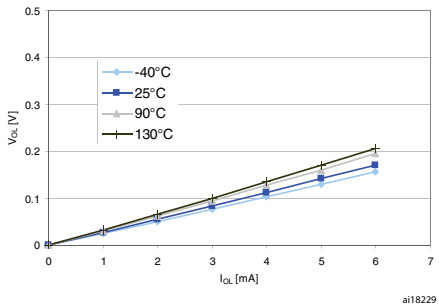


Figure 34. Typical V_{DD} - V_{OH} @ V_{DD} = 3.0 V (high sink ports)

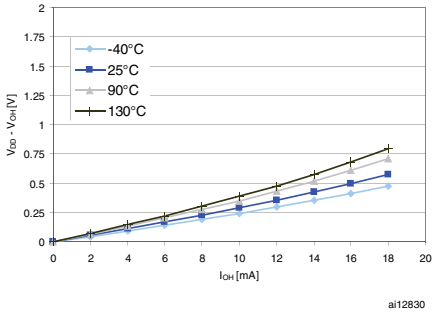
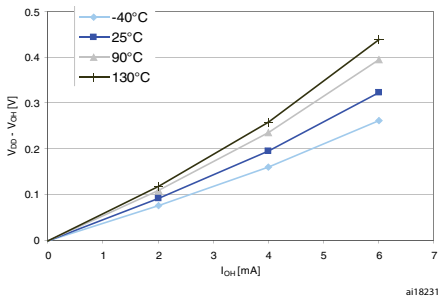


Figure 35. Typical V_{DD} - V_{OH} @ V_{DD} = 1.8 V (high sink ports)



NRST pin

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

In the following table, data based on characterization results.

Table 51. DAC accuracy

Symbol	Parameter	Conditions	Typ.	Max.	Unit
DNL	Differential non linearity(1)	R_L ≥5 kΩ, C_L≤50 pF DACOUT buffer ON(2)	1.5	3	12-bit LSB
		No load DACOUT buffer OFF	1.5	3	
INL	Integral non linearity(3)	R_L ≥5 kΩ, C_L≤ 50 pF DACOUT buffer ON(2)	2	4	
		No load DACOUT buffer OFF	2	4	
Offset	Offset error(4)	R_L ≥5 kΩ, C_L≤ 50 pF DACOUT buffer ON(2)	±10	±25	
		No load DACOUT buffer OFF	±5	±8	
Offset1	Offset error at Code 1 (5)	DACOUT buffer OFF	±1.5	±5	
Gain error	Gain error(6)	R_L ≥5 kΩ, C_L≤ 50 pF DACOUT buffer ON(2)	+0.1/-0.2	+0.2/-0.5	%
		No load DACOUT buffer OFF	+0/-0.2	+0/-0.4	
TUE	Total unadjusted error	R_L ≥5 kΩ, C_L≤ 50 pF DACOUT buffer ON(2)	12	30	12-bit LSB
		No load -DACOUT buffer OFF	8	12	

1. Difference between two consecutive codes - 1 LSB.
2. In 48-pin package devices the DAC2 output buffer must be kept off and no load must be applied on the DAC_OUT2 output.
3. Difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023.
4. Difference between the value measured at Code (0x800) and the ideal value = V_{REF+}/2.
5. Difference between the value measured at Code (0x001) and the ideal value.
6. Difference between the ideal slope of the transfer function and the measured slope computed from Code 0x000 and 0xFFF when buffer is ON, and from Code giving 0.2 V and (V_{DDA} -0.2) V when buffer is OFF.

In the following table, data are guaranteed by design.

Table 52. DAC output on PB4-PB5-PB6(1)

Symbol	Parameter	Conditions	Max	Unit
R_{int}	Internal resistance between DAC output and PB4-PB5-PB6 output	2.7 V < V_{DD} < 3.6 V	1.4	kΩ
		2.4 V < V_{DD} < 3.6 V	1.6	
		2.0 V < V_{DD} < 3.6 V	3.2	
		1.8 V < V_{DD} < 3.6 V	8.2	

1. 32 or 28-pin packages only. The DAC channel can be routed either on PB4, PB5 or PB6 using the routing interface I/O switch registers.

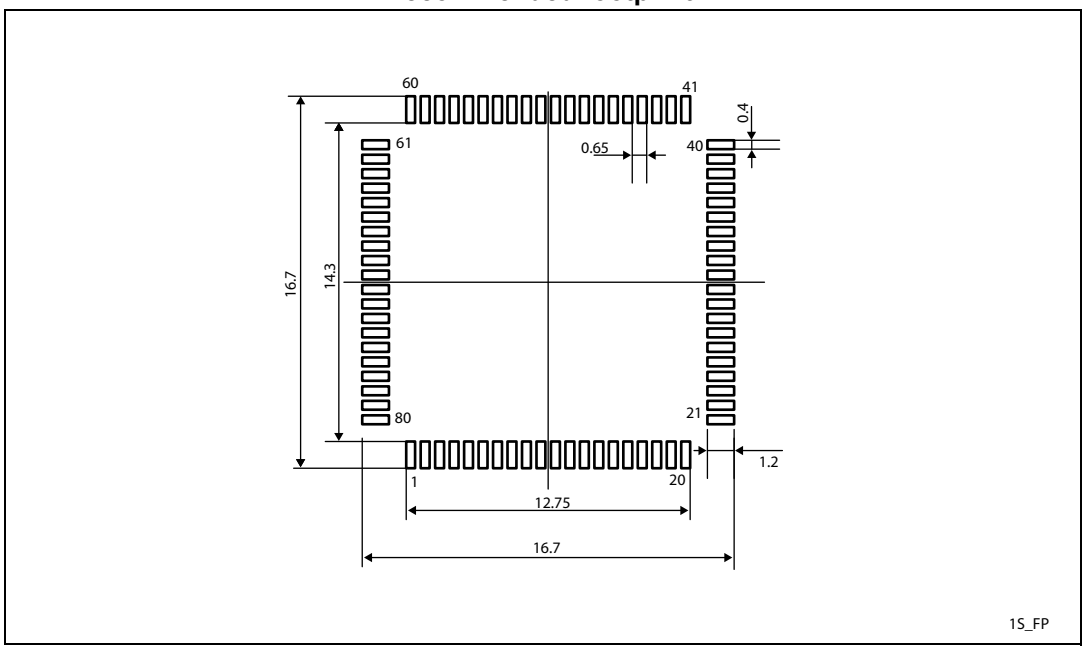
9.3.14 12-bit ADC1 characteristics

In the following table, data are guaranteed by design.

Table 53. ADC1 characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DDA}	Analog supply voltage	-	1.8		3.6	V
V_{REF+}	Reference supply voltage	2.4 V ≤V_{DDA}≤ 3.6 V	2.4		V_{DDA}	V
		1.8 V≤V_{DDA}≤ 2.4 V	V_{DDA}			
V_{REF-}	Lower reference voltage	-	V_{SSA}			
I_{VDDA}	Current on the V_{DDA} input pin	-	-	1000	1450	µA
I_{VREF+}	Current on the V_{REF+} input pin	-	-	400	700 (peak)(1)	
		-	-		450 (average)(1)	
V_{AIN}	Conversion voltage range	-	0(2)	-	V_{REF+}	
T_A	Temperature range	-	-40	-	125	°C
R_{AIN}	External resistance on V_{AIN}	on PF0/1/2/3 fast channels	-	-	50(3)	kΩ
		on all other channels	-	-		
C_{ADC}	Internal sample and hold capacitor	on PF0/1/2/3 fast channels	-	16	-	pF
		on all other channels	-		-	
f_{ADC}	ADC sampling clock frequency	2.4 V≤V_{DDA}≤3.6 V without zooming	0.320	-	16	MHz
		1.8 V≤V_{DDA}≤2.4 V with zooming	0.320	-	8	
f_{CONV}	12-bit conversion rate	V_{AIN} on PF0/1/2/3 fast channels	-	-	1(3)(4)	
		V_{AIN} on all other channels	-	-	760(3)(4)	kHz
f_{TRIG}	External trigger frequency	-	-	-	t_{conv}	$1/f_{ADC}$
t_{LAT}	External trigger latency	-	-	-	3.5	$1/f_{SYSCLK}$

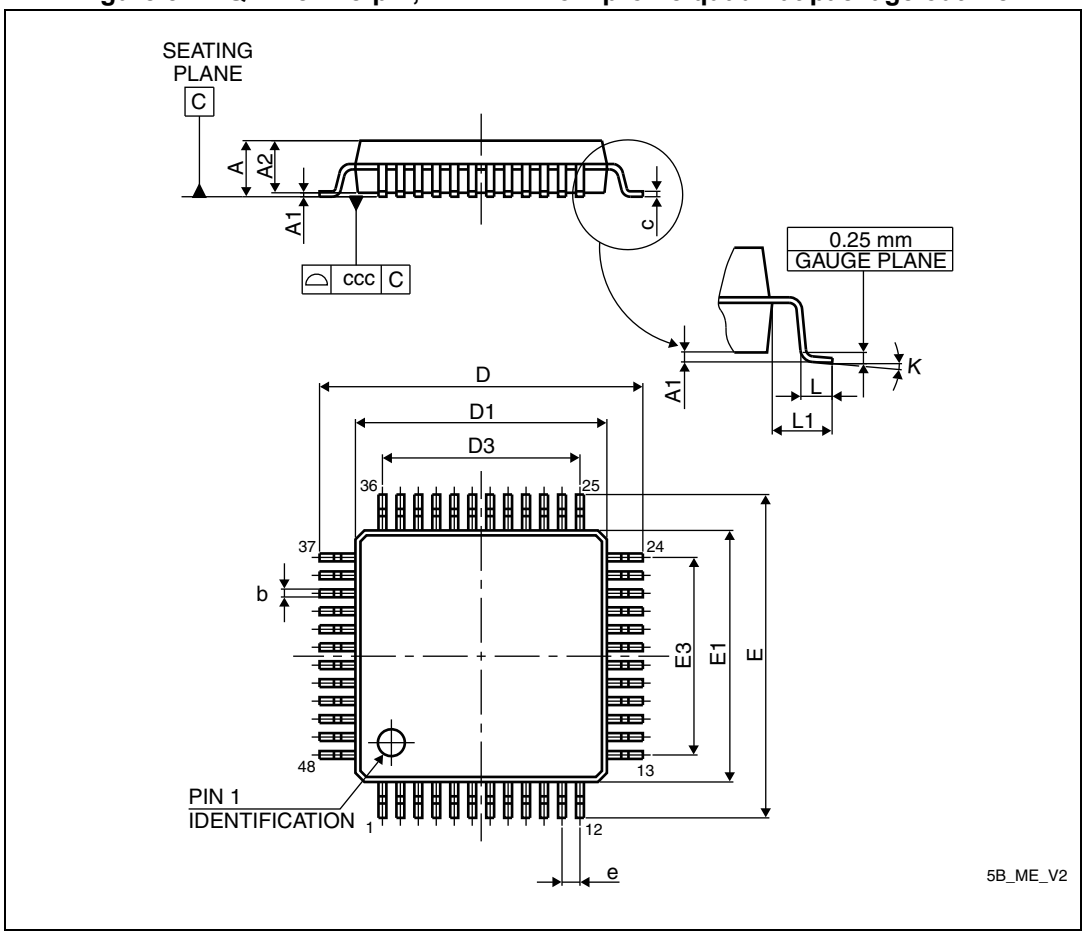
Figure 49. LQFP80 - 80-pin, 14 x 14 mm low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

10.3 LQFP48 package information

Figure 54. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline



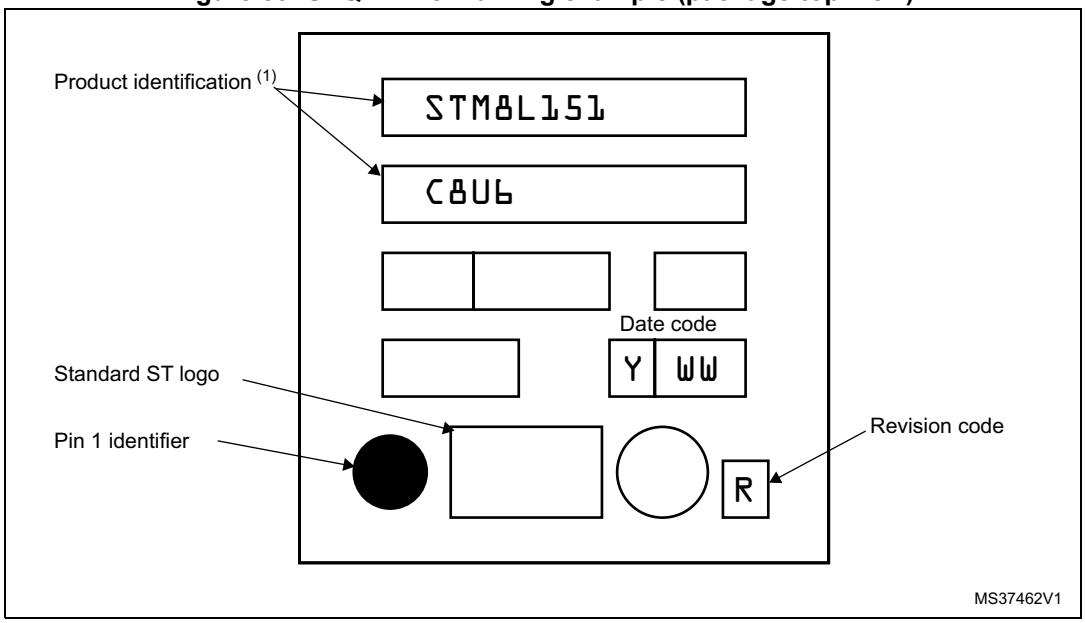
1. Drawing is not to scale.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 59. UFQFPN48 marking example (package top view)



1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 67. WLCSP32 - 32-ball, 1.913 x 3.329 mm, 0.4 mm pitch wafer level chip scale package mechanical data(1)

Symbol	millimeters			inches(2)		
	Min	Typ	Max	Min	Typ	Max
A	0.525	0.555	0.585	0.0207	0.0219	0.0230
A1	-	0.175	-	-	0.0069	-
A2	-	0.380	-	-	0.0150	-
A3(3)	-	0.025	-	-	0.0010	-
b(4)	0.220	0.250	0.280	0.0087	0.0098	0.0110
D	1.878	1.913	1.948	0.0739	0.0753	0.0767
E	3.294	3.329	3.364	0.1297	0.1311	0.1324
e	-	0.400	-	-	0.0157	-
e1	-	1.200	-	-	0.0472	-
e2	-	2.800	-	-	0.1102	-
F	-	0.3565	-	-	0.0140	-
G	-	0.2645	-	-	0.0104	-
aaa	-	-	0.100	-	-	0.0039
bbb	-	-	0.100	-	-	0.0039
ccc	-	-	0.100	-	-	0.0039
ddd	-	-	0.050	-	-	0.0020
eee	-	-	0.050	-	-	0.0020

1. Preliminary data.
2. Values in inches are converted from mm and rounded to 4 decimal digits.
3. Back side coating.
4. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

Figure 61. WLCSP32 - 32-ball, 1.913 x 3.329 mm, 0.4 mm pitch wafer level chip scale package recommended footprint

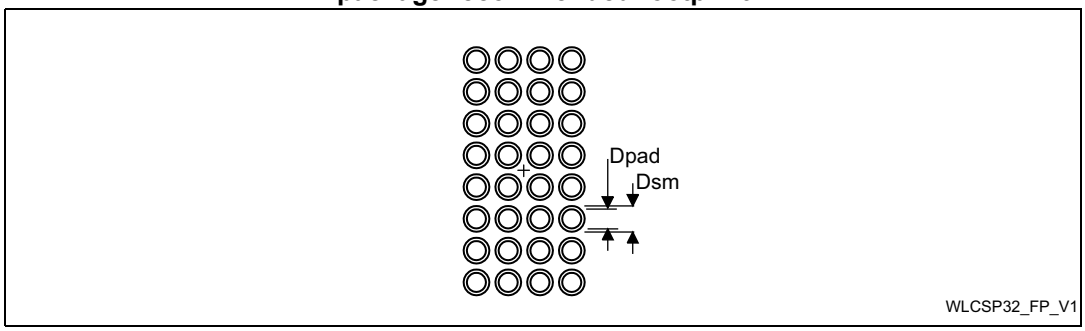


Table 68. WLCSP32 recommended PCB design rules

Dimension	Recommended values
Pitch	0.4 mm
Dpad	0.225 mm
Dsm	0.290 mm typical (depending on the solder mask registration tolerance)
Stencil opening	0.250 mm
Stencil thickness	0.100 mm

11 Ordering information scheme

Table 69. Ordering information scheme

Example: STM8 L 152 C 8 T 6 D xx

Device family

STM8 microcontroller

Product type

L = Low-power

Device subfamily

151: Devices without LCD

152: Devices with LCD

Pin count

K = 32 balls

C = 48 pins

R = 64 pins

M = 80 pins

Program memory size

8 = 64 Kbyte of Flash memory

6 = 32 Kbyte of Flash memory

Package

T = LQFP

U = UFQFPN

Y = WLCSP32

Temperature range

3 = Industrial temperature range, – 40 to 125 °C

7 = Industrial temperature range, – 40 to 105 °C

6 = Industrial temperature range, – 40 to 85 °C

Option

Blank = V_{DD} range from 1.8 to 3.6 V and BOR enabled

D = V_{DD} range from 1.65 to 3.6 V and BOR disabled

Packing

TR = tape and reel

For a list of available options (e.g. memory size, package) and order-able part numbers or for further information on any aspect of this device, please go to *www.st.com* or contact the ST Sales Office nearest to you.