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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, IR, LCD, POR, PWM, WDT
Number of I/O	54
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 28x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8l152r8t6

2.2 Device overview

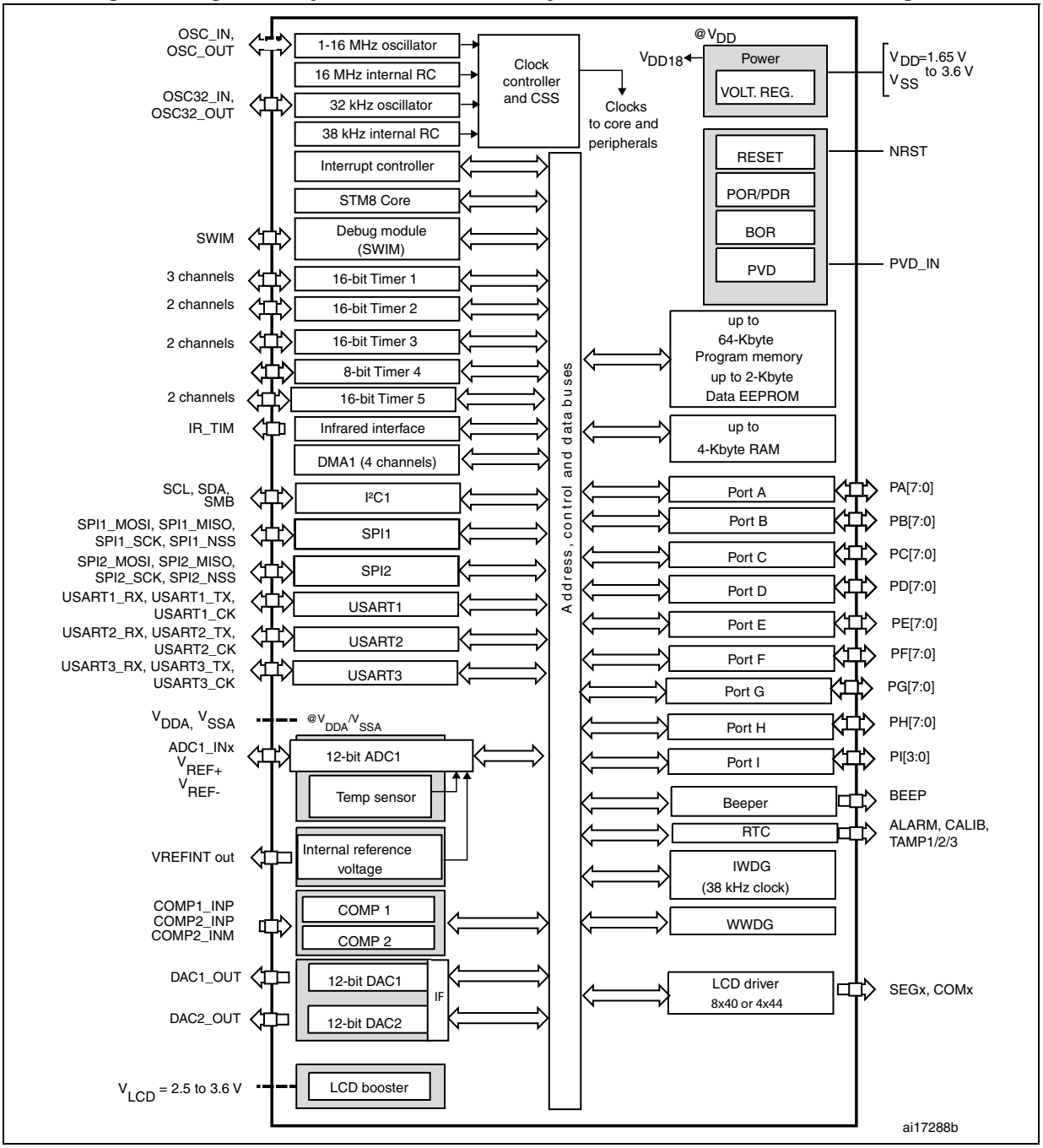
Table 2. High-density and medium+ density STM8L15xx6/8 low power device features and peripheral counts

Features		STM8L15xC8	STM8L15xK8	STM8L15xR8	STM8L15xM8	STM8L15xR6
Flash (Kbyte)		64	64	64	64	32
Data EEPROM (Kbyte)		2	2	2	2	1
RAM (Kbyte)		4	4	4	4	2
LCD		8x24 or 4x28(1)	4x15(1)	8x36 or 4x40(1)	8x40 or 4x44(1)	8x36 or 4x40(1)
Timers	Basic	1 (8-bit)	1 (8-bit)	1 (8-bit)	1 (8-bit)	1 (8-bit)
	General purpose	3 (16-bit)	3 (16-bit)	3 (16-bit)	3 (16-bit)	3 (16-bit)
	Advanced control	1 (16-bit)	1 (16-bit)	1 (16-bit)	1 (16-bit)	1 (16-bit)
Communication interfaces	SPI	2	1	2	2	2
	I2C	1	1	1	1	1
	USART	3	2	3	3	3
GPIOs		41(2)	28(2)	54(2)	68(2)	54(2)
12-bit synchronized ADC (number of channels)		1 (25)	1 (18)	1 (28)	1 (28)	1 (28)
12-Bit DAC Number of channels		2 2	1 1	2 2	2 2	2 2
Comparators (COMP1/COMP2)		2	2	2	2	2
Others		RTC, window watchdog, independent watchdog, 16-MHz and 38-kHz internal RC, 1- to 16-MHz and 32-kHz external oscillator				
CPU frequency		16 MHz				
Operating voltage		1.8 to 3.6 V (down to 1.65 V at power-down) with BOR 1.65 to 3.6 V without BOR				
Operating temperature		–40 to +85 °C / –40 to +105 °C / –40 to +125 °C				
Packages		UFQFPN48 LQFP48	WLCSP32	LQFP64	LQFP80	LQFP64

1. STM8L152x6/8 versions only.
2. The number of GPIOs given in this table includes the NRST/PA1 pin but the application can use the NRST/PA1 pin as general purpose output only (PA1).

3 Functional overview

Figure 1. High-density and medium+ density STM8L15xx6/8 device block diagram



1. **Legend**:
   AF: alternate function
   ADC: Analog-to-digital converter
   BOR: Brownout reset
   DMA: Direct memory access
   DAC: Digital-to-analog converter
   I²C: Inter-integrated circuit multimaster interface
   IWDG: Independent watchdog

Table 5. High-density and medium+ density STM8L15x pin description (continued)

Pin number				Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP80	LQFP64	UFQFPN48 and LQFP48	WLCSP32				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
58	46	-	-	PD5/TIM1_CH3 /LCD_SEG19(3)/ ADC1_IN9/ *[COMP1_INP]*	I/O	FT(6)	**X**	X	X	HS	X	X	**Port D5**	Timer 1 - channel 3 / LCD segment 19 / ADC1_IN9/ *[Comparator 1 positive input]*
-	-	34	-(4)	PD5/TIM1_CH3 /LCD_SEG19(3)/ ADC1_IN9/SPI2_MOSI/ *[COMP1_INP]*	I/O	FT(6)	**X**	X	X	HS	X	X	**Port D5**	Timer 1 - channel 3 / LCD segment 19 / ADC1_IN9/ SPI2 master out/slave in/ *[Comparator 1 positive input]*
59	47	-	-	PD6/TIM1_BKIN /LCD_SEG20(3)/ ADC1_IN8/RTC_CALIB/ *[COMP1_INP]*/VREFINT	I/O	FT(6)	**X**	X	X	HS	X	X	**Port D6**	Timer 1 - break input / LCD segment 20 / ADC1_IN8 / RTC calibration/*[Comparator 1 positive input]*/Internal reference voltage output
-	-	35	-(4)	PD6/TIM1_BKIN /LCD_SEG20(3)/ ADC1_IN8/RTC_CALIB/ SPI2_SCK/*[COMP1_INP]*/ VREFINT	I/O	FT(6)	**X**	X	X	HS	X	X	**Port D6**	Timer 1 - break input / LCD segment 20 / ADC1_IN8 / RTC calibration/SPI2 clock/ *[Comparator 1 positive input]*/Internal reference voltage output
60	48	-	-	PD7/TIM1_CH1N /LCD_SEG21(3)/ ADC1_IN7/RTC_ALARM/ *[COMP1_INP]*/VREFINT	I/O	FT(6)	**X**	X	X	HS	X	X	**Port D7**	Timer 1 - inverted channel 1/ LCD segment 21 / ADC1_IN7 / RTC alarm/*[Comparator 1 positive input]*/Internal reference voltage output
-	-	36	-(4)	PD7/TIM1_CH1N /LCD_SEG21(3)/ ADC1_IN7/RTC_ALARM /SPI2_NSS/*[COMP1_INP]*/ VREFINT	I/O	FT(6)	**X**	X	X	HS	X	X	**Port D7**	Timer 1 - inverted channel 1/ LCD segment 21 / ADC1_IN7 / RTC alarm /SPI2 master/slave select/*[Comparator 1 positive input]*/Internal reference voltage output
61	49	-	-	PG4/LCD_SEG32/ SPI2_NSS	I/O	FT(6)	**X**	X	X	HS	X	X	**Port G4**	LCD segment 32 / SPI2 master/slave select

Table 5. High-density and medium+ density STM8L15x pin description (continued)

Pin number				Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP80	LQFP64	UFQFPN48 and LQFP48	WLCSP32				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
-	-	-	G4	$V_{DD1}/V_{DDA}/V_{REF+}$	S	-	-	-	-	-	-	-	Digital power supply / Analog power supply / ADC1 positive voltage reference	
17	13	12	-	V_{REF+}/V_{REF+_DAC}	S	-	-	-	-	-	-	-	ADC1 and DAC1/2 positive voltage reference	
18	14	-	-	PG0/LCD SEG28(3) /USART3_RX/ *[TIM2_BKIN]*	I/O	FT(6)	**X**	X	X	HS	X	X	**Port G0**	LCD segment 28/ USART3 receive / *[Timer 2 - break input]*
19	15	-	-	PG1/LCD SEG29(3) /USART3_TX/ *[TIM3_BKIN]*	I/O	FT(6)	**X**	X	X	HS	X	X	**Port G1**	LCD segment 29/ USART3 transmit / *[Timer 3 -break input]*
20	16	-	-	PG2/LCD_SEG30(3)/ USART3_CK	I/O	FT(6)	**X**	X	X	HS	X	X	**Port G2**	LCD segment 30/ USART 3 synchronous clock
21	17	-	-	PG3/LCD SEG 31 (3)/ *[TIM3_ETR]*	I/O	FT(6)	**X**	X	X	HS	X	X	**Port G3**	LCD segment 31/ *[Timer 3 - trigger]*
33	-	-	-	PH4/USART2_RX	I/O	FT(6)	**X**	X	X	HS	X	X	**Port H4**	USART2 receive
34	-	-	-	PH5/USART2_TX	I/O	FT(6)	**X**	X	X	HS	X	X	**Port H5**	USART2 transmit
35	-	-	-	PH6/USART2_CK/ TIM5_CH1	I/O	FT(6)	**X**	X	X	HS	X	X	**Port H6**	USART2 synchronous clock/ Timer 5 - channel 1
36	-	-	-	PH7/TIM5_CH2	I/O	FT(6)	**X**	X	X	HS	X	X	**Port H7**	Timer 5 - channel 2
-	-	9	F4	V_{SS} /V_{SSA} /V_{REF-}	S	-	-	-	-	-	-	-	I/O ground / Analog ground voltage / ADC1 negative voltage reference	
13	9	-	-	V_{SSA} /V_{REF-}	S	-	-	-	-	-	-	-	Analog ground voltage / ADC1 negative voltage reference	
37	29	-	-	V_{DD3}	S	-	-	-	-	-	-	-	IOs supply voltage	
38	30	-	H1	V_{SS3}	S	-	-	-	-	-	-	-	IOs ground voltage	
5	1	1	A4	PA0(9)/*[USART1_CK]*(2)/ SWIM/BEEP/IR_TIM (10)	I/O		X	**X**	X	HS	X	X	**Port A0**	*[USART1 synchronous clock]*(2)/ SWIM input and output / Beep output / Infrared Timer output
68	56	40	-	V_{SS2}	S	-	-	-	-	-	-	-	IOs ground voltage	
67	55	39	-	V_{DD2}	S	-	-	-	-	-	-	-	IOs supply voltage	

Table 9. General hardware register map

Address	Block	Register label	Register name	Reset status
0x00 502E to 0x00 5049	Reserved area (28 byte)			
0x00 5050	Flash	FLASH_CR1	Flash control register 1	0x00
0x00 5051		FLASH_CR2	Flash control register 2	0x00
0x00 5052		FLASH _PUKR	Flash program memory unprotection key register	0x00
0x00 5053		FLASH _DUKR	Data EEPROM unprotection key register	0x00
0x00 5054		FLASH _IAPSR	Flash in-application programming status register	0x00
0x00 5055 to 0x00 506F	Reserved area (27 byte)			
0x00 5070	DMA1	DMA1_GCSR	DMA1 global configuration & status register	0xFC
0x00 5071		DMA1_GIR1	DMA1 global interrupt register 1	0x00
0x00 5072 to 0x00 5074		Reserved area (3 byte)		
0x00 5075		DMA1_C0CR	DMA1 channel 0 configuration register	0x00
0x00 5076		DMA1_C0SPR	DMA1 channel 0 status & priority register	0x00
0x00 5077		DMA1_C0NDTR	DMA1 number of data to transfer register (channel 0)	0x00
0x00 5078		DMA1_C0PARH	DMA1 peripheral address high register (channel 0)	0x52
0x00 5079		DMA1_C0PARL	DMA1 peripheral address low register (channel 0)	0x00
0x00 507A		Reserved area (1 byte)		
0x00 507B		DMA1_C0M0ARH	DMA1 memory 0 address high register (channel 0)	0x00
0x00 507C		DMA1_C0M0ARL	DMA1 memory 0 address low register (channel 0)	0x00
0x00 507D to 0x00 507E		Reserved area (2 byte)		
0x00 507F		DMA1_C1CR	DMA1 channel 1 configuration register	0x00
0x00 5080		DMA1_C1SPR	DMA1 channel 1 status & priority register	0x00
0x00 5081		DMA1_C1NDTR	DMA1 number of data to transfer register (channel 1)	0x00
0x00 5082		DMA1_C1PARH	DMA1 peripheral address high register (channel 1)	0x52
0x00 5083	DMA1	DMA1_C1PARL	DMA1 peripheral address low register (channel 1)	0x00

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 52B0	TIM1	TIM1_CR1	TIM1 control register 1	0x00
0x00 52B1		TIM1_CR2	TIM1 control register 2	0x00
0x00 52B2		TIM1_SMCR	TIM1 Slave mode control register	0x00
0x00 52B3		TIM1_ETR	TIM1 external trigger register	0x00
0x00 52B4		TIM1_DER	TIM1 DMA1 request enable register	0x00
0x00 52B5		TIM1_IER	TIM1 Interrupt enable register	0x00
0x00 52B6		TIM1_SR1	TIM1 status register 1	0x00
0x00 52B7		TIM1_SR2	TIM1 status register 2	0x00
0x00 52B8		TIM1_EGR	TIM1 event generation register	0x00
0x00 52B9		TIM1_CCMR1	TIM1 Capture/Compare mode register 1	0x00
0x00 52BA		TIM1_CCMR2	TIM1 Capture/Compare mode register 2	0x00
0x00 52BB		TIM1_CCMR3	TIM1 Capture/Compare mode register 3	0x00
0x00 52BC		TIM1_CCMR4	TIM1 Capture/Compare mode register 4	0x00
0x00 52BD		TIM1_CCER1	TIM1 Capture/Compare enable register 1	0x00
0x00 52BE		TIM1_CCER2	TIM1 Capture/Compare enable register 2	0x00
0x00 52BF		TIM1_CNTRH	TIM1 counter high	0x00
0x00 52C0		TIM1_CNTRL	TIM1 counter low	0x00
0x00 52C1		TIM1_PSCRH	TIM1 prescaler register high	0x00
0x00 52C2		TIM1_PSCRL	TIM1 prescaler register low	0x00
0x00 52C3		TIM1_ARRH	TIM1 Auto-reload register high	0xFF
0x00 52C4		TIM1_ARRL	TIM1 Auto-reload register low	0xFF
0x00 52C5		TIM1_RCR	TIM1 Repetition counter register	0x00
0x00 52C6		TIM1_CCR1H	TIM1 Capture/Compare register 1 high	0x00
0x00 52C7		TIM1_CCR1L	TIM1 Capture/Compare register 1 low	0x00
0x00 52C8		TIM1_CCR2H	TIM1 Capture/Compare register 2 high	0x00
0x00 52C9		TIM1_CCR2L	TIM1 Capture/Compare register 2 low	0x00
0x00 52CA		TIM1_CCR3H	TIM1 Capture/Compare register 3 high	0x00
0x00 52CB		TIM1_CCR3L	TIM1 Capture/Compare register 3 low	0x00
0x00 52CC		TIM1_CCR4H	TIM1 Capture/Compare register 4 high	0x00
0x00 52CD		TIM1_CCR4L	TIM1 Capture/Compare register 4 low	0x00
0x00 52CE		TIM1_BKR	TIM1 break register	0x00
0x00 52CF		TIM1_DTR	TIM1 dead-time register	0x00
0x00 52D0		TIM1_OISR	TIM1 output idle state register	0x00
0x00 52D1		TIM1_DCR1	DMA1 control register 1	0x00

Table 10. CPU/SWIM/debug module/interrupt controller registers (continued)

Address	Block	Register label	Register name	Reset status
0x00 7F90	DM	DM_BK1RE	DM breakpoint 1 register extended byte	0xFF
0x00 7F91		DM_BK1RH	DM breakpoint 1 register high byte	0xFF
0x00 7F92		DM_BK1RL	DM breakpoint 1 register low byte	0xFF
0x00 7F93		DM_BK2RE	DM breakpoint 2 register extended byte	0xFF
0x00 7F94		DM_BK2RH	DM breakpoint 2 register high byte	0xFF
0x00 7F95		DM_BK2RL	DM breakpoint 2 register low byte	0xFF
0x00 7F96		DM_CR1	DM Debug module control register 1	0x00
0x00 7F97		DM_CR2	DM Debug module control register 2	0x00
0x00 7F98		DM_CSR1	DM Debug module control/status register 1	0x10
0x00 7F99		DM_CSR2	DM Debug module control/status register 2	0x00
0x00 7F9A		DM_ENFCTR	DM enable function register	0xFF
0x00 7F9B to 0x00 7F9F	Reserved area (5 byte)			

1. Accessible by debug module only

6 Interrupt vector mapping

Table 11. Interrupt mapping

IRQ No.	Source block	Description	Wakeup from Halt mode	Wakeup from Active-halt mode	Wakeup from Wait (WFI mode)	Wakeup from Wait (WFE mode)(1)	Vector address
-	RESET	Reset	Yes	Yes	Yes	Yes	0x00 8000
-	TRAP	Software interrupt	-	-	-	-	0x00 8004
0	TLI(2)	External Top level Interrupt	-	-	-	-	0x00 8008
1	FLASH	EOP/WR_PG_DIS	-	-	Yes	Yes(3)	0x00 800C
2	DMA1 0/1	DMA1 channels 0/1	-	-	Yes	Yes(3)	0x00 8010
3	DMA1 2/3	DMA1 channels 2/3	-	-	Yes	Yes(3)	0x00 8014
4	RTC/LSE_ CSS	RTC alarm interrupt/LSE CSS interrupt	Yes	Yes	Yes	Yes	0x00 8018
5	EXTI E/F/PVD(4)	PortE/F interrupt/PVD interrupt	Yes	Yes	Yes	Yes(3)	0x00 801C
6	EXTIB/G	External interrupt port B/G	Yes	Yes	Yes	Yes(3)	0x00 8020
7	EXTID/H	External interrupt port D/H	Yes	Yes	Yes	Yes(3)	0x00 8024
8	EXTI0	External interrupt 0	Yes	Yes	Yes	Yes(3)	0x00 8028
9	EXTI1	External interrupt 1	Yes	Yes	Yes	Yes(3)	0x00 802C
10	EXTI2	External interrupt 2	Yes	Yes	Yes	Yes(3)	0x00 8030
11	EXTI3	External interrupt 3	Yes	Yes	Yes	Yes(3)	0x00 8034
12	EXTI4	External interrupt 4	Yes	Yes	Yes	Yes(3)	0x00 8038
13	EXTI5	External interrupt 5	Yes	Yes	Yes	Yes(3)	0x00 803C
14	EXTI6	External interrupt 6	Yes	Yes	Yes	Yes(3)	0x00 8040
15	EXTI7	External interrupt 7	Yes	Yes	Yes	Yes(3)	0x00 8044
16	LCD	LCD interrupt	-	-	Yes	Yes	0x00 8048
17	CLK/ TIM1/ DAC	System clock switch/CSS interrupt/TIM1 break/DAC	-	-	Yes	Yes	0x00 804C
18	COMP1/ COMP2 ADC1	Comparator 1 and 2 interrupt/ADC1	Yes	Yes	Yes	Yes(3)	0x00 8050
19	TIM2/ USART2	TIM2 update /overflow/trigger/break/ USART2 transmission complete/transmit data register empty interrupt	-	-	Yes	Yes(3)	0x00 8054

9.3.3 Supply current characteristics

Total current consumption

The MCU is placed under the following conditions:

- All I/O pins in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except if explicitly mentioned.

In the following table, data are based on characterization results, unless otherwise specified.

Subject to general operating conditions for V_{DD} and T_A.

Table 20. Total current consumption in Run mode

Symbol	Para meter	Conditions(1)			Typ.	Max.				Unit
						55°C	85 °C (2)	105 °C (3)	125 °C (4)	
$I_{DD(RUN)}$	Supply current in run mode (5)	All peripherals OFF, code executed from RAM, V_{DD} from 1.65 V to 3.6 V	HSI RC osc. (16 MHz)(6)	f_{CPU} = 125 kHz	0.22	0.28	0.39	0.47	0.51	mA
				f_{CPU} = 1 MHz	0.32	0.38	0.49	0.57	0.61	
				f_{CPU} = 4 MHz	0.59	0.65	0.76	0.84	0.88	
				f_{CPU} = 8 MHz	0.93	0.99	1.1	1.18	1.22	
				f_{CPU} = 16 MHz	1.62	1.68	1.79(7)	1.87(7)	1.91(7)	
			HSE external clock (f_{CPU}=f_{HSE}) (8)	f_{CPU} = 125 kHz	0.21	0.25	0.35	0.44	0.49	
				f_{CPU} = 1 MHz	0.3	0.34	0.44	0.53	0.58	
				f_{CPU} = 4 MHz	0.57	0.61	0.71	0.8	0.85	
				f_{CPU} = 8 MHz	0.95	0.99	1.09	1.18	1.23	
				f_{CPU} = 16 MHz	1.73	1.77	1.87(7)	1.96(7)	2.01(7)	
			LSI RC osc. (typ. 38 kHz)	f_{CPU} = f_{LSI}	0.029	0.035	0.039	0.044	0.055	
			LSE external clock (32.768 kHz)	f_{CPU} = f_{LSE}	0.028	0.034	0.038	0.042	0.054	

Figure 18. Typical $I_{DD(LPR)}$ vs. V_{DD} (LSI clock source), all peripherals OFF

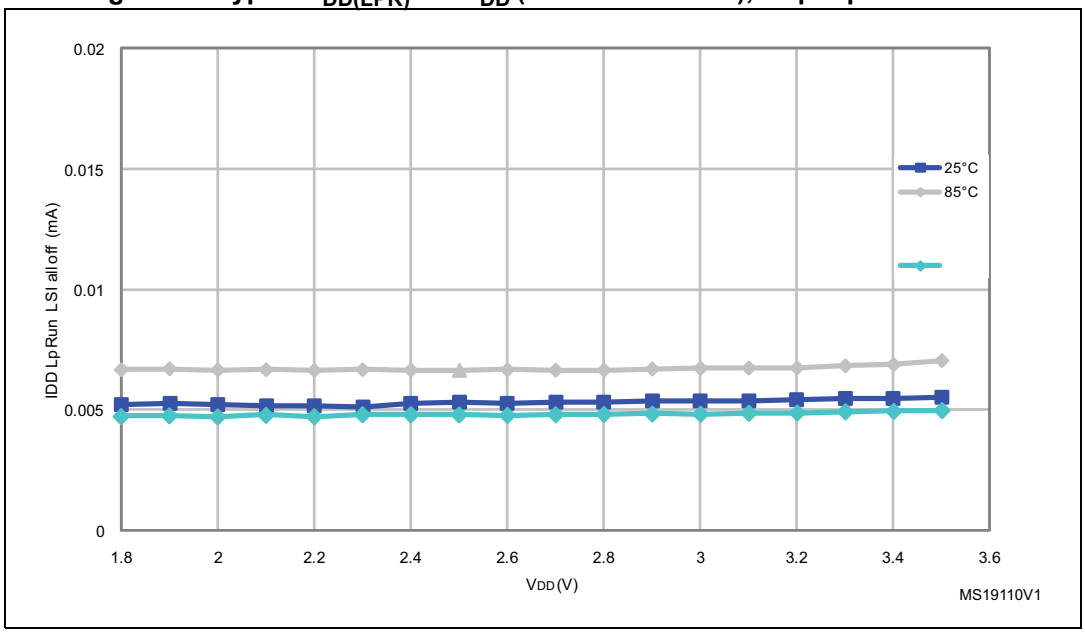
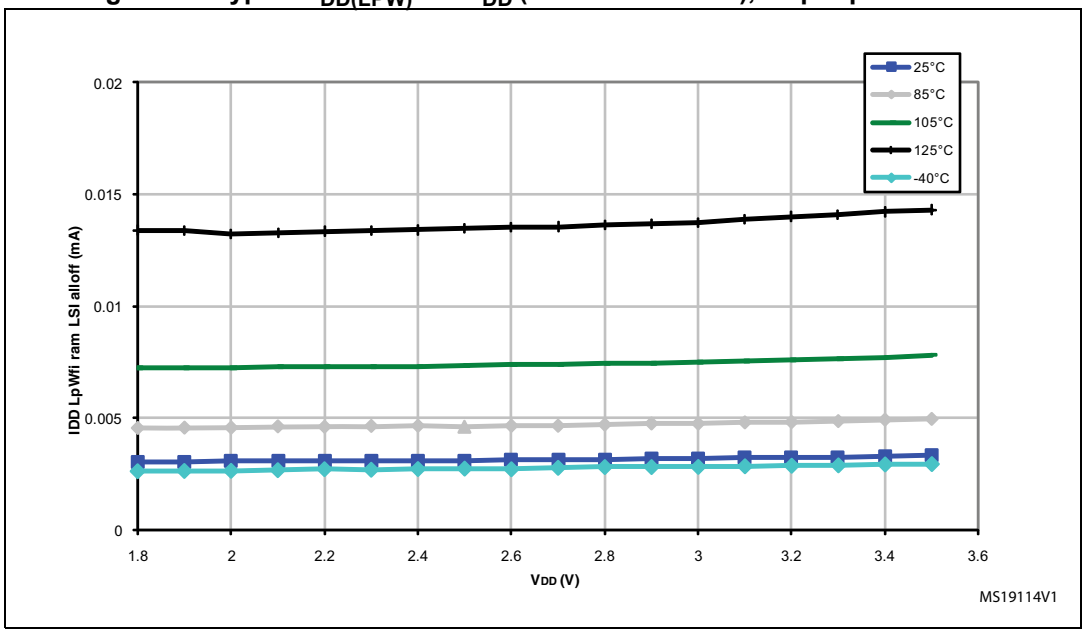


Figure 19. Typical $I_{DD(LPW)}$ vs. V_{DD} (LSI clock source), all peripherals OFF



1. Typical current consumption measured with code executed from RAM.

Figure 26. Typical V_{IL} and V_{IH} vs. V_{DD} (standard I/Os)

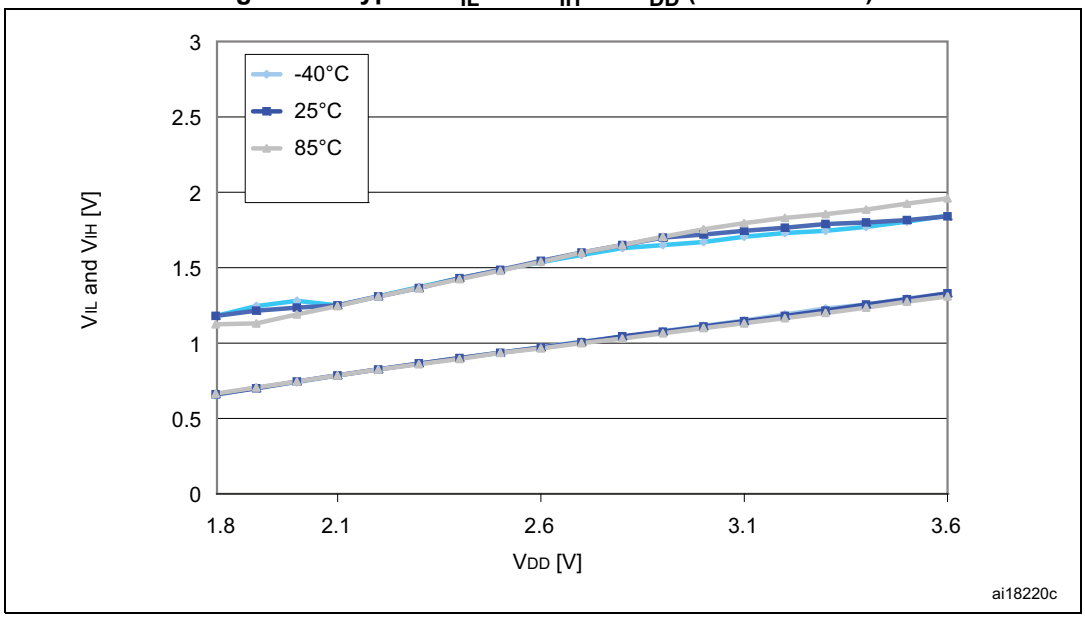


Figure 27. Typical V_{IL} and V_{IH} vs. V_{DD} (true open drain I/Os)

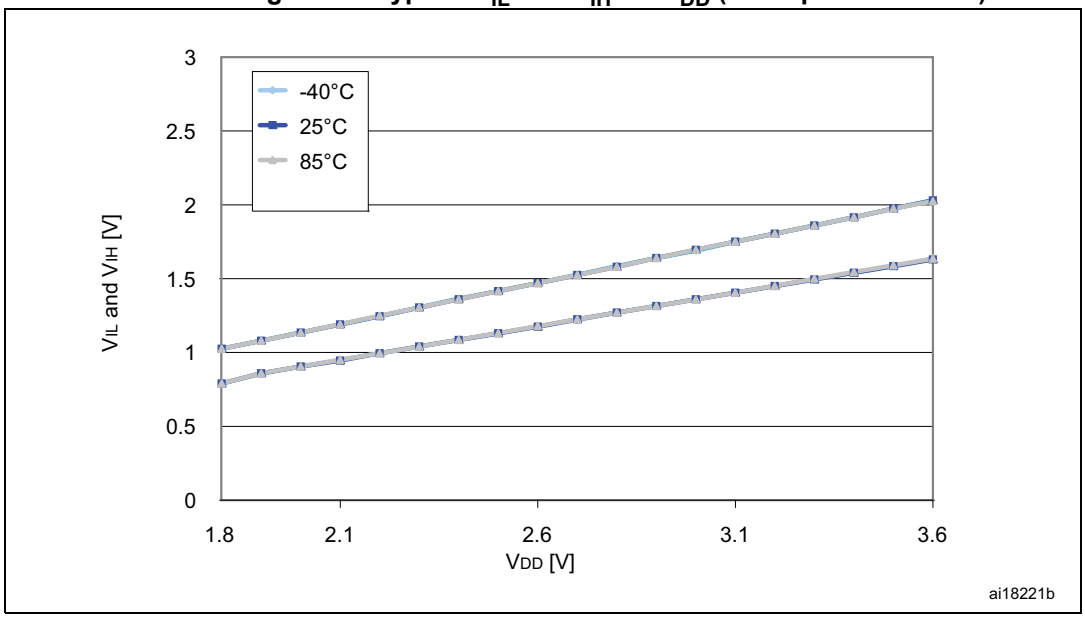
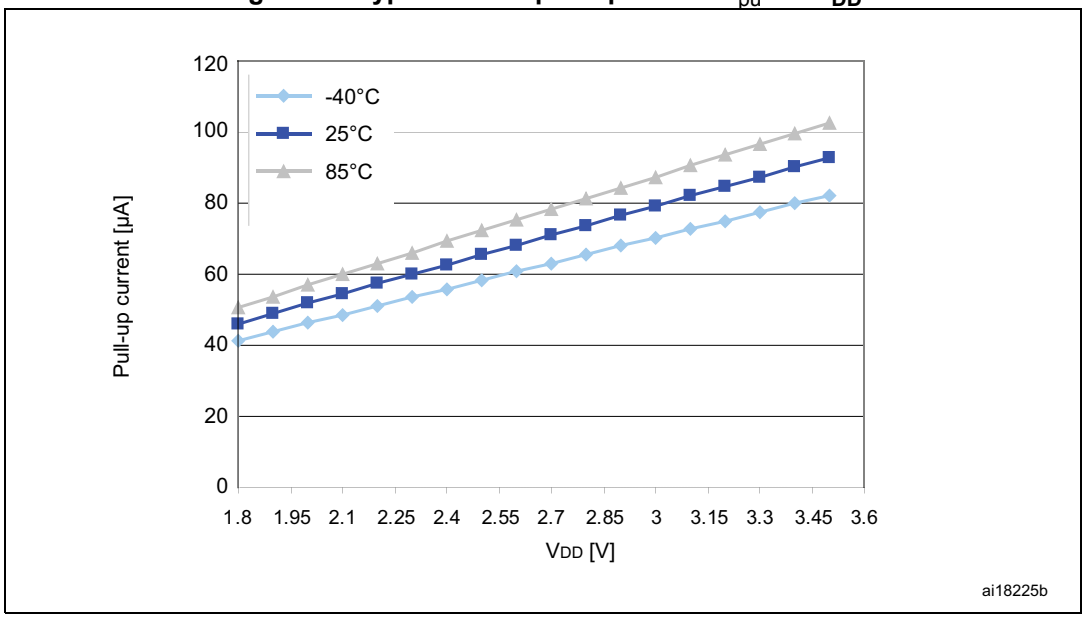


Figure 37. Typical NRST pull-up current I_{pu} vs. V_{DD}



The reset network shown in *Figure 38* protects the device against parasitic resets. The user must ensure that the level on the NRST pin can go below the V_{IL} max. level specified in *Table 42*. Otherwise the reset is not taken into account internally. For power consumption-sensitive applications, the capacity of the external reset capacitor can be reduced to limit the charge/discharge current. If the NRST signal is used to reset the external circuitry, the user must pay attention to the charge/discharge time of the external capacitor to meet the reset timing conditions of the external devices. The minimum recommended capacity is 10 nF.

Figure 38. Recommended NRST pin configuration

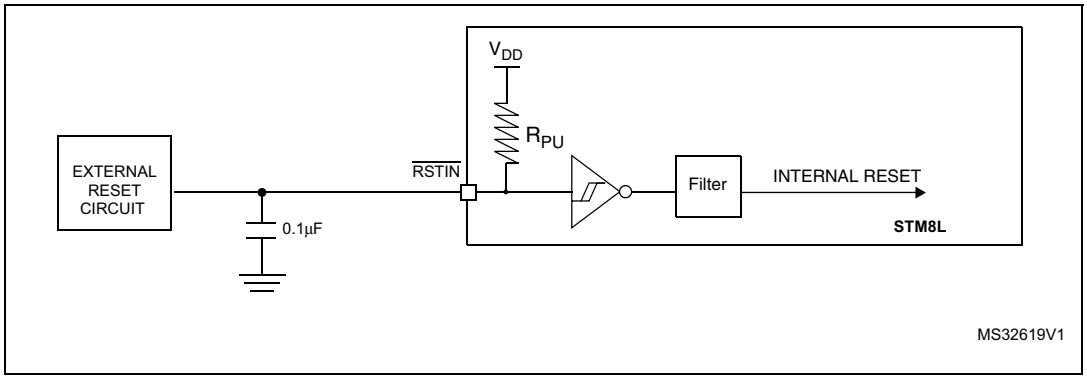


Figure 45. Maximum dynamic current consumption on V_{REF+} supply pin during ADC conversion

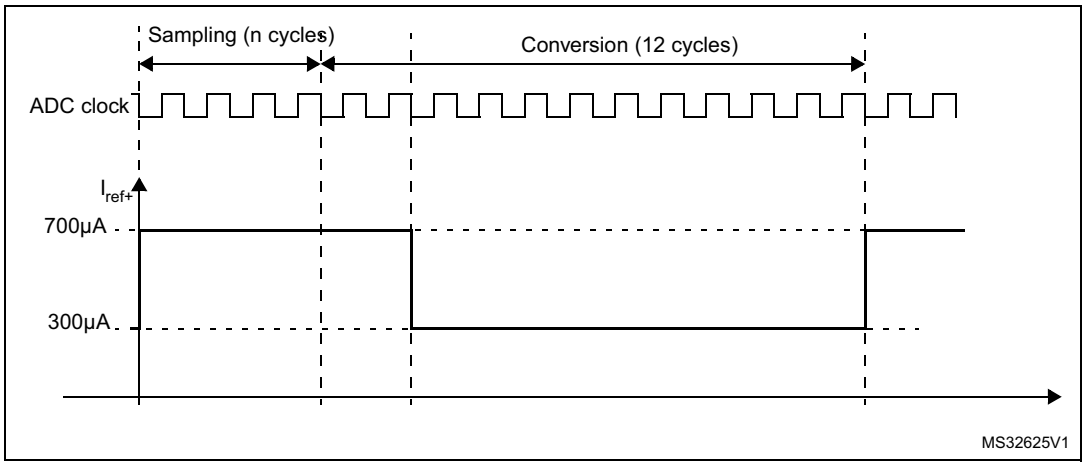


Table 57. R_{AIN} max for f_{ADC} = 16 MHz(1)

Ts (cycles)	Ts (µs)	R_{AIN} max (kohm)			
		Slow channels		Fast channels	
		2.4 V < V_{DDA} < 3.6 V	1.8 V < V_{DDA} < 2.4 V	2.4 V < V_{DDA} < 3.3 V	1.8 V < V_{DDA} < 2.4 V
4	0.25	Not allowed	Not allowed	0.7	Not allowed
9	0.5625	0.8	Not allowed	2.0	1.0
16	1	2.0	0.8	4.0	3.0
24	1.5	3.0	1.8	6.0	4.5
48	3	6.8	4.0	15.0	10.0
96	6	15.0	10.0	30.0	20.0
192	12	32.0	25.0	50.0	40.0
384	24	50.0	50.0	50.0	50.0

1. Guaranteed by design.

General PCB design guidelines

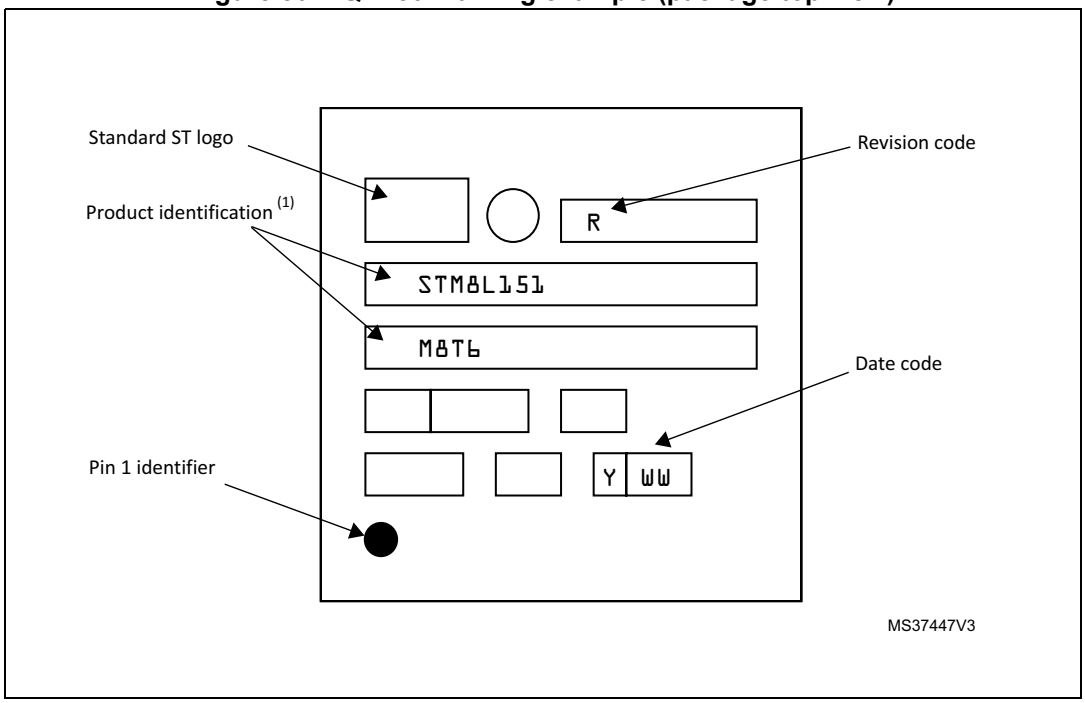
Power supply decoupling should be performed as shown in *Figure 46* or *Figure 47*, depending on whether V_{REF+} is connected to V_{DDA} or not. Good quality ceramic 10 nF capacitors should be used. They should be placed as close as possible to the chip.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

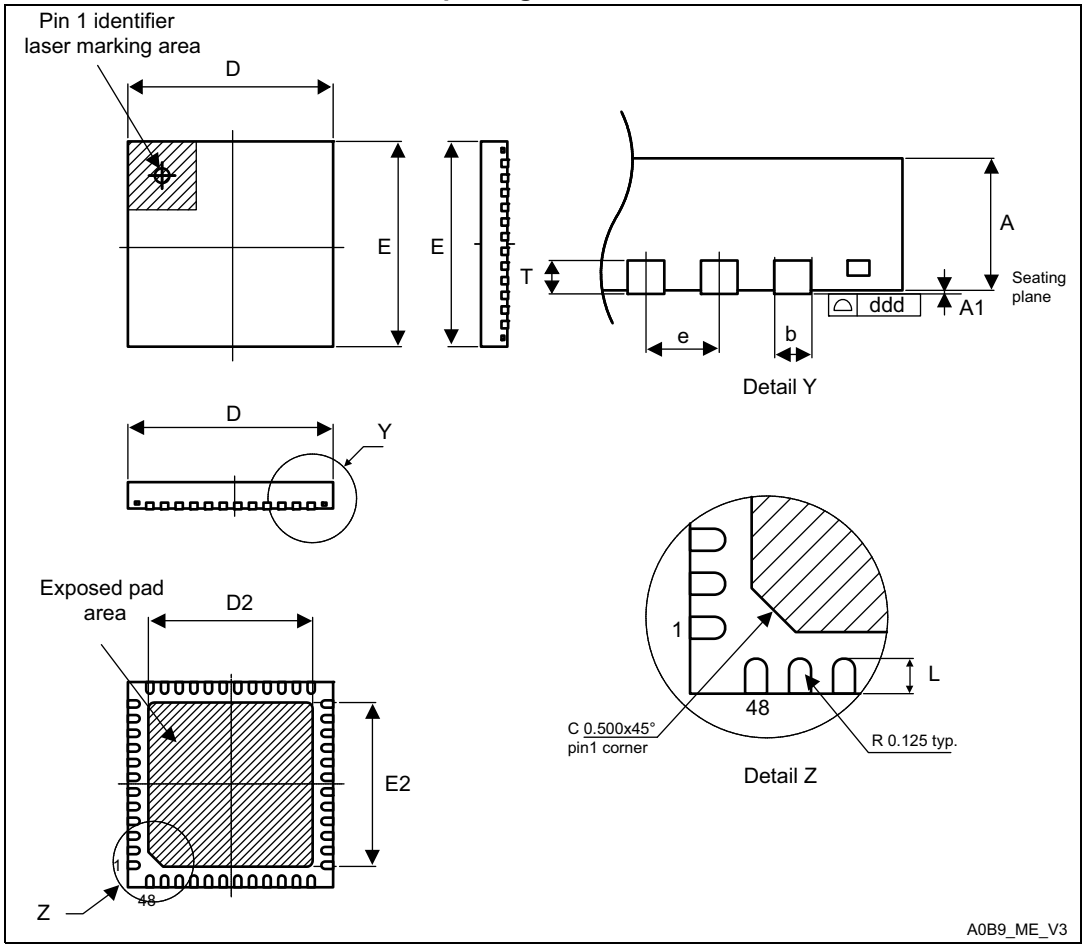
Figure 50. LQFP80 marking example (package top view)



1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

10.4 UFQFPN48 package information

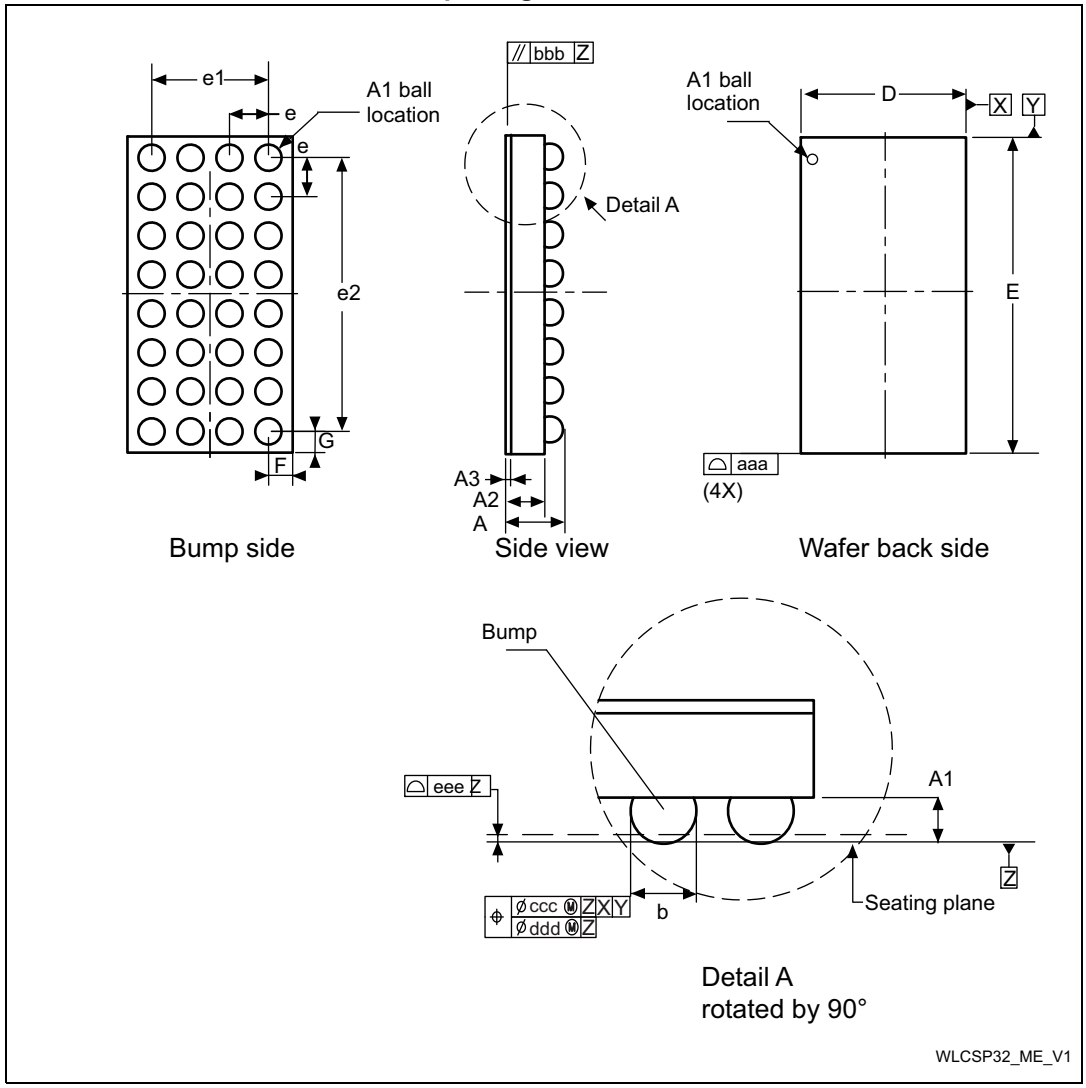
Figure 57. UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline



1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this back-side pad to PCB ground.

10.5 WLCSP32 package information

Figure 60. WLCSP32 - 32-ball, 1.913 x 3.329 mm, 0.4 mm pitch wafer level chip scale package outline



1. Drawing is not to scale.
2. Preliminary drawing.

Table 70. Document revision history (continued)

Date	Revision	Changes
03-Apr-2013	5	Updated capacitive sensing channels and “Dynamic consumption” in *Features* Updated LCD feature in *Table 2: High-density and medium+ density STM8L15xx6/8 low power device features and peripheral counts* Updated Halt mode definition in *Section 3.1: Low-power modes* Added *Bootloader* Updated *Section 3.12: System configuration controller and routing interface* Added *Section 3.13: Touch sensing* *Table 5: High-density and medium+ density STM8L15x pin description*: updated NRST/PA1, PI0, PI1, PI2, PE0, PE1, PE2, PF4, PF5, PF6, PF7, footnote *1.* and added *Note:* Updated ‘0x00 502E to 0x00 5049’ reserved area in *Table 9: General hardware register map* Updated reference to SWIM/DEBUG manual in *Section 7: Option bytes* Updated BOR factory default settings to 0x00 in *Table 12: Option byte addresses* Corrected ROP option byte value in *Table 12: Option byte addresses* Added *Figure 45: Maximum dynamic current consumption on VREF+ supply pin during ADC conversion* Updated STABVREFINT max value in *Table 46: Reference voltage characteristics* Updated *Figure 41: SPI1 timing diagram - master mode* Added *Table 57: RAIN max for fADC = 16 MHz* Updated Max DAC_OUT in *Table 50: DAC characteristics* Updated *Section 9.3.12: Comparator characteristics*
31-Jul-2013	6	Added ‘Top view’ footnotes under the pinout figures in *Section 4: Pin description* Updated the PF4-PF7 pins for the LQFP80 in *Table 5: High-density and medium+ density STM8L15x pin description* Updated all packages: Updated *Figure 57: UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline* and *Table 65: LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data* Added *Figure 49: LQFP80 - 80-pin, 14 x 14 mm low-profile quad flat package recommended footprint* Added ‘tape and reel’ in *Table 69: Ordering information scheme*

Table 70. Document revision history (continued)

Date	Revision	Changes
15-Feb-2017	10	Updated value of feature 12-bit synchronized ADC (number of channels) for STM8L15xK8 on *Table 2: High-density and medium+ density STM8L15xx6/8 low power device features and peripheral counts*.