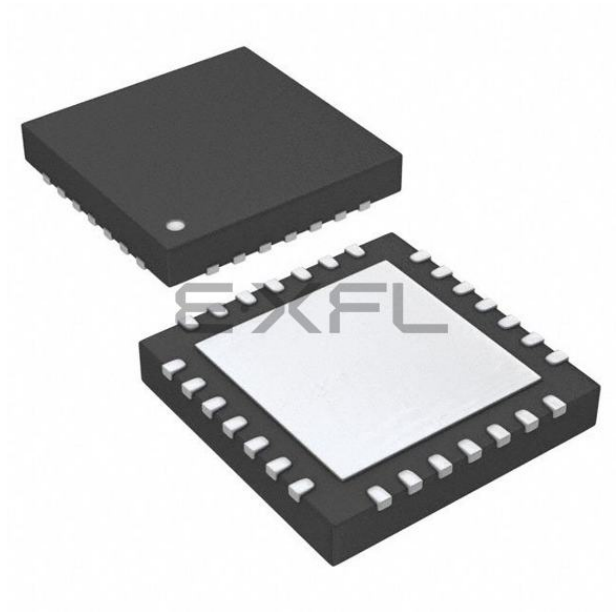

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Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
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Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
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PIC16(L)F1516/1517/1518/1519

PIC16(L)F1516/1517/1518/1519 Family Silicon Errata and Data Sheet Clarification

The PIC16(L)F1516/1517/1518/1519 family devices that you have received conform functionally to the current Device Data Sheet (DS40001452**D**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC16(L)F1516/1517/1518/1519 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A7**).

Data Sheet clarifications and corrections start on page 6, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC16(L)F1516/1517/1518/1519 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	DEVICE ID<13:0>(1),(2)					
	DEV<8:0>	REV<4:0> Silicon Revision				
		A2	A3	A4	A6	A7
PIC16F1516	01 0110 100	—	0 0011	0 0100	0 0110	0 0111
PIC16LF1516	01 0111 100	0 0010	0 0011	0 0100	0 0110	0 0111
PIC16F1517	01 0110 101	—	0 0011	0 0100	0 0110	0 0111
PIC16LF1517	01 0111 101	0 0010	0 0011	0 0100	0 0110	0 0111
PIC16F1518	01 0110 110	—	0 0011	0 0100	0 0110	0 0111
PIC16LF1518	01 0111 110	0 0010	0 0011	0 0100	0 0110	0 0111
PIC16F1519	01 0110 111	—	0 0011	0 0100	0 0110	0 0111
PIC16LF1519	01 0111 111	0 0010	0 0011	0 0100	0 0110	0 0111

Note 1: The Device ID is located in the configuration memory at address 8006h.

2: Refer to the *"PIC16(L)F151X/152X Memory Programming Specification"* (DS41442) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)				
				A2	A3	A4	A6	A7
High-Frequency Internal Oscillator (HFINTOSC)	HFINTOSC Operation	1.1	HFINTOSC is not stable when V_{DD} <2.3V.	X				
High-Frequency Internal Oscillator (HFINTOSC)	HFINTOSC Operation	1.2	HFINTOSC Max. V_{DD} at -40°C.		X			
FVR	FVR Ready Bit (FVRRDY)	2.1	FVRRDY bit may not get set at low V_{DD} and low operating temperature.	X				
Oscillator	HFINTOSC Ready/ Stable bit	3.1	Bits remained set to '1' after initial trigger.	X	X	X		
Oscillator	Clock Switching	3.2	Clock switching can cause a single corrupted instruction.	X	X	X		
Oscillator	Oscillator Start-up Timer (OST) bit	3.3	OST bit remains set.	X	X	X		
Configuration Word	Configuration Word 1, Bit 8	4.1	Writing the unimplemented Configuration Word bit 8 affects bit 7.	X	X			
Low-Dropout (LDO) Voltage Regulator	Low-Power Sleep mode	5.1	Unexpected Resets may occur at ambient temperatures below 0°C.	X	X	X	X	
MSSP (Master Synchronous Serial Port)	SPI Master mode	6.1	Buffer Full (BF) bit or MSSP Interrupt Flag (SSPIF) bit becomes set half SCK cycle too early.	X	X	X	X	X
MSSP (Master Synchronous Serial Port)	SPI Slave mode	6.2	SPI Master releasing Slave Select during Slave Sleep mode corrupts data.	X	X	X	X	X
MSSP (Master Synchronous Serial Port)	SPI Slave mode	6.3	SPI Master enabling Slave Select too early could lose received data in Slave.	X	X	X	X	X
MSSP (Master Synchronous Serial Port)	SPI Slave mode	6.4	WCOL is erroneously set in SPI Slave mode during Sleep.	X	X	X	X	X
Enhanced Universal Synchronous Receiver Transmitter (EUSART)	Transmit mode	7.1	Possible duplicate byte transmitted	X	X	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A7**).

1. Module: High-Frequency Internal Oscillator (HFINTOSC)

1.1 Internal Oscillator min. VDD

The High-Frequency Internal Oscillator requires a minimum voltage of 2.3V to operate.

Work around

None.

Affected Silicon Revisions

A2	A3	A4	A6	A7			
X							

1.2 HFINTOSC Max. VDD at -40°C

For the LF devices only, the High-Frequency Internal Oscillator may stop working at -40°C when VDD is 3.6V.

Work around

None.

Affected Silicon Revisions

A2	A3	A4	A6	A7			
	X						

2. Module: FVR

2.1 FVR Ready Bit (FVRRDY)

After the FVR is stabilized, the FVR Ready bit may not be set when the temperature is -40°C and VDD = 1.8V.

Work around

Operate above -30°C or with VDD >2.0V.

Affected Silicon Revisions

A2	A3	A4	A6	A7			
X							

3. Module: Oscillator

3.1 OSCSTAT bits: HFIOFR and HFIOFS

When HFINTOSC is selected, the HFIOFR and HFIOFS bits will become set when the oscillator becomes ready and stable. Once these bits are set, they become “stuck”, indicating that HFINTOSC is always ready and stable. If the HFINTOSC is disabled, the bits fail to be cleared.

Work around

None.

Affected Silicon Revisions

A2	A3	A4	A6	A7			
X	X	X					

3.2 Clock Switching

When switching clock sources between INTOSC clock source and an external clock source, one corrupted instruction may be executed after the switch occurs.

This issue affects Two-Speed Start-up and Fail-Safe Clock Monitor operation.

Work around

When switching from an external oscillator clock source, first switch to 16 MHz HFINTOSC. Once running at 16 MHz HFINTOSC, configure IRCF to run at desired internal oscillator frequency.

When switching from an internal oscillator (INTOSC) to an external oscillator clock source, first switch to HFINTOSC High-Power mode (8 MHz or 16 MHz). Once running from HFINTOSC, switch to the external oscillator clock source.

Affected Silicon Revisions

A2	A3	A4	A6	A7			
X	X	X					

3.3 Oscillator Start-up Timer (OST) bit

During the Two-Speed Start-up sequence, the OST is enabled to count 1024 clock cycles. After the count is reached, the OSTS bit is set, the system clock is held low until the next falling edge of the external crystal (LP, XT or HS mode), before switching to the external clock source.

When an external oscillator is configured as the primary clock and Fail-Safe Clock mode is enabled (FCMEN = 1), any of the following conditions will result in the Oscillator Start-up Timer (OST) failing to restart:

- $\overline{\text{MCLR}}$ Reset
- Wake from Sleep
- Clock change from INTOSC to Primary Clock

This anomaly will manifest itself as a clock failure condition for external oscillators which take longer than the clock failure time-out period to start.

Work around

None.

Affected Silicon Revisions

A2	A3	A4	A6	A7			
X	X	X					

4. Module: Configuration Word

4.1 Configuration Word 1, Bit 8

If an attempt is made to clear bit 8, bit 7 will be cleared instead. A cleared bit 7 enables code-protect on the device.

Work around

Do not write Configuration Word 1, bit 8 to '0'.

Affected Silicon Revisions

A2	A3	A4	A6	A7			
X	X						

5. Module: Low-Dropout (LDO) Voltage Regulator

5.1 Low-Power Sleep mode at Ambient Temperatures Below 0°C

Under the following conditions:

- ambient temperatures below 0°C
- while in Sleep mode
- VREGCON configured for Low-Power Sleep mode (VREGPM = 1)

On very rare occasions, the LDO voltage will drop below the minimum V_{DD}, causing unexpected device Resets.

Work around

For applications that operate at ambient temperatures below 0°C, use the LDO voltage regulator in Normal-Power mode (VREGPM = 0).

Affected Silicon Revisions

A2	A3	A4	A6	A7			
X	X	X	X				

6. Module: MSSP (Master Synchronous Serial Port)

6.1 SPI Master mode

When the MSSP is used in SPI Master mode and the CKE bit is clear (CKE = 0), the Buffer Full (BF) bit and the MSSP Interrupt Flag (SSPIF) bit becomes set half an SCK cycle early. If the user software immediately reacts to either of the bits being set, a write collision may occur as indicated by the WCOL bit being set.

Work around

To avoid a write collision one of the following methods should be used:

Method 1: Add a software delay of one SCK period after detecting the completed transfer (the BF bit or SSPIF bit becomes set) and prior to writing to the SSPBUF register. Verify the WCOL bit is clear after writing to SSPBUF. If the WCOL bit is set, clear the bit in software and rewrite the SSPBUF register.

Method 2: As part of the MSSP initialization procedure, set the CKE bit (CKE = 1).

Affected Silicon Revisions

A2	A3	A4	A6	A7			
X	X	X	X	X			

6.2 SPI Slave mode

When the MSSP module is configured in SPI Slave mode with $\overline{SS}$ pin control enabled (SSPM = 0100) and the device is in Sleep mode during the SPI activity, if the SPI master releases the $\overline{SS}$ line ($\overline{SS}$ goes high) before the device wakes from Sleep and updates SSPBUF, the received data will be lost.

Work around

1. The SPI master must wait a minimum of parameter SP83 ($1.5T_{CY}$ + 40 ns) after the last SCK edge and the additional wake-up time from Sleep (device dependent) before releasing the $\overline{SS}$ line.
2. If both the Master and Slave devices have an available pin, once the Slave has completed the transaction and BF or SSPIF is set, the slave could toggle an output to inform the Master that the transaction is complete and that it is safe to release the $\overline{SS}$ line.

Affected Silicon Revisions

A2	A3	A4	A6	A7			
X	X	X	X	X			

6.3 SPI Slave mode

When the MSSP module is configured in SPI Slave mode with $\overline{SS}$ pin control enabled (SSPM = 0100) and the device is in Sleep mode during SPI activity, if the SPI Master enables $\overline{SS}$ ($\overline{SS}$ goes low) within 1 T_{CY} before Sleep is executed, the data written into the SSPBUF by the slave for transmission will remain in the SSPBUF, and the byte received by the slave will be completely discarded. The MSb of the data byte that is currently loaded into SSPBUF will be transmitted on each of the eight SCK clocks, resulting in either a 0x00 or 0xFF to be incorrectly transmitted. This issue typically occurs when the device wakes up from Sleep to process data and immediately goes back to Sleep during the next transmission.

Work around

The SPI Slave must wait a minimum of 2.25 * T_{CY} from the time the $\overline{SS}$ line becomes active ($\overline{SS}$ goes low) before executing the Sleep command.

Affected Silicon Revisions

A2	A3	A4	A6	A7			
X	X	X	X	X			

6.4 SPI Slave mode

When the MSSP module is configured with either of the Slave modes listed below and Sleep is executed during transmission, the WCOL bit is erroneously set. Although the WCOL is set, it does not cause a break in transmission or reception.

Modes:

1. SPI Slave mode with $\overline{SS}$ disabled (SSPM = 0101) and CKE = 0, *or*
2. SPI Slave mode with $\overline{SS}$ enabled (SSPM = 0100) and $\overline{SS}$ in not set and then cleared before each consecutive transmission. This typically occurs during multiple byte transmissions in which the Master does not release the $\overline{SS}$ line until all transmission has completed.

Work around

1. The WCOL bit can be ignored since the issue does not interfere with MSSP hardware, *or*
2. Clear the SSPEN after each transaction then set SSPEN before next transaction.

Affected Silicon Revisions

A2	A3	A4	A6	A7			
X	X	X	X	X			

7. Module: Enhanced Universal Synchronous Receiver Transmitter (EUSART)

7.1 Transmit mode

Under certain conditions, a byte written to the TXREG register can be transmitted twice. This happens when a byte is written to TXREG just as the TSR register becomes empty. This new byte is immediately transferred to the TSR register, but also remains in the TXREG register until the completion of the current instruction cycle. If the new byte in the TSR register is transmitted before this instruction cycle has completed, the duplicate in the TXREG register will subsequently be transferred to the TSR register on the following instruction clock cycle and transmitted.

Work around

When transmitting bytes, it is common practice to check the TXIF bit before writing to TXREG register. To avoid the issue of duplicate bytes being transmitted, a NOP should be placed before the write to TXREG register. This changes the timing so that the issue does not occur.

Affected Silicon Revisions

A2	A3	A4	A6	A7			
X	X	X	X	X			

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40001452**D**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: MSSP(SPI)

The electrical specification parameter number 70 from Table 25-12 has been modified as follows:

TABLE 25-12: SPI MODE REQUIREMENTS

Param. No.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
70*	TssL2scH, TssL2scL	$\overline{SS}\downarrow$ to SCK$\downarrow$ or SCK$\uparrow$ input	**2.25***TCY	—	—	ns	

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (12/2010)

Initial release of this document.

Rev B Document (03/2011)

Added Silicon Revision A3; Added PIC16F1516, PIC16F1517, PIC16F1518 and PIC16F1519 devices; Added Module 1.2.

Rev C Document (03/2012)

Added Silicon Revision A4; Added Module 3 Oscillator; Added Module 4 Configuration Word; Other minor corrections.

Data Sheet Clarifications: Added Module 1, Oscillator.

Rev D Document (07/2012)

Added MPLAB X IDE; Added Module 5, Low-Dropout (LDO) Voltage Regulator.

Data Sheet Clarifications: Added Module 2, Memory, High-Endurance Flash.

Rev E Document (12/2012)

Added Silicon Revision A6.

Data Sheet Clarifications removed for DS41452C.

Rev F Document (10/2013)

Added Silicon Revision A7; Other minor corrections.

Rev G Document (11/2014)

Added module 6, MSSP; Other minor corrections.

Rev H Document (02/2015)

Added Modules 6.2, 6.3, 6.4 and 7 (EUSART); Other minor corrections.

Data Sheet Clarifications: Added Module 1 (MSSP Module).

NOTES:

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