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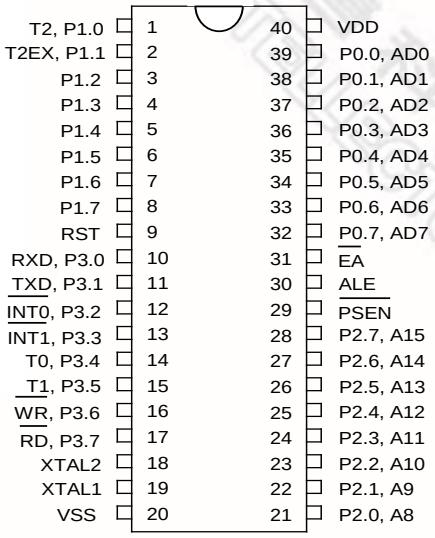
Applications of "Embedded - Microcontrollers"

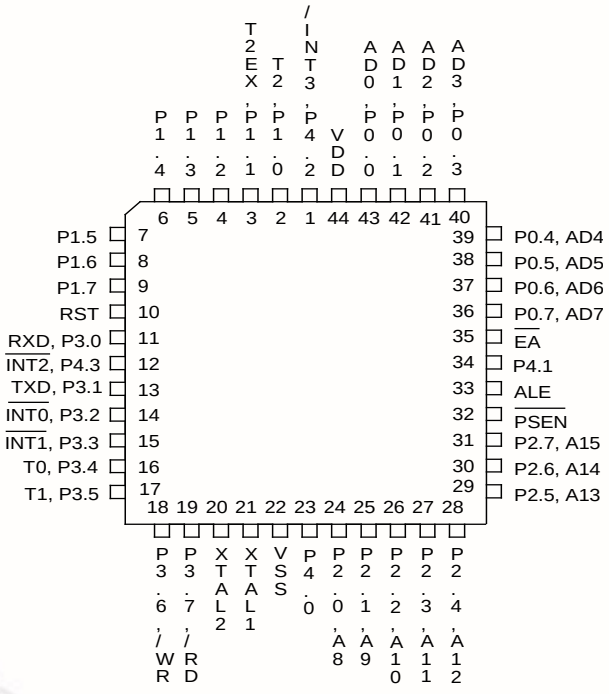
Details	
Product Status	Obsolete
Core Processor	80C52
Core Size	8-Bit
Speed	25MHz
Connectivity	EBI/EMI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.25K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w78ird2a25dl

3. PIN CONFIGURATIONS

40-Pin DIP



44-Pin PLCC



4. PIN DESCRIPTION

SYMBOL	TYPE*	DESCRIPTIONS
$\overline{EA}$	I	EXTERNAL ACCESS ENABLE: This pin forces the processor to execute instructions in external ROM. The ROM address and data are not presented on the bus if the $\overline{EA}$ pin is high.
$\overline{PSEN}$	O H	PROGRAM STORE ENABLE: $\overline{PSEN}$ indicates external ROM data is on the Port 0 address/data bus. If internal ROM is accessed, no $\overline{PSEN}$ strobe signal is present on this pin.
ALE	O H	ADDRESS LATCH ENABLE: ALE is used to enable the address latch that separates the address from the data on Port 0. ALE runs at 1/6th of the oscillator frequency.
RST	I L	RESET: If this pin is set high for two machine cycles while the oscillator is running, the W78IRD2 is reset.
XTAL1	I	CRYSTAL 1: Crystal oscillator input or external clock input.
XTAL2	O	CRYSTAL 2: Crystal oscillator output.
V_{SS}	I	GROUND: ground potential.
V_{DD}	I	POWER SUPPLY: Supply voltage for operation.
P0.0 – P0.7	I/O D	PORT 0: 8-bit, bi-directional I/O port, the same as that of the standard 80C52 Port 0 has internal pull-up resisters enabled by software.
P1.0 – P1.7	I/O H	PORT 1: 8-bit, bi-directional I/O port, the same as that of the standard 80C52.
P2.0 – P2.7	I/O H	PORT 2: 8-bit, bi-directional I/O port with internal pull-ups. This port also provides the upper address bits when accessing external memory.
P3.0 – P3.7	I/O H	PORT 3: 8-bit, bi-directional I/O port, the same as that of the standard 80C52.
P4.0 – P4.3	I/O H	PORT 4: 4-bit, bi-directional I/O port with chip-select functions.

*** Note: TYPE** I: input, O: output, I/O: bi-directional, H: pull-high, L: pull-low, D: open drain

5. FUNCTIONAL DESCRIPTION

The W78IRD2 architecture consists of a core processor that supports 111 different op-codes and references 64 KB of program space and 64 KB of data space. It is surrounded by various registers; four general-purpose I/O ports; one special-purpose, programmable, 4-bit I/O port; 256 bytes of RAM; 1 KB of auxiliary RAM (AUX-RAM); three timer/counters; a serial port; and an internal 74373 latch and 74244 buffer which can be switched to port 2.

This section introduces the RAM, Timers/Counters, Clock, Power Management, Reduce EMI Emission, and Reset.

5.1 RAM

The W78IRD2 has two banks of RAM: 256 bytes of RAM and 1 KB of AUX-RAM. AUX-RAM is enabled by clearing bit 1 in the AUXR register, and it is enabled after reset. Different addresses in RAM are addressed in different ways.

- RAM 00H – 7FH can be addressed directly or indirectly, as in the 8051. The address pointers are R0 and R1 of the selected bank.
- RAM 80H – FFH can only be addressed indirectly, as in the 8051. The address pointers are R0 and R1 of the selected bank.
- AUX-RAM 00H –3FFH is addressed indirectly in the same way external data memory is accessed with the MOVX instruction. The address pointers are R0 and R1 of the selected bank and the DPTR register.
- Addresses higher than 3FFH are stored in external memory and are accessed indirectly with the MOVX instruction, as in the 8051.

When AUX-RAM is enabled, the instruction "MOVX @Ri" always accesses AUX-RAM. When the W78IRD2 is executing instructions from internal program memory, accessing AUX-RAM does not affect ports P0, P2, $\overline{WR}$ or $\overline{RD}$.

For example,

```
ANL   AUXR,#11111101B  ; Enable AUX-RAM
MOV   DPTR,#1234H
MOV   A,#56H
MOVX  @DPTR,A          ; Write 56h to address 1234H in external memory
MOV   XRAMAH,#02H      ; Only 2 LSB effective
MOV   R0,#34H
MOV   A,@R0            ; Read AUX-RAM data at address 0234H
```

5.2 Timers/Counters

The W78IRD2 has three timers/counters called Timer 0, Timer 1, and Timer 2. Each timer/counter consists of two 8-bit data registers: TL0 and TH0 for Timer 0, TL1 and TH1 for Timer 1, and TL2 and TH2 for Timer 2.

The operations of Timer 0 and Timer 1 are similar to those in the W78C52, and these timers are controlled by the TCON and TMOD registers.

Timer 2 is controlled by the T2CON register. Like Timers 0 and 1, Timer 2 can operate as either an external event counter or an internal timer, depending on the setting of bit C/T2 in T2CON. Timer 2 has

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	P0UP

Mnemonic: POPT Address: 86h

BIT	NAME	FUNCTION
1 – 7	-	Reserve
0	P0UP	0: Port 0 pins are open-drain. 1: Port 0 pins are internally pulled-up. Port 0 is structurally the same as Port 2.

Power Control

Bit:	7	6	5	4	3	2	1	0
	SMOD	SMOD0	-	POR	GF1	GF0	PD	IDL

Mnemonic: PCON Address: 87h

BIT	NAME	FUNCTION
7	SMOD	1: Double the serial-port baud rate in serial port modes 1, 2, and 3.
6	SMOD0	0: Framing Error Detection Disable. SCON.7 acts as per the standard 8052 function. 1: Framing Error Detection Enable. SCON.7 indicates a Frame Error and acts as the FE (FE_1) flag.
5	-	Reserved
4	POF	This bit is set to 1 when a power-on reset has occurred. It can be cleared by software.
3	GF1	General-purpose flag.
2	GF0	General-purpose flag.
1	PD	Set this bit to 1 to go into POWER DOWN mode.
0	IDL	Set this bit to 1 to go into IDLE mode.

Timer Control

Bit:	7	6	5	4	3	2	1	0
	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Mnemonic: TCON Address: 88h

Serial Data Buffer

Bit:	7	6	5	4	3	2	1	0
	SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0

Mnemonic: SBUF Address: 99h

BIT	NAME	FUNCTION
7~0	SBUF	Serial port data is read from or written to this location. It actually consists of two separate, internal 8-bit registers, the receive register and the transmit buffer. Any read access reads data from the receive register, while write access writes to the transmit buffer.

Port 2

Bit:	7	6	5	4	3	2	1	0
	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0

Mnemonic: P2 Address: A0h

Ram High Byte Address

Bit:	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	XRAMAH.1	XRAMAH.0

Mnemonic: XRAMAH Address: A1h

The AUX-RAM high byte address

Auxiliary 1 Register

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	GF2	0	-	DPS

Mnemonic: AUXR1 Address: A2h

BIT	NAME	FUNCTION
7~4	-	Reserved
3	GF2	General purpose, user–defined flag.
2	0	The bit cannot be written and is always read as 0.
1	-	Reserved
0	DPS	0 = switch to DPTR0 1 = switch to DPTR1

BIT	NAME	FUNCTION
7~0	SADEN	This register enables the Automatic Address Recognition feature of the serial port. When a bit in SADEN is set to 1, the same bit in SADDR is compared to the incoming serial data. When a bit in SADEN is set to 0, the same bit in SADDR is a "don't care" value in the comparison. The serial port interrupt occurs only if all the SADDR bits where SADEN is set to 1 match the incoming serial data.

On-Chip Programming Control

Bit:	7	6	5	4	3	2	1	0
	SWRST/ REBOOT	-	-	-	-	0	FBOOTSL	FPROGEN

Mnemonic: CHPCON Address: BFh

BIT	NAME	FUNCTION
7	W: SWRESET R: REBOOT	When FBOOTSL and FPROGEN are set to 1, set this bit to 1 to force the microcontroller to reset to the initial condition, just like power-on reset. This action re-boots the microcontroller and starts normal operation. Read this bit to determine whether or not a hardware reboot is in progress.
6 – 2	-	Reserved
1	FBOOTSL	Program Location Selection. This bit should be set before entering ISP mode. 0: The Loader Program is in the 64-KB AP Flash EPROM. The 4-KB LD Flash EPROM is the destination for re-programming. 1: The Loader Program is in the 4-KB memory bank. The 64-KB AP Flash EPROM is the destination for re-programming.
0	FPROGEN	FLASH EPROM Programming Enable. 1: Enable in-system programming mode. In this mode, erase, program and read operations are achieved during device enters idle state. 0: Disable in-system programming mode. The on-chip flash memory is read-only.

CHPCON has an unrestricted read access, however, the write access is protected by timed-access protection. See the section of timed-access protection for more information.

External Interrupt Control

Bit:	7	6	5	4	3	2	1	0
	PX3	EX3	IE3	IT3	PX2	EX2	IE2	IT2

Mnemonic: XICON Address: C0h

BIT	NAME	FUNCTION
7~2	-	Reserved
1	T2OE	Timer 2 Output Enable. This bit enables/disables the Timer 2 clock-out function.
0	DCEN	Down Count Enable: Setting DCEN to 1 allows T2EX pin to control the direction that Timer 2 counts in 16-bit auto-reload mode.

Timer 2 Capture Low

Bit:	7	6	5	4	3	2	1	0
	RCAP2L.7	RCAP2L.6	RCAP2L.5	RCAP2L.4	RCAP2L.3	RCAP2L.2	RCAP2L.1	RCAP2L.0

Mnemonic: RCAP2L Address: CAh

RCAP2L Timer 2 Capture LSB: In capture mode, RCAP2L is used to capture the TL2 value. In auto-reload mode, RCAP2L is used as the LSB of the 16-bit reload value.

Timer 2 Capture High

Bit:	7	6	5	4	3	2	1	0
	RCAP2H.7	RCAP2H.6	RCAP2H.5	RCAP2H.4	RCAP2H.3	RCAP2H.2	RCAP2H.1	RCAP2H.0

Mnemonic: RCAP2H Address: CBh

RCAP2H Timer 2 Capture HSB: In capture mode, RCAP2H is used to capture the TH2 value. In auto-reload mode, RCAP2H is used as the MSB of the 16-bit reload value.

Timer 2 Register Low

Bit:	7	6	5	4	3	2	1	0
	TL2.7	TL2.6	TLH2.5	TL2.4	TL2.3	TL2.2	TL2.1	TL2.0

Mnemonic: TL2 Address: CCh

TL2 Timer 2 LSB

Timer 2 Register High

Bit:	7	6	5	4	3	2	1	0
	TH2.7	TH2.6	TH2.5	TH2.4	TH2.3	TH2.2	TH2.1	TH2.0

Mnemonic: TH2 Address: CDh

TL2 Timer 2 MSB

Program Status Word

Bit:	7	6	5	4	3	2	1	0
	CY	AC	F0	RS1	RS0	OV	F1	P

Mnemonic: PSW Address: D0h

BIT	NAME	FUNCTION
7	CY	Carry flag: Set when an arithmetic operation results in a carry being generated from the ALU. It is also used as the accumulator for bit operations.
6	AC	Auxiliary carry: Set when the previous operation resulted in a carry from the high order nibble.
5	F0	General–purpose, user-defined flag 0.
4	RS1	Register bank select bits: See below.
3	RS0	Register bank select bits: See below.
2	OV	Overflow flag: Set when a carry was generated from the seventh bit but not from the eighth bit as a result of the previous operation, or vice-versa.
1	F1	General–purpose, user-defined flag 1.
0	P	Parity flag: Set and cleared by the hardware to indicate an odd or even number, respectively, of 1's in the accumulator.

RS.1-0: Register bank select bits:

RS1	RS0	REGISTER BANK	ADDRESS
0	0	0	00-07h
0	1	1	08-0Fh
1	0	2	10-17h
1	1	3	18-1Fh

PCA Counter Control Register

Bit:	7	6	5	4	3	2	1	0
	CF	CR	-	CCF4	CCF3	CCF2	CCF1	CCF0

Mnemonic: CCON Address: D8h

PCA Counter Mode Register

Bit:	7	6	5	4	3	2	1	0
	CIDL	WDTE	-	-	-	CPS1	CPS0	ECF

Mnemonic: CMOD Address: D9h

PCA Module 0 Register

Bit:	7	6	5	4	3	2	1	0
	-	ECOM0	CAPP0	CAPN0	MAT0	TOG0	PWM0	ECCF0

Mnemonic: CCAPM0 Address: DAh

Continued

BIT	NAME	FUNCTION
2	-	Reserved
1	-	Reserved
0	MD	Stretch MOVX select bits: This bit is used to select the stretch value for the MOVX instruction, which enables the microcontroller to access slower memory devices or peripherals transparently and without the need for external circuits. The RD or WR strobe and all internal timings are stretched by the selected interval. The default value is 1 cycle. For faster access, set the value to 0.

CKCON has an unrestricted read access, however, the write access is protected by timed-access protection. See the section of timed-access protection for more information.

Accumulator

Bit:	7	6	5	4	3	2	1	0
	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0

Mnemonic: ACC Address: E0h

ACC.7-0: The A (or ACC) register is the standard 8052 accumulator.

Port 4

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	P4.3/INT2	P4.2/INT3	P4.1	P4.0

Mnemonic: ACC Address: E8h

P4.3-0: Port 4 is a bi-directional I/O port with internal pull-ups.

BIT	NAME	FUNCTION
7 – 4	-	Reserved
3	P4.3	Port 4 Data bit which outputs to pin P4.3 in mode 0, or external interrupt $\overline{INT2}$.
2	P4.2	Port 4 Data bit which outputs to pin P4.2 in mode 0, or external interrupt $\overline{INT3}$.
1	P4.1	Port 4 Data bit which outputs to pin P4.1 in mode 0.
0	P4.0	Port 4 Data bit which outputs to pin P4.0 in mode 0.

PCA Counter Low Register

Bit:	7	6	5	4	3	2	1	0
	CL.7	CL.6	CL.6	CL.4	CL.3	CL.2	CL.1	CL.0

Mnemonic: CL Address: E9h

PCA Counter High Register

Bit:	7	6	5	4	3	2	1	0
	CH.7	CH.6	CH.6	CH.4	CH.3	CH.2	CH.1	CH.0

Mnemonic: CH Address: F9h

PCA Module 0 Compare/Capture High Register

Bit:	7	6	5	4	3	2	1	0
	CCAP0H.7	CCAP0H.6	CCAP0H.5	CCAP0H.4	CCAP0H.3	CCAP0H.2	CCAP0H.1	CCAP0H.0

Mnemonic: CCAP0H Address: FAh

PCA Module 1 Compare/Capture High Register

Bit:	7	6	5	4	3	2	1	0
	CCAP1H.7	CCAP1H.6	CCAP1H.5	CCAP1H.4	CCAP1H.3	CCAP1H.2	CCAP1H.1	CCAP1H.0

Mnemonic: CCAP1H Address: FBh

PCA Module 2 Compare/Capture High Register

Bit:	7	6	5	4	3	2	1	0
	CCAP2H.7	CCAP2H.6	CCAP2H.5	CCAP2H.4	CCAP2H.3	CCAP2H.2	CCAP2H.1	CCAP2H.0

Mnemonic: CCAP2H Address: FCh

PCA Module 3 Compare/Capture High Register

Bit:	7	6	5	4	3	2	1	0
	CCAP3H.7	CCAP3H.6	CCAP3H.5	CCAP3H.4	CCAP3H.3	CCAP3H.2	CCAP3H.1	CCAP3H.0

Mnemonic: CCAP3H Address: FDh

PCA Module 4 Compare/Capture High Register

Bit:	7	6	5	4	3	2	1	0
	CCAP4H.7	CCAP4H.6	CCAP4H.5	CCAP4H.4	CCAP4H.3	CCAP4H.2	CCAP4H.1	CCAP4H.0

Mnemonic: CCAP4H Address: FEh

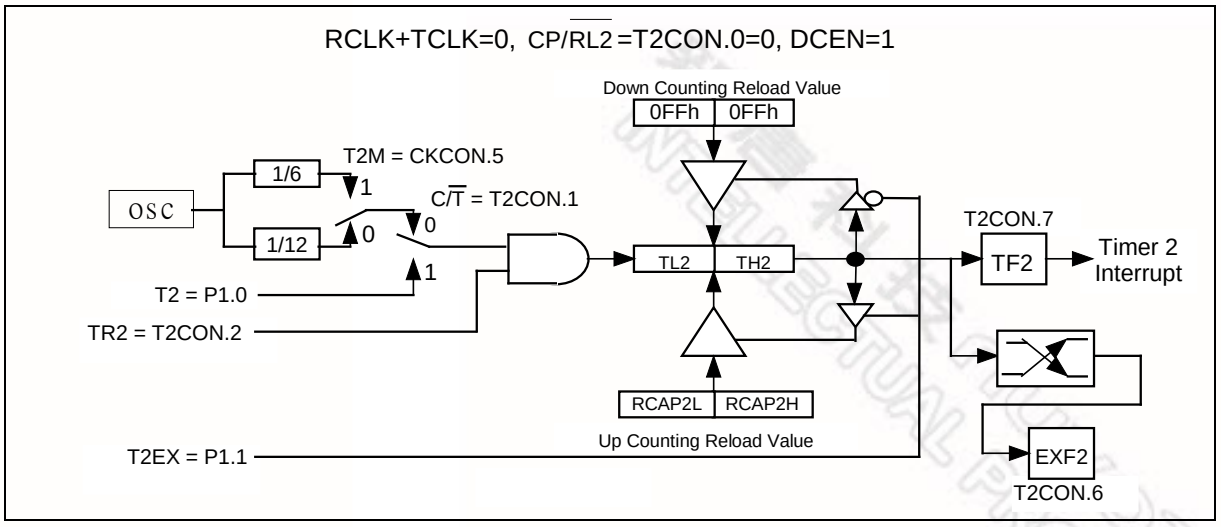


Figure 9-6 16-Bit Auto-reload Up/Down Counter

Baud Rate Generator Mode

Baud-rate generator mode is enabled by setting either the RCLK or TCLK bits in T2CON register. In baud-rate generator mode, Timer 2 is a 16-bit up-counter that automatically reloads when it overflows, but this overflow does not set the timer overflow bit TF2. If EXEN2 is set, then a negative transition on the T2EX pin sets EXF2 bit in T2CON and, if enabled, generates an interrupt request.

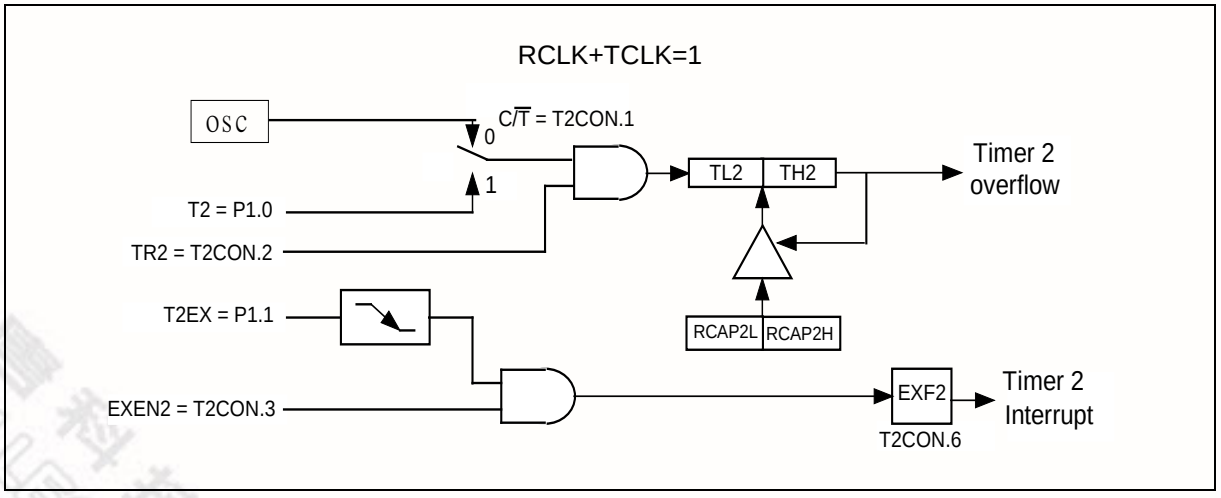


Figure 9-7 Baud Rate Generator Mode

10. ENHANCED FULL DUPLEX SERIAL PORT

The W78IRD2 serial port is a full-duplex port, and the W78IRD2 provides additional features such as frame-error detection and automatic address recognition. The serial port runs in one of four operating modes.

Serial Ports Modes

SM1	SM0	MODE	TYPE	BAUD CLOCK	FRAME SIZE	START BIT	STOP BIT	9TH BIT FUNCTION
0	0	0	Synch.	12 TCLKS	8 bits	No	No	None
0	1	1	Asynch.	Timer 1 or 2	10 bits	1	1	None
1	0	2	Asynch.	32 or 64 TCLKS	11 bits	1	1	0, 1
1	1	3	Asynch.	Timer 1 or 2	11 bits	1	1	0, 1

In synchronous mode (mode 0), the W78IRD2 generates the clock and operates in a half-duplex mode. In asynchronous modes (modes 1 – 3), full-duplex operation is available so that the serial port can simultaneously transmit and receive data. In any mode, register SBUF functions as both the transmit register and the receive buffer. Any write to SBUF writes to the transmit register, while any read from SBUF reads from the receive buffer. The rest of this section discusses each operating mode and then discusses frame-error detection and automatic address recognition.

10.1 MODE 0

Mode 0 is a half-duplex, synchronous mode. RxD transmits and receives serial data, and TxD transmits the shift clock. The TxD clock is provided by the W78IRD2. Eight bits are transmitted or received per frame, LSB first. The baud rate is fixed at 1/12 of the oscillator frequency. The functional block diagram is shown below.

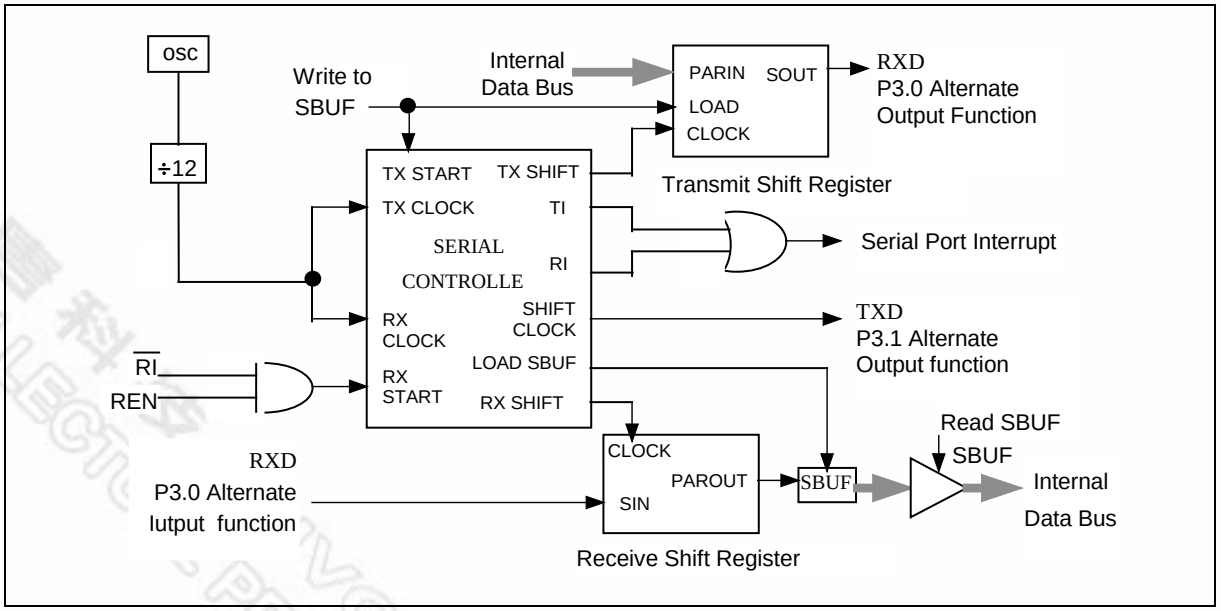


Figure 10-1 Serial Port Mode 0

Transmission begins when data is written to SBUF but is synchronized with the roll-over of Timer 1 (divided by 16 or 32, as configured) and not the write signal. The W78IRD2 waits until the next roll-over of Timer 1 (divided by 16 or 32) before the data is put on TxD. The next bit is placed on TxD after the next rollover. After all eight bits of data are transmitted, the stop bit is transmitted. Finally, the TI flag is set, at the tenth rollover after the write signal.

Reception is enabled only if REN is high. The W78IRD2 samples the RxD line at a rate of 16 times the selected baud rate, looking for a falling edge. When a falling edge is detected on the RxD pin, Timer 1 (divided by 16 or 32) is immediately reset to align the bit boundaries better, and the serial port starts receiving data. The 16 states of the counter effectively divide the time into 16 slices, and bit detection is done on a best-of-three basis using the eighth, ninth and tenth states. If the start bit is invalid (1), reception is aborted, and the serial port resumes looking for a falling edge on RxD. If the start bit is valid, the eight data bits are shifted in. Then, if

(1) RI = 0 and

(2) SM2 = 0 or the stop bit = 1,

the stop bit is put into RB8, the data is put in SBUF, and RI is set. Otherwise, the received frame may be lost. In the middle of the stop bit, the W78IRD2 resumes looking for falling edges on RxD.

10.3 MODE 2

Mode 2 is a full-duplex, asynchronous mode. Serial communication frames are made up of eleven bits transmitted on TXD and received on RXD. The eleven bits consist of a start bit (0), eight data bits (LSB first), a programmable ninth bit (TB8) and a stop bit (1). The ninth bit is read into and transmitted from RB8. The baud rate is either 1/32 or 1/64 of the oscillator frequency, and the 1/32 or 1/64 factor is determined by the SMOD bit in PCON SFR. The functional diagram is shown below.

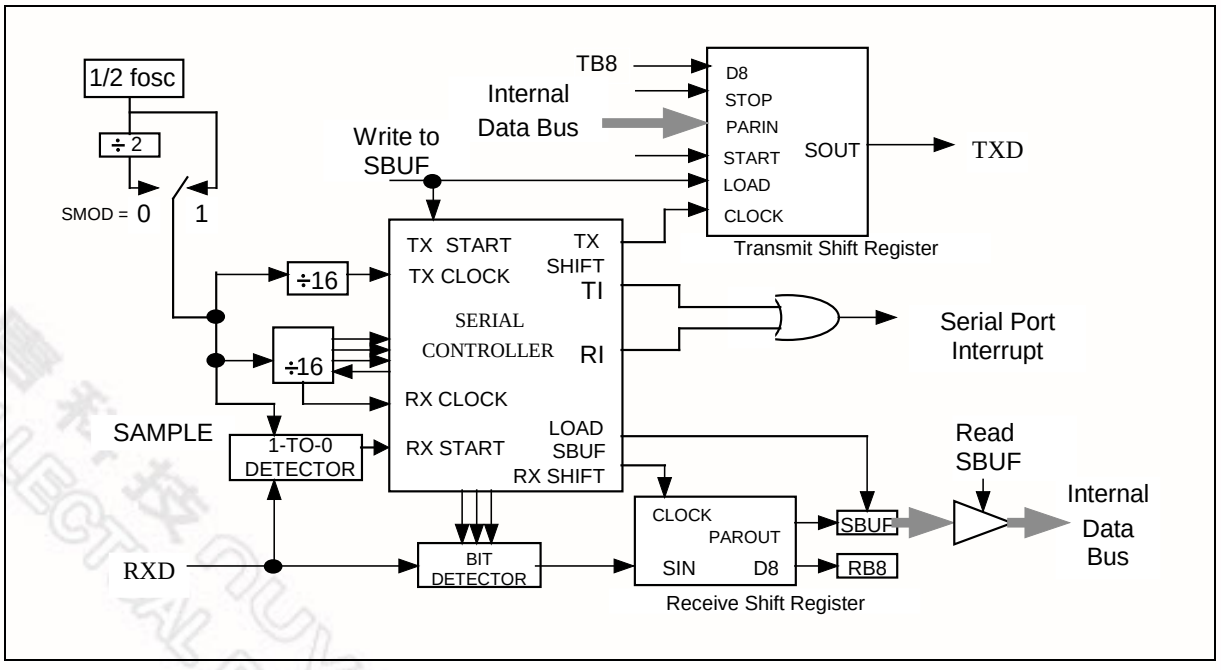


Figure 10-3 Serial Port Mode 2

Transmission begins when data is written to SBUF but is synchronized with the roll-over of the counter (divided by 32 or 64, as configured) and not the write signal. The W78IRD2 waits until the next roll-over

MODULE FUNCTION	ECOMN	CAPPN	CAPNN	MATN	TOGN	PWMN	ECCFN
No operation	0	0	0	0	0	0	0
16-bit capture by a positive edge trigger on CEXn	X	1	0	0	0	0	X
16-bit capture by a negative trigger on CEXn	X	0	1	0	0	0	X
16-bit capture by a transition on CEXn	X	1	1	0	0	0	X
16-bit Software Timer	1	0	0	1	0	0	X
16-bit High Speed Output	1	0	0	1	1	0	X
8-bit PWM	1	0	0	0	0	1	0
Watchdog Timer (only in module4)	1	0	0	1	X	0	X

PCA Module Modes (CCAPMn Register)

PWM enables pulse width modulation. The TOG bit causes the output CEX*n* to toggle when there is a match between the PCA counter and the module's compare/capture register. The match bit MAT causes the CCF bit in the CCON register to be set when there is a match between the PCA counter and the module's compare/capture register, and the ECCF bit enables the CCF flag to generate an interrupt. The bits CAPP and CAPN determine whether positive and negative edges, respectively, are captured. The bit ECOM enables the comparator function.

The PCA Timer is the common time-base for all five modules and can be programmed to select the appropriate timer source. The default value is 12 clocks (12T) per machine cycle, and 6T can also be selected by a bit in the options registers. The actual timer is then determined by the CPS1 and CPS2 bits in the CMOD SFR, as follows:

CPS1	CPS0	PCA TIMER COUNT SOURCE FOR 12T	PCA TIMER COUNT SOURCE FOR 6T
0	0	Oscillator frequency / 12	Oscillator frequency / 6
0	1	Oscillator frequency / 4	Oscillator frequency / 2
1	0	Timer 0 overflow	Timer 0 overflow
1	1	External input at ECI pin	External input at ECI pin

11.2 16-bit Software Timer Comparator Mode

The PCA modules can be used as software timers by setting both the ECOM and MAT bits in the CCAPMn register.

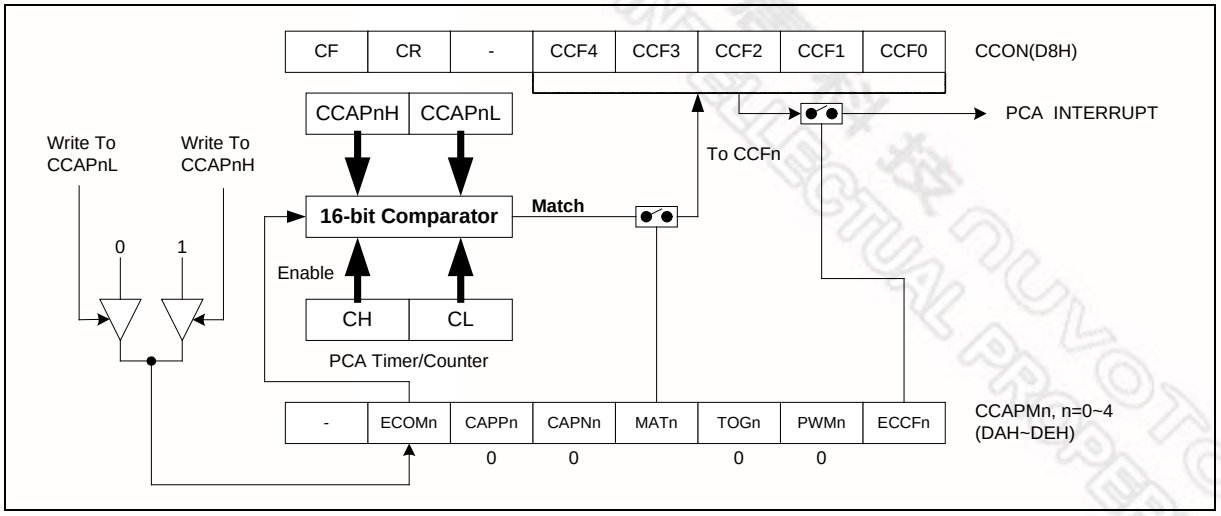


Figure 11-3 PCA 16-bit Timer Comparator Mode

In this mode, the PCA timer is compared to the module's capture registers. When a match occurs, an interrupt is generated if the CCFn (CCON) and ECCFn (CCAPMn) bits are set.

11.3 High Speed Output Mode

To activate this mode, the TOG, MAT, and ECOM (CCAPMn) bits must be set.

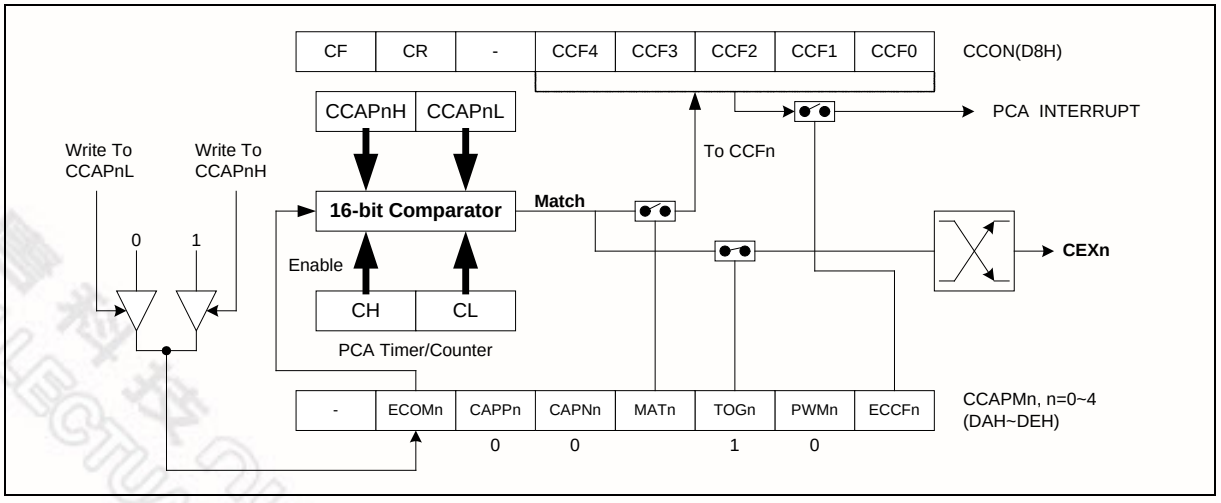


Figure 11-4 PCA High Speed Output Mode

In this mode, the CEX*n* output toggles each time a match occurs between the PCA counter and the module's capture registers.

14. TIMED-ACCESS PROTECTION

The W78IRD2 has features like Timer clock selecting by setting CKCON, software reset and ISP function that are crucial to the proper operation of the system. Consequently, The SFR CHPCON and CKCON, which control the functions, have restricted write access to protect CPU from errant operation. The W78IRD2 provides has a timed-access protection scheme that controls write access to critical bits.

In this scheme, protected bits have a timed write-enable window. A write is successful only if this window is active; otherwise, the write is discarded. The write-enable window is opened in two steps. First, the software writes 87h to the register CHPENR. This starts a counter, which expires in three machine cycles. Then, if the software writes 59h to CHPENR before the counter expires, the write-enable window is opened for three machine cycles. After three machine cycles, the window automatically closes, and the procedure must be repeated again to access protected bits.

The suggested code for opening the write-enable window is

```
CHPENR REG 0F6h      ; Define new register CHPENR, located at 0F6h
  MOV CHPENR, #87h
  MOV CHPENR, #59h
```

Five examples, some correct and some incorrect, of using timed-access protection are shown below.

Example 1: Valid access

```
  MOV CHPENR, #87h    ;3 M/C, Note: M/C = Machine Cycles
  MOV CHPENR, #59h    ;3 M/C
  MOV CKCON, #00h     ;3 M/C
```

Example 2: Valid access

```
  MOV CHPENR, #87h    ;3 M/C
  MOV CHPENR, #59h    ;3 M/C
  NOP                 ;1 M/C
  SETB  EWT           ;2 M/C
```

Example 3: Valid access

```
  MOV CHPENR, #87h    ;3 M/C
  MOV CHPENR, #59h    ;3 M/C
  ORL  CKCON, #01h    ;3M/C
```

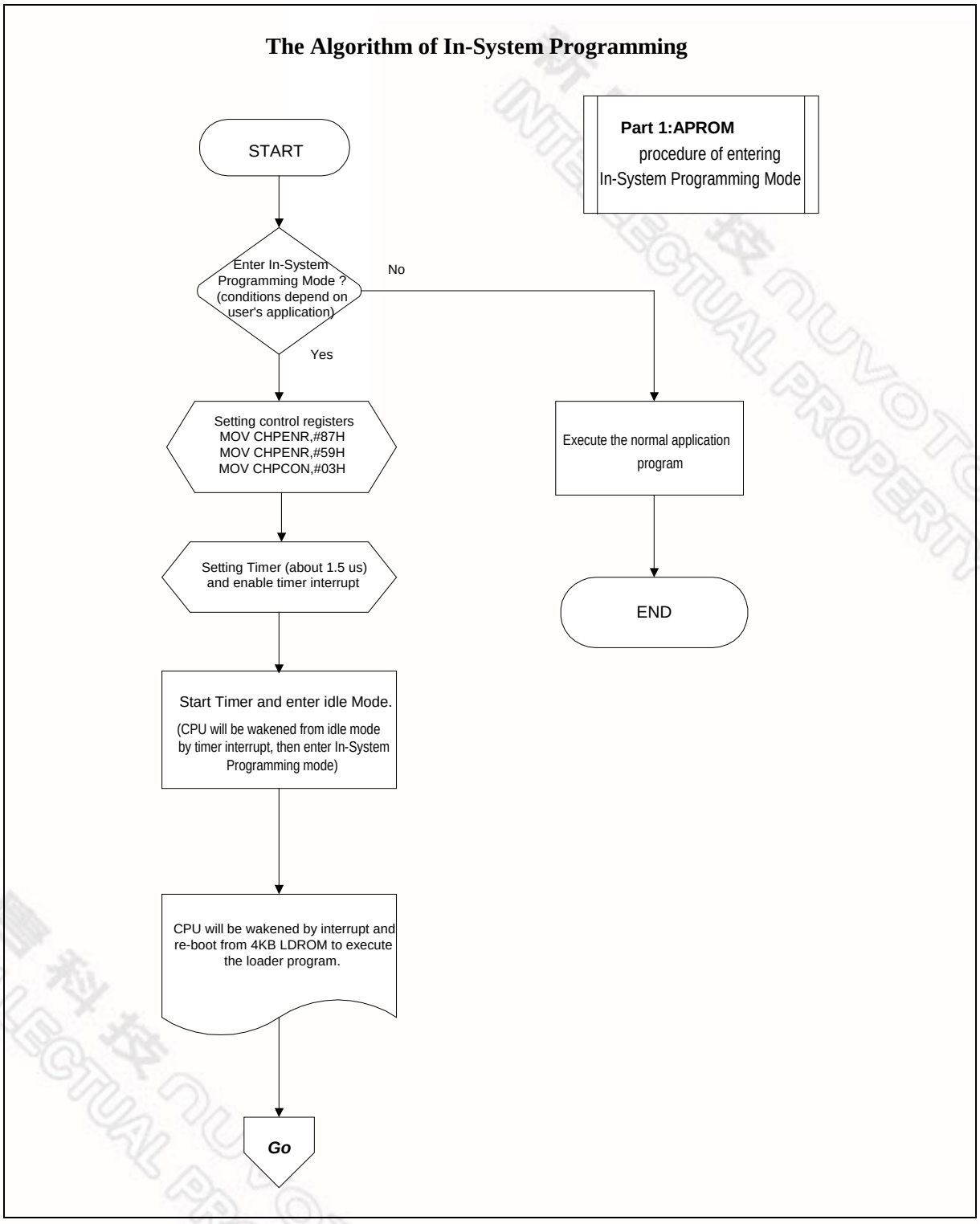
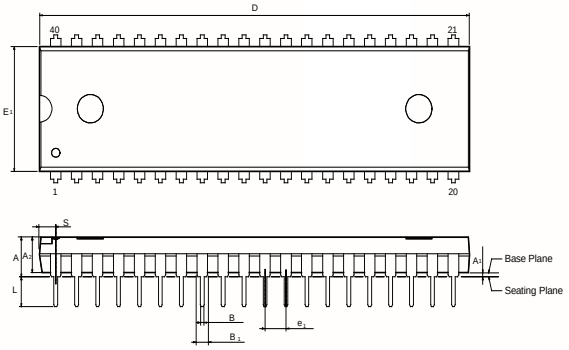


Figure 15-1 The algorithm of ISP for AP ROM

21. PACKAGE DIMENSIONS

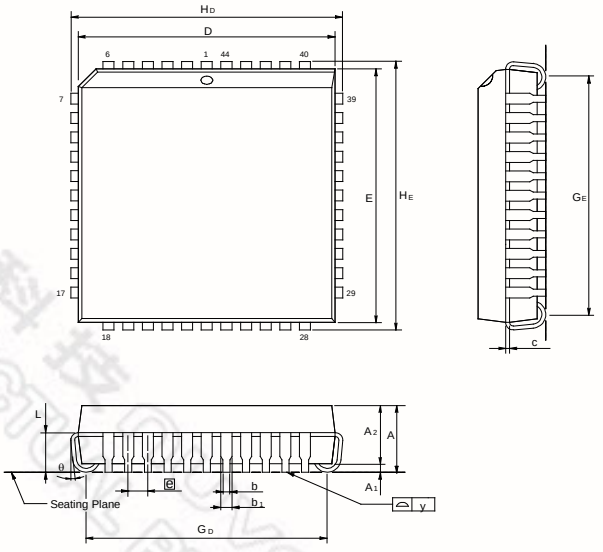
40-pin DIP



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.210	—	—	5.334
A_1	0.010	—	—	0.254	—	—
A_2	0.150	0.155	0.160	3.81	3.937	4.064
B	0.016	0.018	0.022	0.406	0.457	0.559
B_1	0.048	0.050	0.054	1.219	1.27	1.372
c	0.008	0.010	0.014	0.203	0.254	0.356
D	—	2.055	2.070	—	52.20	52.58
E	0.590	0.600	0.610	14.986	15.24	15.494
E_1	0.540	0.545	0.550	13.72	13.84	13.97
e_1	0.090	0.100	0.110	2.286	2.54	2.794
L	0.120	0.130	0.140	3.048	3.302	3.556
a	0	—	15	0	—	15
e_A	0.630	0.650	0.670	16.00	16.51	17.01
S	—	—	0.090	—	—	2.286

Notes:
1. Dimension D Max. & S include mold flash or tie bar burrs.
2. Dimension E1 does not include interlead flash.
3. Dimension D & E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dambar protrusion/intrusion.
5. Controlling dimension: Inches.
6. General appearance spec. should be based on final visual inspection spec.

44-pin PLCC



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.185	—	—	4.699
A_1	0.020	—	—	0.508	—	—
A_2	0.145	0.150	0.155	3.683	3.81	3.937
b_1	0.026	0.028	0.032	0.66	0.711	0.813
b	0.016	0.018	0.022	0.406	0.457	0.559
c	0.008	0.010	0.014	0.203	0.254	0.356
D	0.648	0.653	0.658	16.46	16.59	16.71
E	0.648	0.653	0.658	16.46	16.59	16.71
e	0.050 BSC			1.27 BSC		
G_D	0.590	0.610	0.630	14.99	15.49	16.00
G_E	0.590	0.610	0.630	14.99	15.49	16.00
H_D	0.680	0.690	0.700	17.27	17.53	17.78
H_E	0.680	0.690	0.700	17.27	17.53	17.78
L	0.090	0.100	0.110	2.296	2.54	2.794
y	—	—	0.004	—	—	0.10

Notes:
1. Dimension D & E do not include interlead flash.
2. Dimension b1 does not include dambar protrusion/intrusion.
3. Controlling dimension: Inches
4. General appearance spec. should be based on final visual inspection spec.

```
BLANK_CHECK_ERROR:
        MOV P1, #F0H
        MOV P3, #F0H
        JMP $

;*******************************************************************************
;* RE-PROGRAMMING 64KB AP Flash EPROM BANK
;*******************************************************************************
PROGRAM_64KROM:
        MOV DPTR, #0H       ; THE ADDRESS OF NEW ROM CODE
        MOV R2, #00H        ; TARGET LOW BYTE ADDRESS
        MOV R1, #00H        ; TARGET HIGH BYTE ADDRESS
        MOV DPTR, #0H       ; EXTERNAL SRAM BUFFER ADDRESS
        MOV SFRAH, R1       ; SFRAH, TARGET HIGH ADDRESS
        MOV SFRCN, #21H     ; SFRCN(C7H) = 21 (PROGRAM 64K)
        MOV R6, #5AH        ; SET TIMER FOR PROGRAMMING, ABOUT 50 μS.
        MOV R7, #FFH
        MOV TL0, R6
        MOV TH0, R7

PROG_D_64K:
        MOV SFRAL, R2       ; SFRAL(C4H) = LOW BYTE ADDRESS
        MOVX A, @DPTR       ; READ DATA FROM EXTERNAL SRAM BUFFER
        MOV SFRFD, A        ; SFRFD(C6H) = DATA IN
        MOV TCON, #10H      ; TCON = 10H, TR0 = 1, GO
        MOV PCON, #01H      ; ENTER IDLE MODE (PRORGAMMING)
        INC DPTR
        INC R2
        CJNE R2, #0H, PROG_D_64K
        INC  R1
        MOV SFRAH, R1
        CJNE R1, #0H, PROG_D_64K

;*******************************************************************************
; * VERIFY 64KB AP Flash EPROM BANK
;*******************************************************************************
        MOV R4, #03H        ; ERROR COUNTER
        MOV R6, #FBH        ; SET TIMER FOR READ VERIFY, ABOUT 1.5 μS.
        MOV R7, #FFH
        MOV TL0, R6
        MOV TH0, R7
        MOV DPTR, #0H       ; The start address of sample code
        MOV R2, #0H         ; Target low byte address
        MOV R1, #0H         ; Target high byte address
        MOV SFRAH, R1       ; SFRAH, Target high address
        MOV SFRCN, #00H     ; SFRCN = 00 (Read ROM CODE)

READ_VERIFY_64K:
        MOV SFRAL, R2       ; SFRAL(C4H) = LOW ADDRESS
        MOV TCON, #10H      ; TCON = 10H, TR0 = 1, GO
        MOV PCON, #01H
        INC R2
        MOVX A, @DPTR
        INC DPTR
        CJNE A, SFRFD, ERROR_64K
        CJNE R2, #0H, READ_VERIFY_64K
```