

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | 80C52 |
| Core Size | 8-Bit |
| Speed | 25MHz |
| Connectivity | EBI/EMI, UART/USART |
| Peripherals | POR, PWM, WDT |
| Number of I/O | 36 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 1.25K x 8 |
| Voltage - Supply (Vcc/Vdd) | 4.5V ~ 5.5V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-LCC (J-Lead) |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w78ird2a25pl |

## 1. GENERAL DESCRIPTION

The W78IRD2 is an 8-bit microcontroller which is pin- and instruction-set-compatible with the standard 80C52. The W78IRD2 contains a 64-KB Flash EPROM whose contents may be updated in-system by a loader program stored in an auxiliary, 4-KB Flash EPROM. Once the contents are confirmed, it can be protected for security.

The W78IRD2 also contains 256 bytes of on-chip RAM; 1 KB of auxiliary RAM; four 8-bit, bi-directional and bit-addressable I/O ports; an additional 4-bit port P4; three 16-bit timer/counters; and a serial port. These peripherals are all supported by nine interrupt sources with 4 levels of priority.

The W78IRD2 has two power-reduction modes: idle mode and power-down mode, both of which are software-selectable. Idle mode turns off the processor clock but allows peripherals to continue operating, while power-down mode stops the crystal oscillator for minimum power consumption. Power-down mode can be activated at any time and in any state without affecting the processor.

## 2. FEATURES

- 8-bit CMOS microcontroller
- Pin-compatible with standard 80C52
- Instruction-set compatible with 80C52
- Four 8-bit I/O ports; Port 0 has internal pull-up resisters enabled by software
- One extra 4-bit I/O port with interrupt and chip-select functions
- Three 16-bit timers
- Programmable clock out
- Programmable Counter Array (PCA) with PWM, Capture, Compare and Watchdog functions
- 9 interrupt sources with 4 levels of priority
- Full-duplex serial port with framing-error detection and automatic address recognition
- 64-KB, in-system-programmable, Flash EPROM (AP Flash EPRAOM)
- 4-KB auxiliary Flash EPROM for loader program (LD Flash EPROM)
- 256-byte on-chip RAM
- 1-KB auxiliary RAM, software-selectable
- Software Reset
- 12 clocks per machine cycle operation (default). Speed up to 20 MHz.
- 6 clocks per machine cycle operation set by the writer. Speed up to 12 MHz.
- 2 DPTR registers
- Low EMI (inhibit ALE)
- Built-in power management with idle mode and power down mode
- Code protection
- Packages:
  - Lead Free (RoHS) DIP 40: W78IRD2A25DL
  - Lead Free (RoHS) PLCC 44: W78IRD2A25PL

| BIT | NAME | FUNCTION |
|---|---|---|
| 7 | TF1 | Timer 1 overflow flag: This bit is set when Timer 1 overflows. It is cleared automatically when the program does a timer 1 interrupt service routine. It can also be set or cleared by software. |
| 6 | TR1 | 1: Turn on Timer 1.<br>0: Turn off Timer 1. |
| 5 | TF0 | Timer 0 overflow flag: This bit is set when Timer 0 overflows. It is cleared automatically when the program does a timer 0 interrupt service routine. It can also be set or cleared by software. |
| 4 | TR0 | 1: Turn on Timer 0.<br>0: Turn off Timer 0. |
| 3 | IE1 | Interrupt 1 Edge Detect: This bit is set by the hardware when a falling-edge / low-level is detected on $\overline{\mathrm{INT1}}$. If $\overline{\mathrm{INT1}}$ is edge-triggered, this bit is cleared by the hardware when the interrupt service routine begins. Otherwise, it follows the pin. |
| 2 | IT1 | Interrupt 1 type control<br>1: Interrupt 1 is triggered by a falling-edge on $\overline{\mathrm{INT1}}$.<br>0: Interrupt 1 is triggered by a low-level on $\overline{\mathrm{INT1}}$. |
| 1 | IE0 | Interrupt 0 Edge Detect: This bit is set by the hardware when a falling-edge / low-level is detected on $\overline{\mathrm{INT0}}$. If $\overline{\mathrm{INT0}}$ is edge-triggered, this bit is cleared by the hardware when the interrupt service routine begins. Otherwise, it follows the pin. |
| 0 | IT0 | Interrupt 0 type control<br>1: Interrupt 0 is triggered by a falling-edge on $\overline{\mathrm{INT0}}$.<br>0: Interrupt 0 is triggered by a low-level on $\overline{\mathrm{INT0}}$. |

**Timer Mode Control**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | GATE | C/$\overline{\mathrm{T}}$ | M1 | M0 | GATE | C/$\overline{\mathrm{T}}$ | M1 | M0 |

Mnemonic: TMOD Address: 89h

| BIT | NAME | FUNCTION |
|---|---|---|
| 7 | GATE | Gating control: When this bit is set, Timer/Counter 1 is enabled only while the $\overline{\mathrm{INT1}}$ pin is high and the TR1 control bit is set. When cleared, the $\overline{\mathrm{INT1}}$ pin has no effect, and Timer 1 is enabled whenever TR1 is set. |
| 6 | C/$\overline{\mathrm{T}}$ | Timer or Counter Select: When cleared, Timer 1 is incremented by the internal clock. When set, Timer 1 counts falling edges on the T1 pin. |
| 5 | M1 | Timer 1 Mode Select bits: See below. |
| 4 | M0 | Timer 1 Mode Select bits: See below. |

| BIT | NAME | FUNCTION |
|---|---|---|
| 7~0 | SADEN | This register enables the Automatic Address Recognition feature of the serial port. When a bit in SADEN is set to 1, the same bit in SADDR is compared to the incoming serial data. When a bit in SADEN is set to 0, the same bit in SADDR is a "don't care" value in the comparison. The serial port interrupt occurs only if all the SADDR bits where SADEN is set to 1 match the incoming serial data. |

### On-Chip Programming Control

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | SWRST/ REBOOT | - | - | - | - | 0 | FBOOTSL | FPROGEN |

Mnemonic: CHPCON Address: BFh

| BIT | NAME | FUNCTION |
|---|---|---|
| 7 | W: SWRESET<br>R: REBOOT | When FBOOTSL and FPROGEN are set to 1, set this bit to 1 to force the microcontroller to reset to the initial condition, just like power-on reset. This action re-boots the microcontroller and starts normal operation.<br>Read this bit to determine whether or not a hardware reboot is in progress. |
| 6 – 2 | - | Reserved |
| 1 | FBOOTSL | Program Location Selection. This bit should be set before entering ISP mode.<br>0: The Loader Program is in the 64-KB AP Flash EPROM. The 4-KB LD Flash EPROM is the destination for re-programming.<br>1: The Loader Program is in the 4-KB memory bank. The 64-KB AP Flash EPROM is the destination for re-programming. |
| 0 | FPROGEN | FLASH EPROM Programming Enable.<br>1: Enable in-system programming mode. In this mode, erase, program and read operations are achieved during device enters idle state.<br>0: Disable in-system programming mode. The on-chip flash memory is read-only. |

CHPCON has an unrestricted read access, however, the write access is protected by timed-access protection. See the section of timed-access protection for more information.

### External Interrupt Control

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | PX3 | EX3 | IE3 | IT3 | PX2 | EX2 | IE2 | IT2 |

Mnemonic: XICON Address: C0h

| BIT | NAME | FUNCTION |
|---|---|---|
| 7, 6 | P41FUN1<br>P41FUN0 | P4.1 function control bits, similar to P43FUN1 and P43FUN0 below. |
| 5, 4 | P41CMP1<br>P41CMP0 | P4.1 address-comparator length control bits, similar to P43CMP1 and P43CMP0 below. |
| 3, 2 | P40FUN1<br>P40FUN0 | P4.0 function control bits, similar to P43FUN1 and P43FUN0 below. |
| 1, 0 | P40CMP1<br>P40CMP0 | P4.0 address-comparator length control bits, similar to P43CMP1 and P43CMP0 below. |

## Port 4 Control Register B

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | P43FUN1 | P43FUN0 | P43CMP1 | P43CMP0 | P42FUN1 | P42FUN0 | P42CMP1 | P42CMP0 |

Mnemonic: P4CONB        Address: C3h

| BIT | NAME | FUNCTION |
|---|---|---|
| 7, 6 | P43FUN1<br>P43FUN0 | 00: Mode 0. P4.3 is a general purpose I/O port, like Port 1.<br>01: Mode 1. P4.3 is a read-strobe signal for chip-select purposes. The address range depends on SFR P43AH, P43AL, P43CMP1 and P43CMP0.<br>10: Mode 2. P4.3 is a write-strobe signal for chip-select purposes. The address range depends on SFR P43AH, P43AL, P43CMP1 and P43CMP0.<br>11: Mode 3. P4.3 is a read/write-strobe signal for chip-select purposes. The address range depends on SFR P43AH, P43AL, P43CMP1, and P43CMP0. |
| 5, 4 | P43CMP1<br>P43CMP0 | Chip-select signal address comparison:<br>00: Compare the full 16-bit address with P43AH and P43AL.<br>01: Compare the 15 MSB of the 16-bit address with P43AH and P43AL.<br>10: Compare the 14 MSB of the 16-bit address with P43AH and P43AL.<br>11: Compare the 8 MSB of the 16-bit address with P43AH. |
| 3, 2 | P42FUN1<br>P42FUN0 | P4.2 function control bits, similar to P43FUN1 and P43FUN0 above. |
| 1, 0 | P42CMP1<br>P42CMP0 | P4.2 address-comparator length control bits, similar to P43CMP1 and P43CMP0 above. |

| BIT | NAME | FUNCTION |
|---|---|---|
| 7~2 | - | Reserved |
| 1 | T2OE | Timer 2 Output Enable. This bit enables/disables the Timer 2 clock-out function. |
| 0 | DCEN | Down Count Enable: Setting DCEN to 1 allows T2EX pin to control the direction that Timer 2 counts in 16-bit auto-reload mode. |

**Timer 2 Capture Low**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | RCAP2L.7 | RCAP2L.6 | RCAP2L.5 | RCAP2L.4 | RCAP2L.3 | RCAP2L.2 | RCAP2L.1 | RCAP2L.0 |

Mnemonic: RCAP2L Address: CAh

RCAP2L Timer 2 Capture LSB: In capture mode, RCAP2L is used to capture the TL2 value. In auto-reload mode, RCAP2L is used as the LSB of the 16-bit reload value.

**Timer 2 Capture High**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | RCAP2H.7 | RCAP2H.6 | RCAP2H.5 | RCAP2H.4 | RCAP2H.3 | RCAP2H.2 | RCAP2H.1 | RCAP2H.0 |

Mnemonic: RCAP2H Address: CBh

RCAP2H Timer 2 Capture HSB: In capture mode, RCAP2H is used to capture the TH2 value. In auto-reload mode, RCAP2H is used as the MSB of the 16-bit reload value.

**Timer 2 Register Low**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | TL2.7 | TL2.6 | TLH2.5 | TL2.4 | TL2.3 | TL2.2 | TL2.1 | TL2.0 |

Mnemonic: TL2 Address: CCh

TL2 Timer 2 LSB

**Timer 2 Register High**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | TH2.7 | TH2.6 | TH2.5 | TH2.4 | TH2.3 | TH2.2 | TH2.1 | TH2.0 |

Mnemonic: TH2 Address: CDh

TL2 Timer 2 MSB

**Program Status Word**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | CY | AC | F0 | RS1 | RS0 | OV | F1 | P |

Mnemonic: PSW Address: D0h

### PCA Module 0 Compare/Capture Low Register

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | CCAP0L.7 | CCAP0L.6 | CCAP0L.5 | CCAP0L.4 | CCAP0L.3 | CCAP0L.2 | CCAP0L.1 | CCAP0L.0 |

Mnemonic: CCAP0L Address: EAh

### PCA Module 1 Compare/Capture Low Register

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | CCAP1L.7 | CCAP1L.6 | CCAP1L.5 | CCAP1L.4 | CCAP1L.3 | CCAP1L.2 | CCAP1L.1 | CCAP1L.0 |

Mnemonic: CCAP1L Address: EBh

### PCA Module 2 Compare/Capture Low Register

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | CCAP2L.7 | CCAP2L.6 | CCAP2L.5 | CCAP2L.4 | CCAP2L.3 | CCAP2L.2 | CCAP2L.1 | CCAP2L.0 |

Mnemonic: CCAP2L Address: ECh

### PCA Module 3 Compare/Capture Low Register

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | CCAP3L.7 | CCAP3L.6 | CCAP3L.5 | CCAP3L.4 | CCAP3L.3 | CCAP3L.2 | CCAP3L.1 | CCAP3L.0 |

Mnemonic: CCAP3L Address: EDh

### PCA Module 4 Compare/Capture Low Register

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | CCAP4L.7 | CCAP4L.6 | CCAP4L.5 | CCAP4L.4 | CCAP4L.3 | CCAP4L.2 | CCAP4L.1 | CCAP4L.0 |

Mnemonic: CCAP4L Address: EEh

### B Register

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | B.7 | B.6 | B.5 | B.4 | B.3 | B.2 | B.1 | B.0 |

Mnemonic: B Address: F0h

B.7-0: The B register is the standard 8052 register that serves as a second accumulator.

### Chip Enable Register

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | |

Mnemonic: CHPENR Address: F6h

**PCA Counter High Register**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | CH.7 | CH.6 | CH.6 | CH.4 | CH.3 | CH.2 | CH.1 | CH.0 |

Mnemonic: CH Address: F9h

**PCA Module 0 Compare/Capture High Register**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | CCAP0H.7 | CCAP0H.6 | CCAP0H.5 | CCAP0H.4 | CCAP0H.3 | CCAP0H.2 | CCAP0H.1 | CCAP0H.0 |

Mnemonic: CCAP0H Address: FAh

**PCA Module 1 Compare/Capture High Register**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | CCAP1H.7 | CCAP1H.6 | CCAP1H.5 | CCAP1H.4 | CCAP1H.3 | CCAP1H.2 | CCAP1H.1 | CCAP1H.0 |

Mnemonic: CCAP1H Address: FBh

**PCA Module 2 Compare/Capture High Register**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | CCAP2H.7 | CCAP2H.6 | CCAP2H.5 | CCAP2H.4 | CCAP2H.3 | CCAP2H.2 | CCAP2H.1 | CCAP2H.0 |

Mnemonic: CCAP2H Address: FCh

**PCA Module 3 Compare/Capture High Register**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | CCAP3H.7 | CCAP3H.6 | CCAP3H.5 | CCAP3H.4 | CCAP3H.3 | CCAP3H.2 | CCAP3H.1 | CCAP3H.0 |

Mnemonic: CCAP3H Address: FDh

**PCA Module 4 Compare/Capture High Register**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | CCAP4H.7 | CCAP4H.6 | CCAP4H.5 | CCAP4H.4 | CCAP4H.3 | CCAP4H.2 | CCAP4H.1 | CCAP4H.0 |

Mnemonic: CCAP4H Address: FEh

For example, the following program sets up P4.0 as a write-strobe signal for I/O port addresses 1234H – 1237H with positive polarity, while P4.1 – P4.3 are used as general I/O ports.

```
MOV  P40AH, #12H
MOV  P40AL, #34H            ; Base I/O address 1234H for P4.0
MOV  P4CONA, #00001010B     ; P4.0 is a write-strobe signal; address lines A0 and A1 are masked.
MOV  P4CONB, #00H           ; P4.1 – P4.3 are general I/O ports
MOV  P2ECON, #10H           ; Set P40SINV to 1 to invert the P4.0 write-strobe to positive polarity.
```

Then, any instruction MOVX @DPTR, A (where DPTR is in 1234H – 1237H) generates a positive-polarity, write-strobe signal on pin P4.0, while the instruction MOV P4, #XX puts bits 3 – 1 of data #XX on pins P4.3 – P4.1.

## 8. INTERRUPTS

This section provides more information about external interrupts $\overline{INT2}$ and $\overline{INT3}$ and provides an overview of interrupt priority levels and polling sequences.

### 8.1 External Interrupts 2 and 3

The W78IRD2 offers two additional external interrupts, $\overline{INT2}$ and $\overline{INT3}$, similar to external interrupts $\overline{INT0}$ and $\overline{INT1}$ in the standard 80C52. These interrupts are configured by the XICON (External Interrupt Control) register, which is not a standard register in the 80C52. Its address is 0C0H. XICON is bit-addressable; for example, "SETB 0C2H" sets the EX2 bit of XICON.

### 8.2 Interrupt Priority

Each interrupt has one of four priority levels in the W78IRD2, as shown below.

**Four-level interrupt priority**

| PRIORITY BITS | | INTERRUPT PRIORITY LEVEL |
|---|---|---|
| IPH.X | IP.X | |
| 0 | 0 | Level 0 (lowest priority) |
| 0 | 1 | Level 1 |
| 1 | 0 | Level 2 |
| 1 | 1 | Level 3 (highest priority) |

Interrupts with the same priority level are polled in the sequence indicated below.

**Nine-source interrupt information**

| INTERRUPT SOURCE | POLLING SEQUENCE WITHIN PRIORITY LEVEL | ENABLE REQUIRED SETTINGS | INTERRUPT TYPE EDGE/LEVEL | VECTOR ADDRESS |
|---|---|---|---|---|
| External Interrupt 0 | 0 (highest) | IE.0 | TCON.0 | 03H |
| Timer/Counter 0 | 1 | IE.1 | - | 0BH |
| External Interrupt 1 | 2 | IE.2 | TCON.2 | 13H |
| Timer/Counter 1 | 3 | IE.3 | - | 1BH |
| Programmable Counter Array | 4 | IE.6 | - | 33H |
| Serial Port | 5 | IE.4 | - | 23H |
| Timer/Counter 2 | 6 | IE.5 | - | 2BH |
| External Interrupt 2 | 7 | XICON.2 | XICON.0 | 33H |
| External Interrupt 3 | 8 (lowest) | XICON.6 | XICON.3 | 3BH |

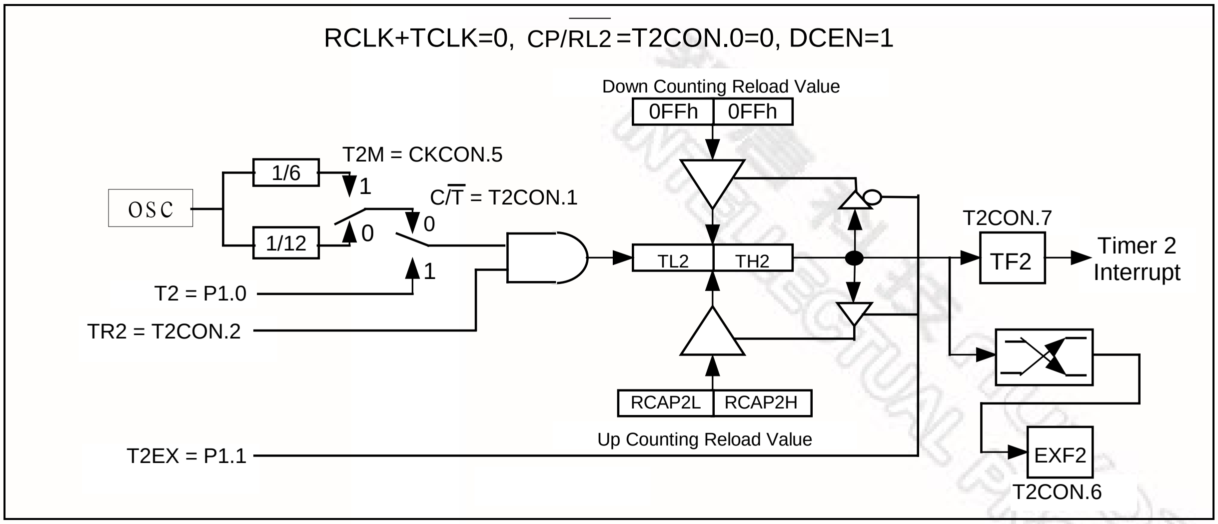



Figure 9-6 16-Bit Auto-reload Up/Down Counter

### Baud Rate Generator Mode

Baud-rate generator mode is enabled by setting either the RCLK or TCLK bits in T2CON register. In baud-rate generator mode, Timer 2 is a 16-bit up-counter that automatically reloads when it overflows, but this overflow does not set the timer overflow bit TF2. If EXEN2 is set, then a negative transition on the T2EX pin sets EXF2 bit in T2CON and, if enabled, generates an interrupt request.

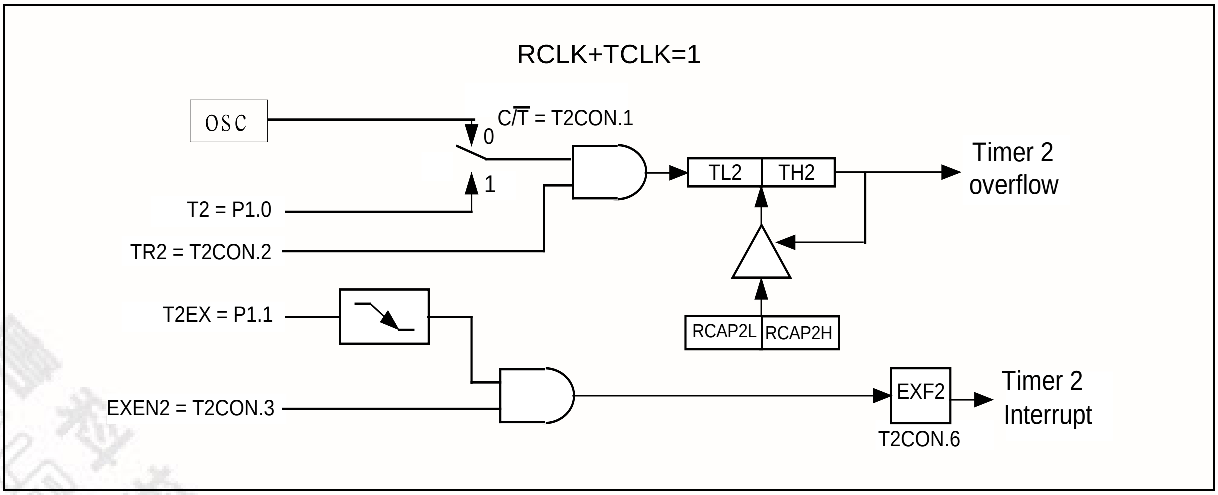



Figure 9-7 Baud Rate Generator Mode

nuvoTon

# 10. ENHANCED FULL DUPLEX SERIAL PORT

The W78IRD2 serial port is a full-duplex port, and the W78IRD2 provides additional features such as frame-error detection and automatic address recognition. The serial port runs in one of four operating modes.

**Serial Ports Modes**

| SM1 | SM0 | MODE | TYPE | BAUD CLOCK | FRAME SIZE | START BIT | STOP BIT | 9TH BIT FUNCTION |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | Synch. | 12 TCLKS | 8 bits | No | No | None |
| 0 | 1 | 1 | Asynch. | Timer 1 or 2 | 10 bits | 1 | 1 | None |
| 1 | 0 | 2 | Asynch. | 32 or 64 TCLKS | 11 bits | 1 | 1 | 0, 1 |
| 1 | 1 | 3 | Asynch. | Timer 1 or 2 | 11 bits | 1 | 1 | 0, 1 |

In synchronous mode (mode 0), the W78IRD2 generates the clock and operates in a half-duplex mode. In asynchronous modes (modes 1 – 3), full-duplex operation is available so that the serial port can simultaneously transmit and receive data. In any mode, register SBUF functions as both the transmit register and the receive buffer. Any write to SBUF writes to the transmit register, while any read from SBUF reads from the receive buffer. The rest of this section discusses each operating mode and then discusses frame-error detection and automatic address recognition.

## 10.1 MODE 0

Mode 0 is a half-duplex, synchronous mode. RxD transmits and receives serial data, and TxD transmits the shift clock. The TxD clock is provided by the W78IRD2. Eight bits are transmitted or received per frame, LSB first. The baud rate is fixed at 1/12 of the oscillator frequency. The functional block diagram is shown below.

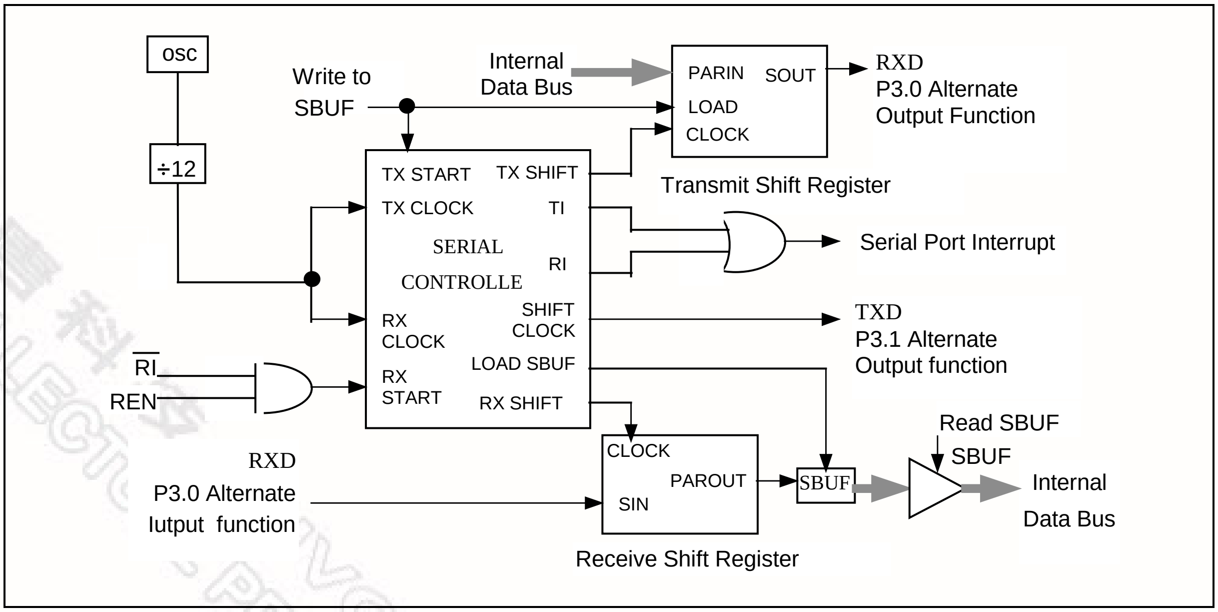



Figure 10-1 Serial Port Mode 0

## 10.5 Framing Error Detection

A frame error occurs when a valid stop bit is not detected. This could indicate incorrect serial data communication. Typically, the frame error is due to noise or contention on the serial communication line. The W78IRD2 has the ability to detect framing errors and set a flag which can be checked by software.

The frame error FE bit is located in SCON.7. This bit is normally used as SM0 in the standard 8051 family. However, in the W78IRD2 it serves a dual function and is called SM0/FE. There are actually two separate flags, one for SM0 and the other for FE. The flag that is actually accessed as SCON.7 is determined by SMOD0 (PCON.6) bit. When SMOD0 is set to 1, then the FE flag is accessed. When SMOD0 is set to 0, then the SM0 flag is accessed.

The FE bit is set to 1 by the hardware but must be cleared by software. Once FE is set, any frames received afterwards, even those without any errors, do not clear the FE flag. The flag has to be cleared by software. Note that SMOD0 must be set to 1 while reading or writing to FE.

## 10.6 Multi-Processor Communications

Multi-processor communication makes use of the 9th data bit in modes 2 and 3. In the W78IRD2, the RI flag is set only if the received byte corresponds to the Given or Broadcast address. This hardware feature eliminates the software overhead required in checking every received address and greatly simplifies the software programmer task.

In multi-processor communication mode, the address bytes are distinguished from the data bytes by the 9th bit, which is set high for address bytes. When the master processor wants to transmit a block of data to one of the slaves, it first sends out the address of the target slave (or slaves). All the slave processors should have their SM2 bit set high when waiting for an address byte. This ensures that they are interrupted only by the reception of an address byte. The automatic address recognition feature ensures that only the addressed slave is actually interrupted because the address comparison is done by the hardware, not the software.

The addressed slave clears the SM2 bit, thereby clearing the way to receive data bytes. With SM2 = 0, the slave is interrupted on the reception of every single complete frame of data. The unaddressed slaves are not affected, as they are still waiting for their address.

The Master processor can selectively communicate with groups of slaves by using the Given Address. All the slaves can be addressed together using the Broadcast Address. The addresses for each slave are defined in the SADDR and SADEN registers. The slave address is an eight-bit value specified in the SADDR SFR. The SADEN SFR is actually a mask for the byte value in SADDR. If a bit position in SADEN is 0, then the corresponding bit position in SADDR is don't care. Only those bit positions in SADDR whose corresponding bits in SADEN are 1 are used to obtain the Given Address. This gives the user flexibility to address multiple slaves without changing the slave address in SADDR.

The following example shows how the user can define the Given Address to address different slaves.

| MODULE FUNCTION | ECOMN | CAPPN | CAPNN | MATN | TOGN | PWMN | ECCFN |
|---|---|---|---|---|---|---|---|
| No operation | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 16-bit capture by a positive edge trigger on CEXn | X | 1 | 0 | 0 | 0 | 0 | X |
| 16-bit capture by a negative trigger on CEXn | X | 0 | 1 | 0 | 0 | 0 | X |
| 16-bit capture by a transition on CEXn | X | 1 | 1 | 0 | 0 | 0 | X |
| 16-bit Software Timer | 1 | 0 | 0 | 1 | 0 | 0 | X |
| 16-bit High Speed Output | 1 | 0 | 0 | 1 | 1 | 0 | X |
| 8-bit PWM | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| Watchdog Timer (only in module4) | 1 | 0 | 0 | 1 | X | 0 | X |

**PCA Module Modes (CCAPMn Register)**

PWM enables pulse width modulation. The TOG bit causes the output CEX*n* to toggle when there is a match between the PCA counter and the module's compare/capture register. The match bit MAT causes the CCF bit in the CCON register to be set when there is a match between the PCA counter and the module's compare/capture register, and the ECCF bit enables the CCF flag to generate an interrupt. The bits CAPP and CAPN determine whether positive and negative edges, respectively, are captured. The bit ECOM enables the comparator function.

The PCA Timer is the common time-base for all five modules and can be programmed to select the appropriate timer source. The default value is 12 clocks (12T) per machine cycle, and 6T can also be selected by a bit in the options registers. The actual timer is then determined by the CPS1 and CPS2 bits in the CMOD SFR, as follows:

| CPS1 | CPS0 | PCA TIMER COUNT SOURCE FOR 12T | PCA TIMER COUNT SOURCE FOR 6T |
|---|---|---|---|
| 0 | 0 | Oscillator frequency / 12 | Oscillator frequency / 6 |
| 0 | 1 | Oscillator frequency / 4 | Oscillator frequency / 2 |
| 1 | 0 | Timer 0 overflow | Timer 0 overflow |
| 1 | 1 | External input at ECI pin | External input at ECI pin |

## 12. HARDWARE WATCHDOG TIMER (ONE-TIME ENABLED WITH RESET-OUT)

The WDT is intended as a way to recover when the CPU may be subject to software problem. The WDT consists of a 14-bit counter and the WDT reset (WDTRST) register located at 0A6H. The WDT is disabled at reset. To enable the WDT, user must write 01EH and 0E1H in sequence to WDTRST.

Once the WDT is enabled, it increments every machine cycle, while the oscillator is running, and **there is no way to disable the WDT except through reset** (either hardware reset or WDT overflow reset). The program must reset the counter by writing 01EH and 0E1H to WDTRST before the WDT counter reaches 3FFFH (i.e., overflows). If it does overflow, it drives a HIGH pulse on the RST-pin. This pulse width is 98 source clocks in 12-clock mode or 49 source clocks in 6-clock mode. No external pull-down resistor or pull-up capacitor is required on the reset pin.

The WDT counter cannot be read or written. To make the best use of the WDT, the WDT should be reset in sections of code that are periodically executed in time to prevent a WDT reset.

## 13. DUAL DPTR

The dual DPTR structure is the way the chip specifies the address of an external data memory location. There are two 16-bit DPTR registers that address external memory. The DPS bit (AUXR1, bit 0) switches between them, and it can be toggled quickly by an INC AUXR1 instruction. (AUXR1, bit 2 cannot be written and is always read as a zero, so the INC AUXR1 instruction does not affect the GF2 bit that is higher in the AUXR1 register.)

It is important to keep track of the value of the DPS bit. For example, procedures and functions should save the DPS bit before switching between DPTR0 and DPTR1 and restore the original value afterwards to prevent other code from using the wrong memory.

# 20. TYPICAL APPLICATION CIRCUITS

## 20.1 External Program Memory and Crystal

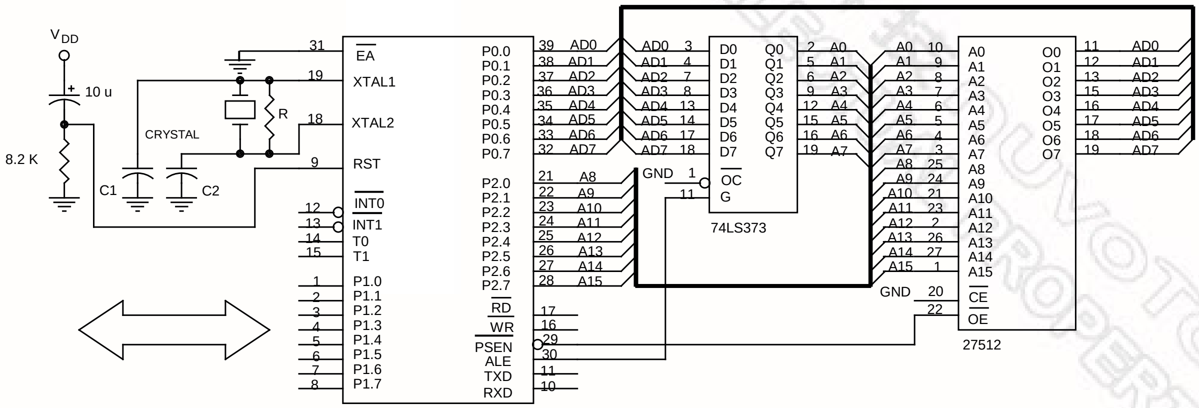



Figure 20-1

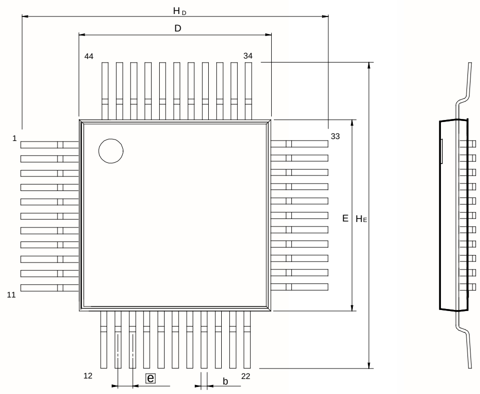
| CRYSTAL | C1 | C2 | R |
|---|---|---|---|
| 6 MHz | 47P | 47P | - |
| 16 MHz | 30P | 30P | - |
| 20 MHz | 15P | 15P | - |

Above table shows the reference values for crystal applications.

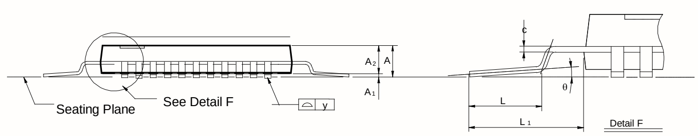
**Notes:**

1. For C1, C2 and R components, see Figure 20-1
2. The crystal should be as close as possible to the XTAL1 and XTAL2 pins on the application board.

## 44-pin PQFP




| Symbol | Dimension in inch | | | Dimension in mm | | |
|---|---|---|---|---|---|---|
| | Min. | Nom. | Max. | Min. | Nom. | Max. |
| A | --- | --- | --- | --- | --- | --- |
| $A_1$ | 0.002 | 0.01 | 0.02 | 0.05 | 0.25 | 0.5 |
| $A_2$ | 0.075 | 0.081 | 0.087 | 1.90 | 2.05 | 2.20 |
| b | 0.01 | 0.014 | 0.018 | 0.25 | 0.35 | 0.45 |
| c | 0.004 | 0.006 | 0.010 | 0.101 | 0.152 | 0.254 |
| D | 0.390 | 0.394 | 0.398 | 9.9 | 10.00 | 10.1 |
| E | 0.390 | 0.394 | 0.398 | 9.9 | 10.00 | 10.1 |
| $\boxed{e}$ | 0.025 | 0.031 | 0.036 | 0.635 | 0.80 | 0.952 |
| $H_D$ | 0.510 | 0.520 | 0.530 | 12.95 | 13.2 | 13.45 |
| $H_E$ | 0.510 | 0.520 | 0.530 | 12.95 | 13.2 | 13.45 |
| L | 0.025 | 0.031 | 0.037 | 0.65 | 0.8 | 0.95 |
| $L_1$ | 0.051 | 0.063 | 0.075 | 1.295 | 1.6 | 1.905 |
| y | — | — | 0.003 | — | — | 0.08 |
| θ | 0° | — | 7° | 0° | — | 7° |




Notes:

1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeter
4. General appearance spec. should be based on final visual inspection spec.

```
        ANL A, #80H
        CJNE A, #80H, UPDATE_64K; CHECK H/W REBOOT MODE ?

        MOV CHPCON, #03H   ; CHPCON = 03H, ENABLE IN-SYSTEM PROGRAMMING.
        MOV CHPENR, #00H   ; DISABLE CHPCON WRITE ATTRIBUTE

        MOV TCON, #00H      ; TCON = 00H, TR = 0 TIMER0 STOP
         MOV TMOD, #01H     ; TMOD = 01H, SET TIMER0 A 16BIT TIMER
        MOV IP, #00H        ; IP = 00H
        MOV IE, #82H        ; IE = 82H, TIMER0 INTERRUPT ENABLED
        MOV R6, #F0H
        MOV R7, #FFH
        MOV TL0, R6
        MOV TH0, R7
        MOV TCON, #10H      ; TCON = 10H, TR0 = 1, GO
        MOV PCON, #01H      ; ENTER IDLE MODE

 UPDATE_64K:
        MOV CHPENR, #00H  ; DISABLE CHPCON WRITE-ATTRIBUTE
        MOV TCON, #00H      ; TCON = 00H, TR = 0 TIM0 STOP
        MOV IP, #00H        ; IP = 00H
        MOV IE, #82H        ; IE = 82H, TIMER0 INTERRUPT ENABLED
        MOV TMOD, #01H      ; TMOD = 01H, MODE1
        MOV R6, #3CH        ; SET WAKE-UP TIME FOR ERASE OPERATION, ABOUT 15 ms. DEPENDING
                            ; ON USER'S SYSTEM CLOCK RATE.
        MOV R7, #B0H
        MOV TL0, R6
        MOV TH0, R7

ERASE_P_4K:
        MOV SFRCN, #22H     ; SFRCN(C7H) = 22H  ERASE 64K
        MOV TCON, #10H      ; TCON = 10H, TR0 = 1, GO
        MOV PCON, #01H      ; ENTER IDLE MODE (FOR ERASE OPERATION)

;*********************************************************************
;* BLANK CHECK
;*********************************************************************
        MOV SFRCN, #0H      ; READ 64KB AP Flash EPROM MODE
        MOV SFRAH, #0H      ; START ADDRESS = 0H
        MOV SFRAL, #0H
         MOV R6, #FBH       ; SET TIMER FOR READ OPERATION, ABOUT 1.5 µS.
        MOV R7, #FFH
        MOV TL0, R6
        MOV TH0, R7

BLANK_CHECK_LOOP:
        SETB TR0            ; ENABLE TIMER 0
        MOV PCON, #01H      ; ENTER IDLE MODE
        MOV A, SFRFD        ; READ ONE BYTE
        CJNE A, #FFH, BLANK_CHECK_ERROR
        INC SFRAL           ; NEXT ADDRESS
        MOV A, SFRAL
        JNZ BLANK_CHECK_LOOP
        INC SFRAH
        MOV A, SFRAH
        CJNE A, #0H, BLANK_CHECK_LOOP   ; END ADDRESS = FFFFH
        JMP PROGRAM_64KROM
```

```
BLANK_CHECK_ERROR:
        MOV P1, #F0H
        MOV P3, #F0H
        JMP $

;*****************************************************************************
;* RE-PROGRAMMING 64KB AP Flash EPROM BANK
;*****************************************************************************
PROGRAM_64KROM:
        MOV DPTR, #0H           ; THE ADDRESS OF NEW ROM CODE
        MOV R2, #00H            ; TARGET LOW BYTE ADDRESS
        MOV R1, #00H            ; TARGET HIGH BYTE ADDRESS
        MOV DPTR, #0H           ; EXTERNAL SRAM BUFFER ADDRESS
        MOV SFRAH, R1           ; SFRAH, TARGET HIGH ADDRESS
        MOV SFRCN, #21H         ; SFRCN(C7H) = 21 (PROGRAM 64K)
        MOV R6, #5AH            ; SET TIMER FOR PROGRAMMING, ABOUT 50 µS.
        MOV R7, #FFH
        MOV TL0, R6
        MOV TH0, R7

PROG_D_64K:
        MOV SFRAL, R2           ; SFRAL(C4H) = LOW BYTE ADDRESS
        MOVX A, @DPTR           ; READ DATA FROM EXTERNAL SRAM BUFFER
        MOV SFRFD, A            ; SFRFD(C6H) = DATA IN
        MOV TCON, #10H          ; TCON = 10H, TR0 = 1, GO
        MOV PCON, #01H          ; ENTER IDLE MODE (PRORGAMMING)
        INC DPTR
        INC R2
        CJNE R2, #0H, PROG_D_64K
        INC  R1
        MOV SFRAH, R1
        CJNE R1, #0H, PROG_D_64K

;*****************************************************************************
; * VERIFY 64KB AP Flash EPROM BANK
;*****************************************************************************
        MOV R4, #03H            ; ERROR COUNTER
        MOV R6, #FBH            ; SET TIMER FOR READ VERIFY, ABOUT 1.5 µS.
        MOV R7, #FFH
        MOV TL0, R6
        MOV TH0, R7
        MOV DPTR, #0H           ; The start address of sample code
        MOV R2, #0H             ; Target low byte address
        MOV R1, #0H             ; Target high byte address
        MOV SFRAH, R1           ; SFRAH, Target high address
        MOV SFRCN, #00H         ; SFRCN = 00 (Read ROM CODE)

READ_VERIFY_64K:
        MOV SFRAL, R2           ; SFRAL(C4H) = LOW ADDRESS
        MOV TCON, #10H          ; TCON = 10H, TR0 = 1, GO
        MOV PCON, #01H
        INC R2
        MOVX A, @DPTR
        INC DPTR
        CJNE A, SFRFD, ERROR_64K
        CJNE R2, #0H, READ_VERIFY_64K
```

nuvoTon

## 23. REVISION HISTORY

| VERSION | DATE | PAGE | DESCRIPTION |
|---|---|---|---|
| A1 | June 2004 | - | Initial Issued |
| A2 | August 2004 | 38 | Modify the content of PCA |
| | | 74 | Add the application of PCA |
| A3 | Sep. 30, 2004 | 38 | Add Enhanced full duplex serial port with framing error detection and automatic address recognition |
| A4 | April 20, 2005 | 72 | Add Important Notice |
| A5 | June 2, 2005 | 4<br>17<br>22<br>38 | To add Lead Free part No. of packages.<br>Correct GF3 to GF2 in AUXR1<br>Correct XICONH<br>Add Programmable Timers/Counters. |
| A6 | Sep. 5, 2005 | -<br>50 | Re-organize document.<br>Add a section of timed-access protection. |
| A7 | October 2, 2006 | | Remove block diagram |
| | | | Change operating frequency into 20MHz |
| | | 3 | Remove all Leaded parts |

## Important Notice

**Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, "Insecure Usage".**

**Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.**

**All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.**