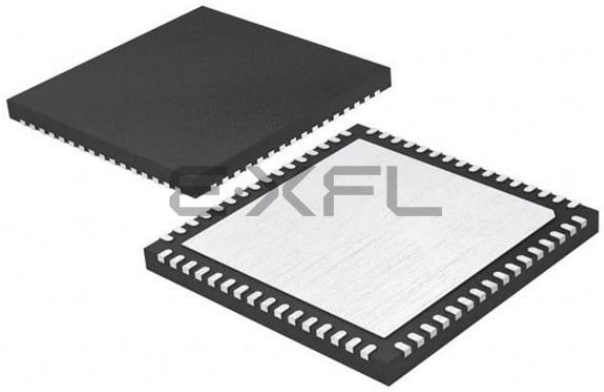
# Microchip Technology - PIC24FJ128GC006-I/MR Datasheet



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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 16-Bit |
| Speed | 32MHz |
| Connectivity | I²C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, LCD, LVD, POR, PWM, WDT |
| Number of I/O | 53 |
| Program Memory Size | 128KB (43K x 24) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 3.6V |
| Data Converters | A/D 29x12b, 2x16b; D/A 2x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-VFQFN Exposed Pad |
| Supplier Device Package | 64-VQFN (9x9) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic24fj128gc006-i-mr |

**TABLE 1: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 64-PIN DEVICES**

| Pin | Function | Pin | Function |
|---|---|---|---|
| 1 | CTED4/PMD5/LCDBIAS2/CN63/RE5 | 33 | AN30/SEG12/**RP16**/USBID/PMA12/CN71/RF3 |
| 2 | PMD6/LCDBIAS1/CN64/RE6 | 34 | VBUS/CN83 |
| 3 | PMD7/LCDBIAS0/CN65/RE7 | 35 | VUSB3V3 |
| 4 | BGBUF2/AN17/OA1P1/C1IND/SEG0/**RP21**/T5CK/PMA5/CN8/RG6 | 36 | D-/CN73/RG3 |
| 5 | VLCAP1/AN18/OA1N4/C1INC/**RP26**/PMA4/CN9/RG7 | 37 | D+/CN72/RG2 |
| 6 | VLCAP2/AN19/OA1N3/C2IND/**RP19**/PMA3/CN10/RG8 | 38 | VDD |
| 7 | $\overline{\text{MCLR}}$ | 39 | OSCI/CLKI/CN23/RC12 |
| 8 | AN49/OA1P0/C2INC/SEG1/DAC1/**RP27**/PMA2/CN11/RG9 | 40 | OSCO/CLKO/CN22/RC15 |
| 9 | VSS | 41 | VSS |
| 10 | VDD | 42 | AN40/SEG13/**RP2**/RTCC/DMLN/OCTRIG1/PMA13/CN53/RD8 |
| 11 | PGEC3/AN5/OA1OUT/C1INA/SEG2/**RP18**/CN7/RB5 | 43 | AN24/SEG14/**RP4**/SDA1/DPLN/PMACK2/CN54/RD9 |
| 12 | PGED3/AN4/OA1N0/C1INB/SEG3/**RP28**/USBOEN/CN6/RB4 | 44 | AN41/C3IND/SEG15/**RP3**/SCL1/PMA15/CS2/CN55/RD10 |
| 13 | AN3/OA2OUT/C2INA/SEG4/VPIO/CN5/RB3 | 45 | TMS/AN42/OA2P0/C3INC/SEG16/**RP12**/PMA14/CS1/CN56/RD11 |
| 14 | AN2/OA2N2/CTCMP/C2INB/SEG5/**RP13**/T4CK/VMIO/CTED13/PMA7/CN4/RB2 | 46 | AN43/OA2N0/SEG17/**RP11**/VCMPST3/DMH/INT0/CN49/RD0 |
| 15 | PGEC1/CVREF-/AVREF-/AN1/OA2P1/SEG6/**RP1**/CTED12/CN3/RB1 | 47 | SOSCI/RC13 |
| 16 | PGED1/CVREF+/AVREF+/DVREF+/BGBUF1/AN0/SEG7/**RP0**/PMA6/CN2/RB0 | 48 | PWRLCLK/SOSCO/**RPI37**/SCLKI/RC14 |
| 17 | PGEC2/AN6/OA1P3/**RP6**/LCDBIAS3/CN24/RB6 | 49 | AN35/SEG20/**RP24**/CN50/RD1**(1)** |
| 18 | PGED2/AN7/COM6/SEG30/**RP7**/CN25/RB7 | 50 | AN25/OA2N1/SEG21/**RP23**/DPH/PMACK1/CN51/RD2 |
| 19 | AVDD | 51 | AN44/OA2P4/SEG22/**RP22**/PMBE0/CN52/RD3 |
| 20 | AVSS | 52 | AN47/OA1P4/SEG23/**RP25**/PMWR/CN13/RD4 |
| 21 | SVSS | 53 | AN48/OA1N1/SEG24/**RP20**/PMRD/CN14/RD5 |
| 22 | CH0+ | 54 | AN34/OA1P2/C3INB/SEG25/CN15/RD6 |
| 23 | CH0- | 55 | AN20/C3INA/SEG26/CN16/RD7 |
| 24 | CH1+/SVREF+ | 56 | VCAP |
| 25 | CH1-/CH1SE/SVREF- | 57 | VBAT |
| 26 | SVDD | 58 | COM7/SEG27/VCMPST1/CN68/RF0 |
| 27 | TCK/AN12/COM5/SEG18/T1CK/CTED2/PMA11/CN30/RB12 | 59 | COM4/SEG47/VCMPST2/CN69/RF1 |
| 28 | TDI/AN13/OA2P3/SEG19/DAC2/CTED1/PMA10/CN31/RB13 | 60 | COM3/PMD0/CN58/RE0 |
| 29 | TDO/AN14/OA2N4/SEG8/**RP14**/CTED5/CTPLS/PMA1/CN32/RB14 | 61 | COM2/PMD1/CN59/RE1 |
| 30 | AN15/SEG9/**RP29**/T2CK/REFO/CTED6/PMA0/CN12/RB15 | 62 | COM1/PMD2/CN60/RE2 |
| 31 | AN11/OA2N3/SEG10/**RP10**/SDA2/T3CK/PMA9/CN17/RF4 | 63 | COM0/CTED9/PMD3/CN61/RE3 |
| 32 | CVREF/AN10/OA2P2/SEG11/**RP17**/SCL2/PMA8/CN18/RF5 | 64 | HLVDIN/SEG62/CTED8/PMD4/CN62/RE4 |

**Legend:** **RPn** and **RPIn** represent remappable pins for Peripheral Pin Select (PPS) functions.

**Note 1:** RD1 is an analog pin and implements the AN35/SEG20/RP24/CN50/RD1 functions. However, there is not an ANSx bit associated with the RD1 port. Using the RD1 pin for the AN35 function would cause a worst-case increase in device current consumption of 500 µA.

## 2.7 Configuration of Analog and Digital Pins During ICSP Operations

If an ICSP compliant emulator is selected as a debugger, it automatically initializes all of the A/D input pins (ANx) as “digital” pins. Depending on the particular device, this is done by setting all bits in the ADxPCFG register(s) or clearing all bits in the ANSx registers.

All PIC24F devices will have either one or more ADxPCFG registers or several ANSx registers (one for each port); no device will have both. Refer to **Section 11.2 “Configuring Analog Port Pins (ANSx)”** for more specific information.

The bits in these registers that correspond to the A/D pins that initialized the emulator must not be changed by the user application firmware; otherwise, communication errors will result between the debugger and the device.

If your application needs to use certain A/D pins as analog input pins during the debug session, the user application must modify the appropriate bits during initialization of the A/D module, as follows:

- For devices with an ADxPCFG register, clear the bits corresponding to the pin(s) to be configured as analog. Do not change any other bits, particularly those corresponding to the PGECx/PGEDx pair, at any time.
- For devices with ANSx registers, set the bits corresponding to the pin(s) to be configured as analog. Do not change any other bits, particularly those corresponding to the PGECx/PGEDx pair, at any time.

When a Microchip debugger/emulator is used as a programmer, the user application firmware must correctly configure the ADxPCFG or ANSx registers. Automatic initialization of these registers is only done during debugger operation. Failure to correctly configure the register(s) will result in all A/D pins being recognized as analog input pins, resulting in the port value being read as a logic ‘0’, which may affect user application functionality.

## 2.8 Sigma-Delta A/D Connections

The Sigma-Delta A/D Converter has input and power connections that are independent from the rest of the microcontroller. These connections are required to use the converter, and are in addition to the connection and layout connections provided in **Section 2.1 “Basic Connection Requirements”** and **Section 2.2 “Power Supply Pins”**.

### 2.8.1 VOLTAGE AND GROUND CONNECTIONS

To minimize noise interference, the Sigma-Delta A/D Converter has independent voltage pins. Converter circuits are supplied through the $SV_{DD}$ pin. Independent ground return is provided through the $SV_{SS}$ pin.

As with the microcontroller’s $V_{DD}/V_{SS}$ and $AV_{DD}/AV_{SS}$ pins, bypass capacitors are required on $SV_{DD}$ and $SV_{SS}$. Requirements for these capacitors are identical to those for the $V_{DD}/V_{SS}$ and $AV_{DD}/AV_{SS}$ pins.

It is recommended that designs using the Sigma-Delta A/D Converter incorporate a separate ground return path for analog circuits. The analog and digital grounds may be tied to a single point at the power source. Analog pins that require grounding should be tied to this analog return. $SV_{SS}$ can be tied to the digital ground, along with $V_{SS}$ and $AV_{SS}$.

### 2.8.2 ANALOG INPUTS

The analog signals to be converted are connected to the pins of CH0 and/or CH1. Each channel has inverting and non-inverting inputs (CHx- and CHx+, respectively), and is fully differential.

If not used for conversion, CH1+ and CH1- can be used to supply an external voltage reference to the converter. If an external reference is not used and CH1 is not needed as a conversion input, both pins should be connected to the analog ground return.

## 2.9 Unused I/Os

Unused I/O pins should be configured as outputs and driven to a logic low state. Alternatively, connect a 1 kΩ to 10 kΩ resistor to $V_{SS}$ on unused pins and drive the output to logic low.

### 4.3.2 DATA ACCESS FROM PROGRAM MEMORY USING TABLE INSTRUCTIONS

The TBLRDL and TBLWTL instructions offer a direct method of reading or writing the lower word of any address within the program space without going through Data Space. The TBLRDH and TBLWTH instructions are the only method to read or write the upper 8 bits of a program space word as data.

The PC is incremented by two for each successive 24-bit program word. This allows program memory addresses to directly map to Data Space addresses. Program memory can thus be regarded as two, 16-bit word-wide address spaces, residing side by side, each with the same address range. TBLRDL and TBLWTL access the space which contains the least significant data word, and TBLRDH and TBLWTH access the space which contains the upper data byte.

Two table instructions are provided to move byte or word-sized (16-bit) data to and from program space. Both function as either byte or word operations.

1. TBLRDL (Table Read Low): In Word mode, it maps the lower word of the program space location (P<15:0>) to a data address (D<15:0>).

   In Byte mode, either the upper or lower byte of the lower program word is mapped to the lower byte of a data address. The upper byte is selected when byte select is '1'; the lower byte is selected when it is '0'.

2. TBLRDH (Table Read High): In Word mode, it maps the entire upper word of a program address (P<23:16>) to a data address. Note that D<15:8>, the 'phantom' byte, will always be '0'.

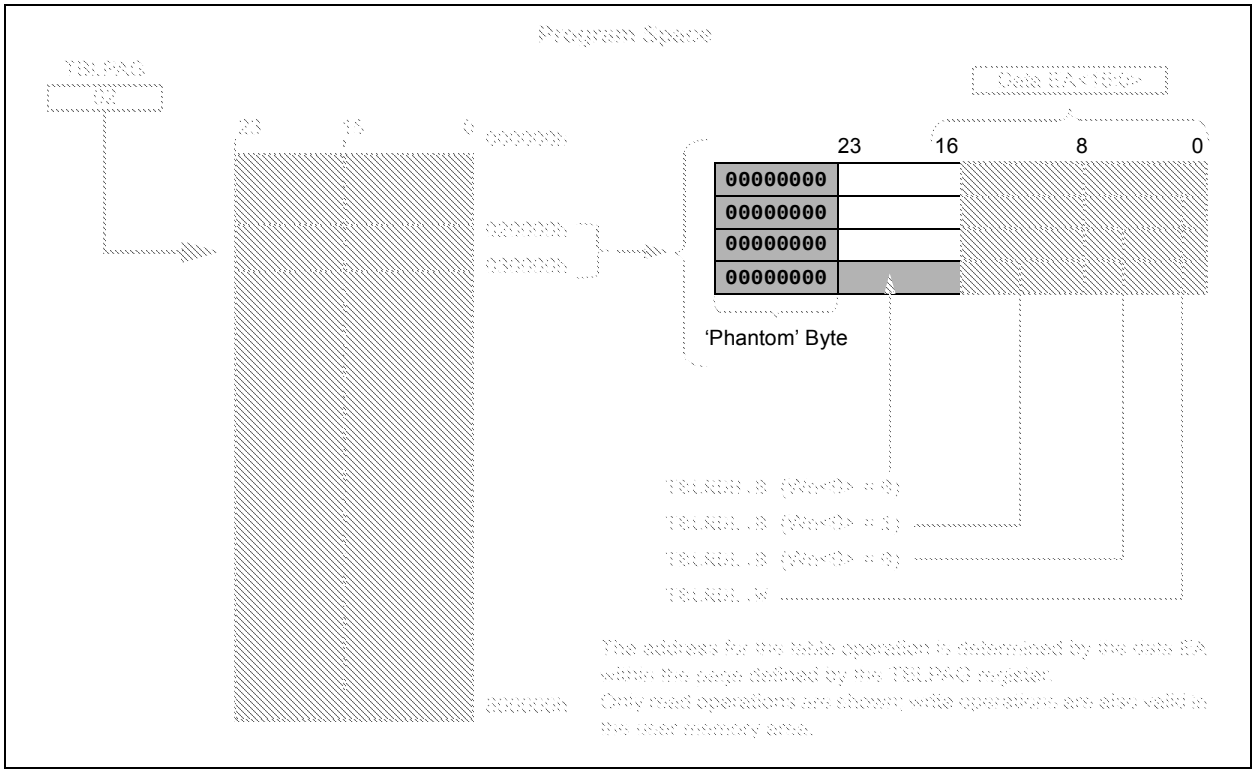
   In Byte mode, it maps the upper or lower byte of the program word to D<7:0> of the data address, as above. Note that the data will always be '0' when the upper 'phantom' byte is selected (Byte Select = 1).

In a similar fashion, two table instructions, TBLWTH and TBLWTL, are used to write individual bytes or words to a program space address. The details of their operation are described in **Section 6.0 "Flash Program Memory"**.

For all table operations, the area of program memory space to be accessed is determined by the Table Memory Page Address register (TBLPAG). TBLPAG covers the entire program memory space of the device, including user and configuration spaces. When TBLPAG<7> = 0, the table page is located in the user memory space. When TBLPAG<7> = 1, the page is located in configuration space.

| **Note:** | Only Table Read operations will execute in the configuration memory space where Device IDs are located. Table Write operations are not allowed. |
|---|---|

**FIGURE 4-9: ACCESSING PROGRAM MEMORY WITH TABLE INSTRUCTIONS**



**REGISTER 7-1: RCON: RESET CONTROL REGISTER (CONTINUED)**

bit 5 **SWDTEN:** Software Enable/Disable of WDT bit(4)
1 = WDT is enabled
0 = WDT is disabled

bit 4 **WDTO:** Watchdog Timer Time-out Flag bit(1)
1 = WDT time-out has occurred
0 = WDT time-out has not occurred

bit 3 **SLEEP:** Wake from Sleep Flag bit(1)
1 = Device has been in Sleep mode
0 = Device has not been in Sleep mode

bit 2 **IDLE:** Wake-up from Idle Flag bit(1)
1 = Device has been in Idle mode
0 = Device has not been in Idle mode

bit 1 **BOR:** Brown-out Reset Flag bit(1)
1 = A Brown-out Reset has occurred (also set after a Power-on Reset)
0 = A Brown-out Reset has not occurred

bit 0 **POR:** Power-on Reset Flag bit(1)
1 = A Power-on Reset has occurred
0 = A Power-on Reset has not occurred

**Note 1:** All of the Reset status bits may be set or cleared in software. Setting one of these bits in software does not cause a device Reset.

**2:** If the $\overline{\text{LPCFG}}$ Configuration bit is '1' (unprogrammed), the retention regulator is disabled and the RETEN bit has no effect.

**3:** Re-enabling the regulator after it enters Standby mode will add a delay, $T_{VREG}$, when waking up from Sleep. Applications that do not use the voltage regulator should set this bit to prevent this delay from occurring.

**4:** If the FWDTEN<1:0> Configuration bits are '11' (unprogrammed), the WDT is always enabled**,** regardless of the SWDTEN bit setting.

**REGISTER 8-5: IFS0: INTERRUPT FLAG STATUS REGISTER 0 (CONTINUED)**

bit 2 **OC1IF:** Output Compare Channel 1 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 1 **IC1IF:** Input Capture Channel 1 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 0 **INT0IF:** External Interrupt 0 Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

**REGISTER 11-28: RPOR0: PERIPHERAL PIN SELECT OUTPUT REGISTER 0**

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP1R5 | RP1R4 | RP1R3 | RP1R2 | RP1R1 | RP1R0 |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP0R5 | RP0R4 | RP0R3 | RP0R2 | RP0R1 | RP0R0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RP1R<5:0>:** RP1 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP1 (see Table 11-4 for peripheral function numbers).

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP0R<5:0>:** RP0 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP0 (see Table 11-4 for peripheral function numbers).

**REGISTER 11-29: RPOR1: PERIPHERAL PIN SELECT OUTPUT REGISTER 1**

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP3R5 | RP3R4 | RP3R3 | RP3R2 | RP3R1 | RP3R0 |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP2R5 | RP2R4 | RP2R3 | RP2R2 | RP2R1 | RP2R0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RP3R<5:0>:** RP3 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP3 (see Table 11-4 for peripheral function numbers).

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP2R<5:0>:** RP2 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP2 (see Table 11-4 for peripheral function numbers).

**REGISTER 13-1: TxCON: TIMER2 AND TIMER4 CONTROL REGISTER(1)**

| R/W-0 | U-0 | R/W-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| TON | — | TSIDL | — | — | — | TIECS1(2) | TIECS0(2) |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | TGATE | TCKPS1 | TCKPS0 | T32(3) | — | TCS(2) | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **TON:** Timerx On bit
When TxCON<3> = 1:
1 = Starts 32-bit Timerx/y
0 = Stops 32-bit Timerx/y
When TxCON<3> = 0:
1 = Starts 16-bit Timerx
0 = Stops 16-bit Timerx

bit 14 **Unimplemented:** Read as '0'

bit 13 **TSIDL:** Timerx Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-10 **Unimplemented:** Read as '0'

bit 9-8 **TIECS<1:0>:** Timerx Extended Clock Source Select bits (selected when TCS = 1)(2)
When TCS = 1:
11 = Generic Timer (TMRCK) external input
10 = LPRC Oscillator
01 = TxCK external clock input
00 = SOSC
When TCS = 0:
These bits are ignored; the timer is clocked from the internal system clock (FOSC/2).

bit 7 **Unimplemented:** Read as '0'

bit 6 **TGATE:** Timerx Gated Time Accumulation Enable bit
When TCS = 1:
This bit is ignored.
When TCS = 0:
1 = Gated time accumulation is enabled
0 = Gated time accumulation is disabled

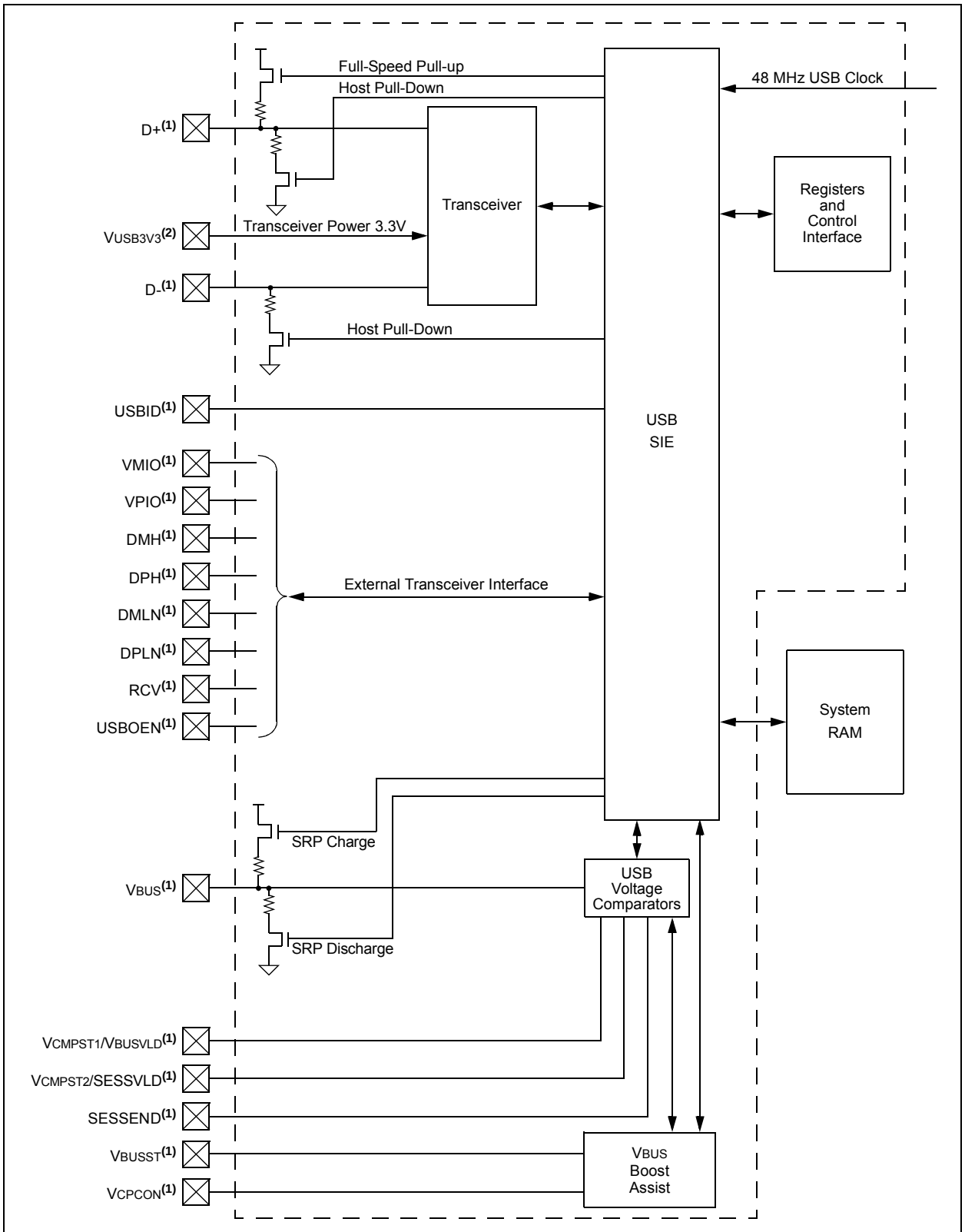
bit 5-4 **TCKPS<1:0>:** Timerx Input Clock Prescale Select bits
11 = 1:256
10 = 1:64
01 = 1:8
00 = 1:1

**Note 1:** Changing the value of TxCON while the timer is running (TON = 1) causes the timer prescale counter to reset and is not recommended.

**2:** If TCS = 1 and TIECS<1:0> = x1, the selected external timer input (TMRCK or TxCK) must be configured to an available RPn/RPIn pin. For more information, see **Section 11.4 "Peripheral Pin Select (PPS)"**.

**3:** In T4CON, the T45 bit is implemented instead of T32 to select 32-bit mode. In 32-bit mode, the T3CON or T5CON control bits do not affect 32-bit timer operation.

**FIGURE 19-1: USB OTG MODULE BLOCK DIAGRAM**




**Note 1:** Pins are multiplexed with digital I/O and other device features.

**2:** Connecting $V_{BUS3V3}$ to $V_{DD}$ is highly recommended, as floating this input can cause increased $I_{PD}$ currents. The pin should be tied to $V_{DD}$ when the USB functions are not used.

#### 19.5.3 SEND A FULL-SPEED BULK DATA TRANSFER TO A TARGET DEVICE

1. Follow the procedure described in **Section 19.5.1 "Enable Host Mode and Discover a Connected Device"** and **Section 19.5.2 "Complete a Control Transaction to a Connected Device"** to discover and configure a device.
2. To enable transmit and receive transfers with handshaking enabled, write '1Dh' to U1EP0. If the target device is a low-speed device, also set the LSPD (U1EP0<7>) bit. If you want the hardware to automatically retry indefinitely if the target device asserts a NAK on the transfer; clear the Retry Disable bit, RETRYDIS (U1EP0<6>).
3. Set up the BD for the current (even or odd) TX EP0 to transfer up to 64 bytes.
4. Set the USB device address of the target device in the USB Address register (U1ADDR<6:0>).
5. Write an OUT token to the desired endpoint to U1TOK. This triggers the module's transmit state machines to begin transmitting the token and the data.
6. Wait for the Token Complete Interrupt Flag, TRNIF. This indicates that the BD has been released back to the microprocessor and the transfer has completed. If the Retry Disable bit (RETRYDIS) is set, the handshake (ACK, NAK, STALL or ERROR ('0Fh')) is returned in the BD PID field. If a STALL interrupt occurs, the pending packet must be dequeued and the error condition in the target device cleared. If a detach interrupt occurs (SE0 for more than 2.5 µs), then the target has detached (U1IR<0> is set).
7. Once the Token Complete Interrupt Flag occurs (TRNIF is set), the BD can be examined and the next data packet queued by returning to Step 2.

| **Note:** | USB speed, transceiver and pull-ups should only be configured during the module setup phase. It is not recommended to change these settings while the module is enabled. |
|---|---|

## 19.6 OTG Operation

#### 19.6.1 SESSION REQUEST PROTOCOL (SRP)

An OTG A-device may decide to power down the VBUS supply when it is not using the USB link through the Session Request Protocol (SRP). Software may do this by configuring a GPIO pin to disable an external power transistor, or voltage regulator enable signal, which controls the VBUS supply. When the VBUS supply is powered down, the A-device is said to have ended a USB session.

An OTG A-device or embedded host may repower the VBUS supply at any time (initiate a new session). An OTG B-device may also request that the OTG A-device repower the VBUS supply (initiate a new session). This is accomplished via Session Request Protocol (SRP).

Prior to requesting a new session, the B-device must first check that the previous session has definitely ended. To do this, the B-device must check for two conditions:

1. VBUS supply is below the session valid voltage.
2. Both D+ and D- have been low for at least 2 ms.

The B-device will be notified of Condition 1 by the SESENDIF (U1OTGIR<2>) interrupt. Software will have to manually check for Condition 2.

| **Note:** | When the A-device powers down the VBUS supply, the B-device must disconnect its pull-up resistor from power. If the device is self-powered, it can do this by clearing DPPULUP (U1OTGCON<7>) and DMPULUP (U1OTGCON<6>). |
|---|---|

The B-device may aid in achieving Condition 1 by discharging the VBUS supply through a resistor. Software may do this by setting VBUSDIS (U1OTGCON<0>).

After these initial conditions are met, the B-device may begin requesting the new session. The B-device begins by pulsing the D+ data line. Software should do this by setting DPPULUP (U1OTGCON<7>). The data line should be held high for 5 to 10 ms.

The B-device then proceeds by pulsing the VBUS supply. Software should do this by setting PUVBUS (U1CNFG2<4>). When an A-device detects SRP signaling (either via the ATTACHIF (U1IR<6>) interrupt or via the SESVDIF (U1OTGIR<3>) interrupt), the A-device must restore the VBUS supply by properly configuring the general purpose I/O port pin controlling the external power source.

The B-device should not monitor the state of the VBUS supply while performing VBUS supply pulsing. When the B-device does detect that the VBUS supply has been restored (via the SESVDIF (U1OTGIR<3>) interrupt), the B-device must reconnect to the USB link by pulling up D+ or D- (via the DPPULUP or DMPULUP bit).

The A-device must complete the SRP by driving USB Reset signaling.

**REGISTER 19-11: U1SOF: USB OTG START-OF-TOKEN THRESHOLD REGISTER (HOST MODE ONLY)**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CNT<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7-0 **CNT<7:0>:** Start-of-Frame Size bits
Value represents 10 + (packet size of n bytes). For example:
0100 1010 = 64-byte packet
0010 1010 = 32-byte packet
0001 0010 = 8-byte packet

## 21.0 ENHANCED PARALLEL MASTER PORT (EPMP)

**Note:** This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"Enhanced Parallel Master Port (EPMP)"** (DS39730) which is available from the Microchip web site (www.microchip.com). The information in this data sheet supersedes the information in the FRM.

The Enhanced Parallel Master Port (EPMP) module provides a parallel, 4-bit (Master mode only), 8-bit (Master and Slave modes) or 16-bit (Master mode only) data bus interface to communicate with off-chip modules, such as memories, FIFOs, LCD controllers and other microcontrollers. This module can serve as either the master or the slave on the communication bus.

For EPMP Master modes, all external addresses are mapped into the internal Extended Data Space (EDS). This is done by allocating a region of the EDS for each Chip Select (CS) and then assigning each Chip Select to a particular external resource, such as a memory or external controller. This region should not be assigned to another device resource, such as RAM or SFRs. To perform a write or read on an external resource, the CPU simply performs a write or read within the address range assigned for the EPMP.

Key features of the EPMP module are:

- Extended Data Space (EDS) Interface Allows Direct Access from the CPU
- Up to 23 Programmable Address Lines
- Up to 2 Chip Select Lines
- Up to 2 Acknowledgment Lines (one per Chip Select)
- 4-Bit, 8-Bit or 16-Bit Wide Data Bus
- Programmable Strobe Options (per Chip Select):
  - Individual Read and Write Strobes; or
  - Read/$\overline{\text{Write}}$ Strobe with Enable Strobe
- Programmable Address/Data Multiplexing
- Programmable Address Wait States
- Programmable Data Wait States (per Chip Select)
- Programmable Polarity on Control Signals (per Chip Select)
- Legacy Parallel Slave Port (PSP) Support
- Enhanced Parallel Slave Support:
  - Address Support
  - 4-Byte Deep Auto-Incrementing Buffer

### 21.1 Specific Package Variations

While all PIC24FJ128GC010 family devices implement the EPMP, I/O pin constraints place some limits on 16-Bit Master mode operations in some package types. This is reflected in the number of dedicated Chip Select pins implemented and the number of dedicated address lines that are available. The differences are summarized in Table 21-1. All available EPMP pin functions are summarized in Table 21-2.

For 64-pin devices, the dedicated Chip Select pins (PMCS1 and PMCS2) are not implemented. In addition, only 16 address lines (PMA<15:0>) are available. If required, PMA14 and PMA15 can be remapped to function as PMCS1 and PMCS2, respectively.

The memory space addressable by the device depends on the number of address lines available, as well as the number of Chip Select signals required for the application. Devices with lower pin counts are more affected by Chip Select requirements, as these take away address lines. Table 21-1 shows the maximum addressable range for each pin count.

**TABLE 21-1: EPMP FEATURE DIFFERENCES BY DEVICE PIN COUNT**

| Device | Dedicated Chip Select | | Address Lines | Address Range (bytes) | | |
|---|---|---|---|---|---|---|
| | CS1 | CS2 | | No CS | 1 CS | 2 CS |
| PIC24FJXXXGC006 (64-pin) | — | — | 16 | 64K | 32K | 16K |
| PIC24FJXXXGC010 (100/121-pin) | X | X | 23 | 16M | | |

**REGISTER 21-4: PMCON4: EPMP CONTROL REGISTER 4**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PTEN15 | PTEN14 | PTEN<13:8> | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PTEN<7:3> | | | | | PTEN<2:0> | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15 **PTEN15:** PMA15 Port Enable bit
1 = PMA15 functions as either Address Line 15 or Chip Select 2
0 = PMA15 functions as port I/O

bit 14 **PTEN14:** PMA14 Port Enable bit
1 = PMA14 functions as either Address Line 14 or Chip Select 1
0 = PMA14 functions as port I/O

bit 13-3 **PTEN<13:3>:** EPMP Address Port Enable bits
1 = PMA<13:3> function as EPMP address lines
0 = PMA<13:3> function as port I/Os

bit 2-0 **PTEN<2:0>:** PMALU/PMALH/PMALL Strobe Enable bits
1 = PMA<2:0> function as either address lines or address latch strobes
0 = PMA<2:0> function as port I/Os

### 24.1.3 DATA SHIFT DIRECTION

The LENDIAN bit (CRCCON1<3>) is used to control the shift direction. By default, the CRC will shift data through the engine, MSb first. Setting LENDIAN (= 1) causes the CRC to shift data, LSb first. This setting allows better integration with various communication schemes and removes the overhead of reversing the bit order in software. Note that this only changes the direction the data is shifted into the engine. The result of the CRC calculation will still be a normal CRC result, not a reverse CRC result.

### 24.1.4 INTERRUPT OPERATION

The module generates an interrupt that is configurable by the user for either of two conditions.

If CRCISEL is '0', an interrupt is generated when the VWORD<4:0> bits make a transition from a value of '1' to '0'. If CRCISEL is '1', an interrupt will be generated after the CRC operation finishes and the module sets the CRCGO bit to '0'. Manually setting CRCGO to '0' will not generate an interrupt. Note that when an interrupt occurs, the CRC calculation would not yet be complete. The module will still need (PLENx + 1)/2 clock cycles after the interrupt is generated until the CRC calculation is finished.

### 24.1.5 TYPICAL OPERATION

To use the module for a typical CRC calculation:

1. Set the CRCEN bit to enable the module.
2. Configure the module for desired operation:
   a) Program the desired polynomial using the CRCXORL and CRCXORH registers, and the PLEN<4:0> bits.
   b) Configure the data width and shift direction using the DWIDTHx and LENDIAN bits.
   c) Select the desired Interrupt mode using the CRCISEL bit.
3. Preload the FIFO by writing to the CRCDATL and CRCDATH registers until the CRCFUL bit is set or no data is left.
4. Clear old results by writing 00h to CRCWDATL and CRCWDATH. The CRCWDAT registers can also be left unchanged to resume a previously halted calculation.
5. Set the CRCGO bit to start calculation.
6. Write remaining data into the FIFO as space becomes available.
7. When the calculation completes, CRCGO is automatically cleared. An interrupt will be generated if CRCISEL = 1.
8. Read CRCWDATL and CRCWDATH for the result of the calculation.

There are eight registers used to control programmable CRC operation:

- CRCCON1
- CRCCON2
- CRCXORL
- CRCXORH
- CRCDATL
- CRCDATH
- CRCWDATL
- CRCWDATH

The CRCCON1 and CRCCON2 registers (Register 24-1 and Register 24-2) control the operation of the module and configure the various settings.

The CRCXORL/H registers (Register 24-3 and Register 24-4) select the polynomial terms to be used in the CRC equation. The CRCDATL/H and CRCWDATL/H registers are each register pairs that serve as buffers for the double-word input data, and CRC processed output, respectively.

**REGISTER 26-1: ADCON1: A/D CONTROL REGISTER 1**

| R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| ADON | — | ADSIDL | ADSLP | FORM3 | FORM2 | FORM1 | FORM0 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PUMPEN | ADCAL(2) | — | — | — | — | — | PWRLVL |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **ADON:** A/D Module Enable bit
1 = Module is enabled
0 = Module is disabled (registers are still readable and writable)

bit 14 **Unimplemented:** Read as '0'

bit 13 **ADSIDL:** A/D Stop in Idle Control bit
1 = Halts when CPU is in Idle mode
0 = Continues to operate in CPU Idle mode

bit 12 **ADSLP:** A/D Suspend in Sleep Control bit
1 = Continues operation in Sleep mode
0 = Ignores triggers and clocks when CPU is in Sleep mode

bit 11-8 **FORM<3:0>:** Data Output Format bits
1xxx = Unimplemented, do not use
0111 = Signed Fractional (sddd dddd dddd 0000)
0110 = Fractional (dddd dddd dddd 0000)
0101 = Signed Integer (ssss sddd dddd dddd)
0100 = Integer (0000 dddd dddd dddd )
0011 = Signed Fractional (sddd dddd dddd 0000)
0010 = Fractional (dddd dddd dddd 0000)
0001 = Signed Integer (ssss sddd dddd dddd)
0000 = Integer, Raw Data (0000 dddd dddd dddd)

bit 7 **PUMPEN:** Analog Channel Switch Charge Pump Enable bit
1 = Charge pump for switches is enabled, reducing switch impedance(1)
0 = Charge pump for switches is disabled

bit 6 **ADCAL:** A/D Internal Analog Calibration bit(2)
1 = Initiates internal analog calibration
0 = No operation

bit 5-1 **Unimplemented:** Read as '0'

bit 0 **PWRLVL:** Power Level Select bit
1 = Full-Power mode; A/D clock rates from 1 MHz to 10 MHz are allowed
0 = Low-Power mode; A/D clock rates from 1 MHz to 2.5 MHz are allowed

**Note 1:** Use of the channel switch charge pump is recommended when $AV_{DD}$ < 2.5V.
**2:** When set, ADCAL remains set for at least one $T_{AD}$ and is then automatically cleared by hardware. Manually clearing the bit does not necessarily cancel the calibration routine. Calibration is complete when ADSTATH<1> = 1.

**REGISTER 26-19: ADLnMSEL1: A/D SAMPLE LIST n MULTICHANNEL SELECT REGISTER 1 (n = 0 to 3)**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| MSEL<31:24> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| MSEL<23:16> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **MSEL<31:16>:** A/D Channel Select bits
1 = Corresponding channel participates in multichannel operations for Sample List n
0 = Channel does not participate in multichannel operations

**REGISTER 26-20: ADLnMSEL0: A/D SAMPLE LIST n MULTICHANNEL SELECT REGISTER 0 (n = 0 to 3)**

| R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| MSEL15 | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **MSEL15:** A/D Channel Select bit
1 = Corresponding channel participates in multichannel operations for Sample List n
0 = Channel does not participate in multichannel operations

bit 14-0 **Unimplemented:** Read as '0'

**REGISTER 27-3: SD1CON3: S/D CONTROL REGISTER 3**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| SDDIV2(1) | SDDIV1(1) | SDDIV0(1) | SDOSR2 | SDOSR1 | SDOSR0 | SDCS1 | SDCS0 |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | SDCH2 | SDCH1 | SDCH0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-13 **SDDIV<2:0>:** S/D Input Clock Divider/Postscaler Ratio bits(1)
- 111 = Reserved
- 110 = 64
- 101 = 32
- 100 = 16
- 011 = 8
- 010 = 4
- 001 = 2
- 000 = 1 (No divider, clock selected by SDCS<1:0> is provided directly to A/D.)

bit 12-10 **SDOSR<2:0>:** S/D Oversampling Ratio (OSR) Selection bits
- 111 = Reserved
- 110 = 16 (fastest result, lowest quality)
- 101 = 32
- 100 = 64
- 011 = 128
- 010 = 256
- 001 = 512
- 000 = 1024 (slowest result, best quality)

bit 9-8 **SDCS<1:0>:** S/D A/D Module Clock Source Select bits
- 11 = Reserved
- 10 = Primary Oscillator (OSCI/CLKI)
- 01 = FRC (8 MHz)(2)
- 00 = System clock (FOSC/2)

bit 7-3 **Unimplemented:** Read as '0'

bit 2-0 **SDCH<2:0>:** S/D Analog Channel Input Select bits (positive input/negative input)
- 1xx = Reserved
- 011 = Measures the reference selected by SDREFP/SDREFN (used for gain error measurements)
- 010 = CH1SE/SVSS (single-ended measurement of CH1SE)
- 001 = CH1+/CH1- (Differential Channel 1)
- 000 = CH0+/CH0- (Differential Channel 0)

**Note 1:** To avoid overclocking or underclocking the module, set SDDIV<2:0> to obtain an A/D clock frequency (input frequency selected by SDCS<1:0> source, divided by selected SDDIVx ratio) at or between 1 MHz and 4 MHz.

**2:** Eight MHz FRC output is used directly, prior to the FRCDIV postscaler.

**REGISTER 34-1: CW1: FLASH CONFIGURATION WORD 1 (CONTINUED)**

bit 4 **FWPSA:** WDT Prescaler Ratio Select bit

1 = Prescaler ratio of 1:128
0 = Prescaler ratio of 1:32

bit 3-0 **WDTPS<3:0>:** Watchdog Timer Postscaler Select bits

1111 = 1:32,768
1110 = 1:16,384
1101 = 1:8,192
1100 = 1:4,096
1011 = 1:2,048
1010 = 1:1,024
1001 = 1:512
1000 = 1:256
0111 = 1:128
0110 = 1:64
0101 = 1:32
0100 = 1:16
0011 = 1:8
0010 = 1:4
0001 = 1:2
0000 = 1:1

**TABLE 36-1: SYMBOLS USED IN OPCODE DESCRIPTIONS**

| Field | Description |
|---|---|
| #text | Means literal defined by "text" |
| (text) | Means "content of text" |
| [text] | Means "the location addressed by text" |
| { } | Optional field or operation |
| <n:m> | Register bit field |
| .b | Byte mode selection |
| .d | Double-Word mode selection |
| .S | Shadow register select |
| .w | Word mode selection (default) |
| bit4 | 4-bit Bit Selection field (used in word addressed instructions) ∈ {0...15} |
| C, DC, N, OV, Z | MCU Status bits: Carry, Digit Carry, Negative, Overflow, Sticky Zero |
| Expr | Absolute address, label or expression (resolved by the linker) |
| f | File register address ∈ {0000h...1FFFh} |
| lit1 | 1-bit unsigned literal ∈ {0,1} |
| lit4 | 4-bit unsigned literal ∈ {0...15} |
| lit5 | 5-bit unsigned literal ∈ {0...31} |
| lit8 | 8-bit unsigned literal ∈ {0...255} |
| lit10 | 10-bit unsigned literal ∈ {0...255} for Byte mode, {0:1023} for Word mode |
| lit14 | 14-bit unsigned literal ∈ {0...16383} |
| lit16 | 16-bit unsigned literal ∈ {0...65535} |
| lit23 | 23-bit unsigned literal ∈ {0...8388607}; LSB must be '0' |
| None | Field does not require an entry, may be blank |
| PC | Program Counter |
| Slit10 | 10-bit signed literal ∈ {-512...511} |
| Slit16 | 16-bit signed literal ∈ {-32768...32767} |
| Slit6 | 6-bit signed literal ∈ {-16...16} |
| Wb | Base W register ∈ {W0..W15} |
| Wd | Destination W register ∈ { Wd, [Wd], [Wd++], [Wd--], [++Wd], [--Wd] } |
| Wdo | Destination W register ∈<br>{ Wnd, [Wnd], [Wnd++], [Wnd--], [++Wnd], [--Wnd], [Wnd+Wb] } |
| Wm,Wn | Dividend, Divisor Working register pair (direct addressing) |
| Wn | One of 16 Working registers ∈ {W0..W15} |
| Wnd | One of 16 destination Working registers ∈ {W0..W15} |
| Wns | One of 16 source Working registers ∈ {W0..W15} |
| WREG | W0 (Working register used in file register instructions) |
| Ws | Source W register ∈ { Ws, [Ws], [Ws++], [Ws--], [++Ws], [--Ws] } |
| Wso | Source W register ∈ { Wns, [Wns], [Wns++], [Wns--], [++Wns], [--Wns], [Wns+Wb] } |

**TABLE 37-15: USB ON-THE-GO MODULE SPECIFICATIONS**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ** | **Max** | **Units** | **Conditions** |
| **Operating Voltage** | | | | | | | |
| DUS01 | VUSB3V3 | USB Supply Voltage | Greater of: 3.0 or (VDD – 0.3V) | 3.3 | 3.6 | V | USB module enabled |
| | | | (VDD – 0.3V)(1) | — | 3.6 | V | USB disabled, RG2/RG3 are unused and externally pulled low or left in a high-impedance state |
| | | | (VDD – 0.3V) | VDD | 3.6 | V | USB disabled, RG2/RG3 are used as general purpose I/O |

**Note 1:** The VUSB pin may also be left in a high-impedance state under these conditions. However, if the voltage floats below (VDD – 0.3V), this may result in higher IPD currents than specified. The preferred method is to tie the VUSB pin to VDD, even if the USB module is not used.

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