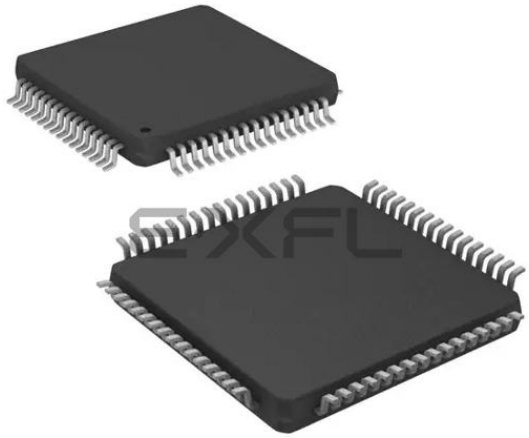
# Microchip Technology - PIC24FJ128GC006-I/PT Datasheet



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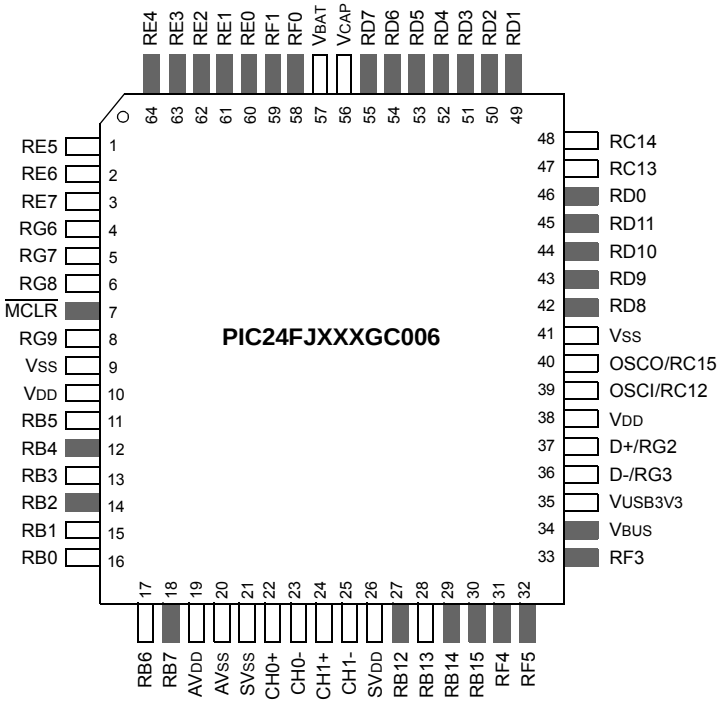
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 16-Bit |
| Speed | 32MHz |
| Connectivity | I²C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, LCD, LVD, POR, PWM, WDT |
| Number of I/O | 53 |
| Program Memory Size | 128KB (43K x 24) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 3.6V |
| Data Converters | A/D 29x12b, 2x16b; D/A 2x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-TQFP |
| Supplier Device Package | 64-TQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic24fj128gc006-i-pt |

## Pin Diagrams

**64-Pin TQFP (10 mm x 10 mm)**
**64-Pin QFN (9 mm x 9 mm)(1)**




**Legend:** **Shaded pins** indicate pins tolerant to up to +5.5 VDC. See Table 1 for a complete description of pin functions.
**Note 1:** It is recommended to connect the metal pad on the bottom of the 64-pin QFN package to VSS.

**TABLE 1-1: DEVICE FEATURES FOR THE PIC24FJ128GC010 FAMILY: 64-PIN DEVICES**

| Features | PIC24FJ64GC006 | PIC24FJ128GC006 |
|---|---|---|
| Operating Frequency | DC – 32 MHz | |
| Program Memory (bytes) | 64K | 128K |
| Program Memory (instructions) | 22,016 | 44,032 |
| Data Memory (bytes) | 8K | |
| Interrupt Sources (soft vectors/ NMI traps) | 65 (61/4) | |
| I/O Ports | Ports B, C, D, E, F, G | |
| Total I/O Pins | 53 | |
| Remappable Pins | 30 (29 I/Os, 1 input only) | |
| Timers: Total Number (16-bit) | 5(1) | |
| 32-Bit (from paired 16-bit timers) | 2 | |
| Input Capture w/Timer Channels | 9(1) | |
| Output Compare/PWM Channels | 9(1) | |
| Input Change Notification Interrupt | 52 | |
| Serial Communications: UART | 4(1) | |
| SPI (3-wire/4-wire) | 2(1) | |
| $I^2C$ | 2 | |
| Digital Signal Modulator | Yes | |
| Parallel Communications (EPMP/PSP) | Yes | |
| JTAG Boundary Scan | Yes | |
| 12-Bit Pipeline Analog-to-Digital Converter (A/D) (input channels) | 29 | |
| Sigma-Delta Analog-to-Digital Converter (A/D) (differential channels) | 2 | |
| Digital-to-Analog Converter (DAC) | 2 | |
| Operational Amplifiers | 2 | |
| Analog Comparators | 3 | |
| CTMU Interface | Yes | |
| LCD Controller (available pixels) | 196 (28 SEG x 7 COM) | |
| Resets (and delays) | Core POR, VDD POR, VBAT POR, BOR, RESET Instruction, $\overline{MCLR}$, WDT, Illegal Opcode, REPEAT Instruction, Hardware Traps, Configuration Word Mismatch (OST, PLL Lock) | |
| Instruction Set | 76 Base Instructions, Multiple Addressing Mode Variations | |
| Packages | 64-Pin TQFP and QFN | |

**Note 1:** Peripherals are accessible through remappable pins.

**TABLE 1-2: DEVICE FEATURES FOR THE PIC24FJ128GC010 FAMILY: 100/121-PIN DEVICES**

| Features | PIC24FJ64GC010 | PIC24FJ128GC010 |
|---|---|---|
| Operating Frequency | DC – 32 MHz | |
| Program Memory (bytes) | 64K | 128K |
| Program Memory (instructions) | 22,016 | 44,032 |
| Data Memory (bytes) | 8K | |
| Interrupt Sources (soft vectors/ NMI traps) | 66 (62/4) | |
| I/O Ports | Ports A, B, C, D, E, F, G | |
| Total I/O Pins | 85 | |
| Remappable Pins | 44 (32 I/Os, 12 input only) | |
| Timers: Total Number (16-bit) | 5(1) | |
| 32-Bit (from paired 16-bit timers) | 2 | |
| Input Capture w/Timer Channels | 9(1) | |
| Output Compare/PWM Channels | 9(1) | |
| Input Change Notification Interrupt | 82 | |
| Serial Communications: UART | 4(1) | |
| SPI (3-wire/4-wire) | 2(1) | |
| $I^2C$ | 2 | |
| Digital Signal Modulator | Yes | |
| Parallel Communications (EPMP/PSP) | Yes | |
| JTAG Boundary Scan | Yes | |
| 12-Bit Pipeline Analog-to-Digital Converter (A/D) (input channels) | 50 | |
| Sigma-Delta Analog-to-Digital Converter (A/D) (differential channels) | 2 | |
| Digital-to-Analog Converter (DAC) | 2 | |
| Operational Amplifiers | 2 | |
| Analog Comparators | 3 | |
| CTMU Interface | Yes | |
| LCD Controller (available pixels) | 472 (59 SEG x 8 COM) | |
| Resets (and delays) | Core POR, VDD POR, VBAT POR, BOR, RESET Instruction, MCLR, WDT, Illegal Opcode, REPEAT Instruction, Hardware Traps, Configuration Word Mismatch (OST, PLL Lock) | |
| Instruction Set | 76 Base Instructions, Multiple Addressing Mode Variations | |
| Packages | 100-Pin TQFP and 121-Pin BGA | |

**Note 1:** Peripherals are accessible through remappable pins.

**TABLE 1-3: PIC24FJ128GC010 FAMILY PINOUT DESCRIPTION (CONTINUED)**

| Pin Function | Pin Number/Grid Locator | | | I/O | Input Buffer | Description |
|---|---|---|---|---|---|---|
| | 64-Pin TQFP/QFN | 100-Pin TQFP | 121-Pin BGA | | | |
| SOSCI | 47 | 73 | C10 | I | ANA | Secondary Oscillator Input. |
| SOSCO | 48 | 74 | B11 | O | ANA | Secondary Oscillator Output. |
| SVDD | 26 | 37 | J5 | P | — | Positive Supply for Sigma-Delta A/D Converter. |
| SVREF+ | 24 | 35 | K5 | I | ANA | Sigma-Delta A/D Converter Voltage Reference (high). |
| SVREF- | 25 | 36 | L5 | I | ANA | Sigma-Delta A/D Converter Voltage Reference (low). |
| SVss | 21 | 32 | K4 | P | — | Ground Reference for Sigma-Delta A/D Converter. |
| T1CK | 27 | 41 | J7 | I | ST | External Timer1 Clock Input. |
| T2CK | 30 | 44 | L8 | I | ST | External Timer2 Clock Input. |
| T3CK | 31 | 49 | L10 | I | ST | External Timer3 Clock Input. |
| T4CK | 14 | 23 | J2 | I | ST | External Timer4 Clock Input. |
| T5CK | 4 | 10 | E3 | I | ST | External Timer5 Clock Input. |
| TCK | 27 | 38 | J6 | I | ST | JTAG Test Clock/Programming Clock Input. |
| TDI | 28 | 60 | G11 | I | ST | JTAG Test Data/Programming Data Input. |
| TDO | 29 | 61 | G9 | O | — | JTAG Test Data Output. |
| TMS | 45 | 17 | G3 | I | ST | JTAG Test Mode Select Input. |
| USBID | 33 | 51 | K10 | I | ST | USB OTG ID (OTG mode only). |
| USBOE | 12 | 21 | H2 | O | — | USB Output Enable Control (for external transceiver). |
| VBAT | 57 | 86 | A7 | P | — | Backup Battery (B+) Input. |
| VBUS | 34 | 54 | H8 | P | — | USB VBUS Connection (5V nominal). |
| VCAP | 56 | 85 | B7 | P | — | External Filter Capacitor Connection. |
| VCMPST1 | 58 | 87 | B6 | I | ST | USB VBUS External Comparator Input 1. |
| VCMPST2 | 59 | 88 | A6 | I | ST | USB VBUS External Comparator Input 2. |
| VCMPST3 | 46 | 72 | D9 | I | ST | USB VBUS External Comparator Input 3. |
| VDD | 10, 38 | 2, 16, 46,62 | C2,G5, K8, F8 | P | — | Positive Supply for Peripheral Digital Logic and I/O Pins. |
| VLCAP1 | 5 | 11 | F4 | P | ANA | LCD Drive Charge Pump Capacitor Pins. |
| VLCAP2 | 6 | 12 | F2 | P | ANA | |
| VMIO | 14 | 23 | J2 | I/O | ST | USB Differential Minus Input/Output (external transceiver). |
| VPIO | 13 | 22 | J1 | I/O | ST | USB Differential Plus Input/Output (external transceiver). |
| VSS | 9, 41 | 15, 45, 65, 75 | F5, G7, F10, B10 | P | — | Ground Reference for Logic and I/O Pins. |
| VUSB3V3 | 35 | 55 | H9 | P | — | USB Transceiver Power Input Voltage (3.3V nominal). |

**Legend:** TTL = TTL input buffer ST = Schmitt Trigger input buffer
ANA = Analog level input/output $I^2C$ = $I^2C$/SMBus input buffer

**TABLE 4-32: COMPARATORS REGISTER MAP**

| File Name | Addr | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CMSTAT | 0630 | CMIDL | — | — | — | — | C3EVT | C2EVT | C1EVT | — | — | — | — | — | C3OUT | C2OUT | C1OUT | 0000 |
| CVRCON | 0632 | — | — | — | — | — | CVREFP | CVREFM1 | CVREFM0 | CVREN | CVROE | CVRSS | CVR4 | CVR3 | CVR2 | CVR1 | CVR0 | 0000 |
| CM1CON | 0634 | CON | COE | CPOL | — | — | — | CEVT | COUT | EVPOL1 | EVPOL0 | — | CREF | — | — | CCH1 | CCH0 | 0000 |
| CM2CON | 0636 | CON | COE | CPOL | — | — | — | CEVT | COUT | EVPOL1 | EVPOL0 | — | CREF | — | — | CCH1 | CCH0 | 0000 |
| CM3CON | 0638 | CON | COE | CPOL | — | — | — | CEVT | COUT | EVPOL1 | EVPOL0 | — | CREF | — | — | CCH1 | CCH0 | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-33: CRC REGISTER MAP**

| File Name | Addr | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CRCCON1 | 0640 | CRCEN | — | CSIDL | VWORD4 | VWORD3 | VWORD2 | VWORD1 | VWORD0 | CRCFUL | CRCMPT | CRCISEL | CRCGO | LENDIAN | — | — | — | 0040 |
| CRCCON2 | 0642 | — | — | — | DWIDTH4 | DWIDTH3 | DWIDTH2 | DWIDTH1 | DWIDTH0 | — | — | — | PLEN4 | PLEN3 | PLEN2 | PLEN1 | PLEN0 | 0000 |
| CRCXORL | 0644 | X<15:1> | | | | | | | | | | | | | | | — | 0000 |
| CRCXORH | 0646 | X<31:16> | | | | | | | | | | | | | | | | 0000 |
| CRCDATL | 0648 | CRC Data Input Register Low | | | | | | | | | | | | | | | | 0000 |
| CRCDATH | 064A | CRC Data Input Register High | | | | | | | | | | | | | | | | 0000 |
| CRCWDATL | 064C | CRC Result Register Low | | | | | | | | | | | | | | | | 0000 |
| CRCWDATH | 064E | CRC Result Register High | | | | | | | | | | | | | | | | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-34: BAND GAP BUFFER INTERFACE REGISTER MAP**

| File Name | Addr | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| BUFCON0 | 0670 | BUFEN | — | BUFSIDL | BUFSLP | — | — | — | — | — | BUFSTBY | — | — | — | — | BUFREF1 | BUFREF0 | 0000 |
| BUFCON1 | 0672 | BUFEN | — | BUFSIDL | BUFSLP | — | — | — | — | BUFOE | BUFSTBY | — | — | — | — | BUFREF1 | BUFREF0 | 0000 |
| BUFCON2 | 0674 | BUFEN | — | BUFSIDL | BUFSLP | — | — | — | — | BUFOE | BUFSTBY | — | — | — | — | BUFREF1 | BUFREF0 | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**REGISTER 8-39: IPC20: INTERRUPT PRIORITY CONTROL REGISTER 20**

| U-0 | R/W-1 | R/W-0 | R/W-0 | U-0 | R/W-1 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | U3TXIP2 | U3TXIP1 | U3TXIP0 | — | U3RXIP2 | U3RXIP1 | U3RXIP0 |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-1 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | U3ERIP2 | U3ERIP1 | U3ERIP0 | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **U3TXIP<2:0>:** UART3 Transmitter Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as ‘0’

bit 10-8 **U3RXIP<2:0>:** UART3 Receiver Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **U3ERIP<2:0>:** UART3 Error Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3-0 **Unimplemented:** Read as ‘0’

### 11.4.6 PERIPHERAL PIN SELECT REGISTERS

The PIC24FJ128GC010 family of devices implements a total of 35 registers for remappable peripheral configuration:

- Input Remappable Peripheral Registers (19)
- Output Remappable Peripheral Registers (16)

**Note:** Input and output register values can only be changed if IOLOCK (OSCCON<6>) = 0. See **Section 11.4.4.1 "Control Register Lock"** for a specific command sequence.

**REGISTER 11-9: RPINR0: PERIPHERAL PIN SELECT INPUT REGISTER 0**

| U-0 | U-0 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| — | — | INT1R5 | INT1R4 | INT1R3 | INT1R2 | INT1R1 | INT1R0 |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **INT1R<5:0>:** Assign External Interrupt 1 (INT1) to Corresponding RPn or RPIn Pin bits

bit 7-0 **Unimplemented:** Read as '0'

**REGISTER 11-10: RPINR1: PERIPHERAL PIN SELECT INPUT REGISTER 1**

| U-0 | U-0 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| — | — | INT3R5 | INT3R4 | INT3R3 | INT3R2 | INT3R1 | INT3R0 |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| — | — | INT2R5 | INT2R4 | INT2R3 | INT2R2 | INT2R1 | INT2R0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **INT3R<5:0>:** Assign External Interrupt 3 (INT3) to Corresponding RPn or RPIn Pin bits

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **INT2R<5:0>:** Assign External Interrupt 2 (INT2) to Corresponding RPn or RPIn Pin bits

**REGISTER 13-1: TxCON: TIMER2 AND TIMER4 CONTROL REGISTER(1)**

| R/W-0 | U-0 | R/W-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| TON | — | TSIDL | — | — | — | TIECS1(2) | TIECS0(2) |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | TGATE | TCKPS1 | TCKPS0 | T32(3) | — | TCS(2) | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **TON:** Timerx On bit
When TxCON<3> = 1:
1 = Starts 32-bit Timerx/y
0 = Stops 32-bit Timerx/y
When TxCON<3> = 0:
1 = Starts 16-bit Timerx
0 = Stops 16-bit Timerx

bit 14 **Unimplemented:** Read as '0'

bit 13 **TSIDL:** Timerx Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-10 **Unimplemented:** Read as '0'

bit 9-8 **TIECS<1:0>:** Timerx Extended Clock Source Select bits (selected when TCS = 1)(2)
When TCS = 1:
11 = Generic Timer (TMRCK) external input
10 = LPRC Oscillator
01 = TxCK external clock input
00 = SOSC
When TCS = 0:
These bits are ignored; the timer is clocked from the internal system clock (FOSC/2).

bit 7 **Unimplemented:** Read as '0'

bit 6 **TGATE:** Timerx Gated Time Accumulation Enable bit
When TCS = 1:
This bit is ignored.
When TCS = 0:
1 = Gated time accumulation is enabled
0 = Gated time accumulation is disabled

bit 5-4 **TCKPS<1:0>:** Timerx Input Clock Prescale Select bits
11 = 1:256
10 = 1:64
01 = 1:8
00 = 1:1

**Note 1:** Changing the value of TxCON while the timer is running (TON = 1) causes the timer prescale counter to reset and is not recommended.

**2:** If TCS = 1 and TIECS<1:0> = x1, the selected external timer input (TMRCK or TxCK) must be configured to an available RPn/RPIn pin. For more information, see **Section 11.4 "Peripheral Pin Select (PPS)"**.

**3:** In T4CON, the T45 bit is implemented instead of T32 to select 32-bit mode. In 32-bit mode, the T3CON or T5CON control bits do not affect 32-bit timer operation.

**REGISTER 13-1: TxCON: TIMER2 AND TIMER4 CONTROL REGISTER(1) (CONTINUED)**

bit 3 **T32:** 32-Bit Timer Mode Select bit(3)
1 = Timerx and Timery form a single 32-bit timer
0 = Timerx and Timery act as two 16-bit timers
In 32-bit mode, T3CON control bits do not affect 32-bit timer operation.

bit 2 **Unimplemented:** Read as '0'

bit 1 **TCS:** Timerx Clock Source Select bit(2)
1 = Timer source is selected by TIECS<1:0>
0 = Internal clock (FOSC/2)

bit 0 **Unimplemented:** Read as '0'

**Note 1:** Changing the value of TxCON while the timer is running (TON = 1) causes the timer prescale counter to reset and is not recommended.

**2:** If TCS = 1 and TIECS<1:0> = x1, the selected external timer input (TMRCK or TxCK) must be configured to an available RPn/RPIn pin. For more information, see **Section 11.4 "Peripheral Pin Select (PPS)"**.

**3:** In T4CON, the T45 bit is implemented instead of T32 to select 32-bit mode. In 32-bit mode, the T3CON or T5CON control bits do not affect 32-bit timer operation.

For 32-bit cascaded operation, these steps are also necessary:

1. Set the OC32 bits for both registers (OCyCON2<8>) and (OCxCON2<8>). Enable the even numbered module first to ensure the modules will start functioning in unison.
2. Clear the OCTRIG bit of the even module (OCyCON2<7>), so the module will run in Synchronous mode.
3. Configure the desired output and Fault settings for OCy.
4. Force the output pin for OCx to the output state by clearing the OCTRIS bit.
5. If Trigger mode operation is required, configure the trigger options in OCx by using the OCTRIG (OCxCON2<7>), TRIGMODE (OCxCON1<3>) and SYNCSELx (OCxCON2<4:0>) bits.
6. Configure the desired Compare or PWM mode of operation (OCM<2:0>) for OCy first, then for OCx.

Depending on the output mode selected, the module holds the OCx pin in its default state and forces a transition to the opposite state when OCxR matches the timer. In Double Compare modes, OCx is forced back to its default state when a match with OCxRS occurs. The OCxIF interrupt flag is set after an OCxR match in Single Compare modes and after each OCxRS match in Double Compare modes.

Single-shot pulse events only occur once, but may be repeated by simply rewriting the value of the OCxCON1 register. Continuous pulse events continue indefinitely until terminated.

## 15.3 Pulse-Width Modulation (PWM) Mode

In PWM mode, the output compare module can be configured for edge-aligned or center-aligned pulse waveform generation. All PWM operations are double-buffered (buffer registers are internal to the module and are not mapped into SFR space).

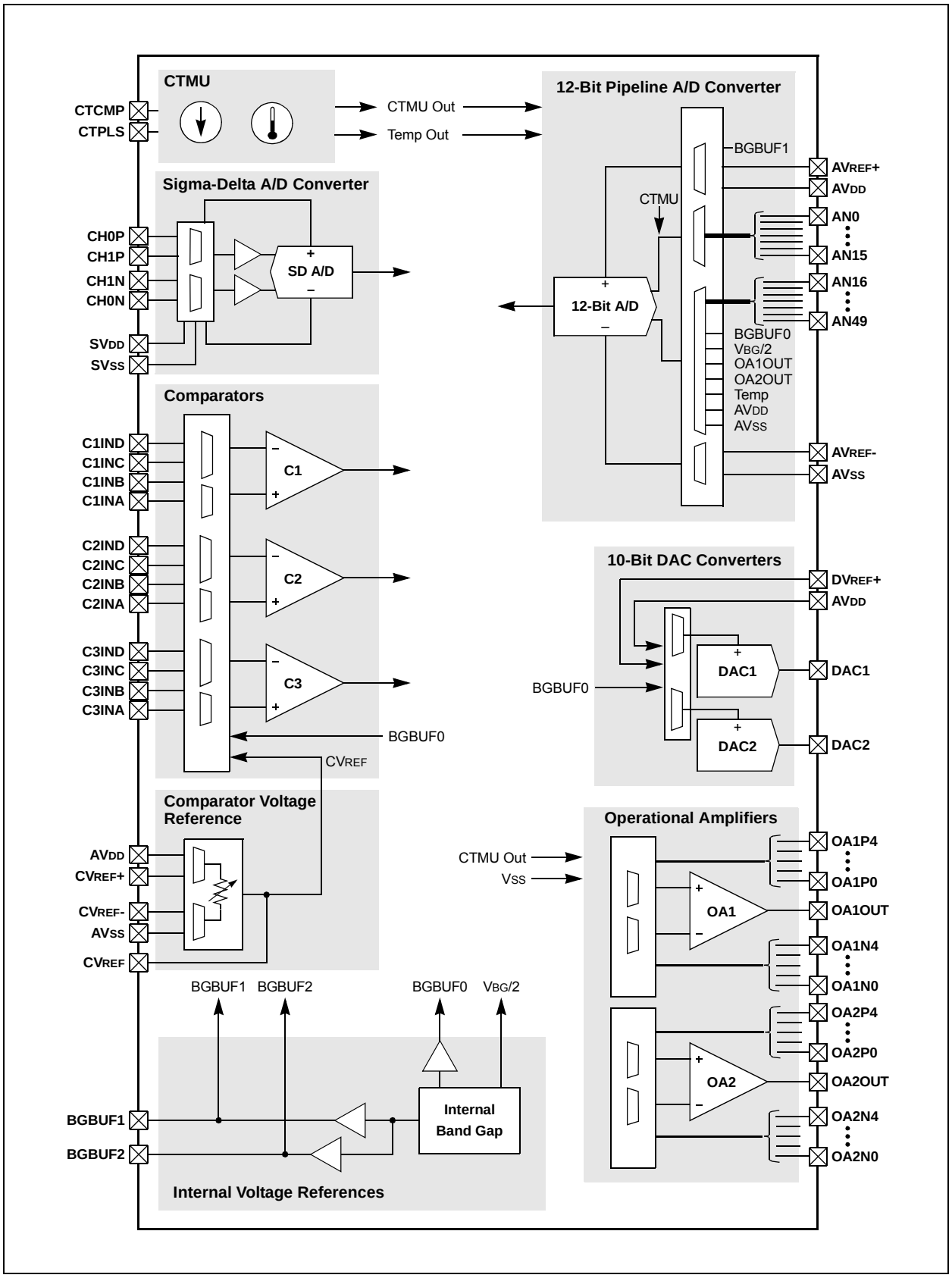
To configure the output compare module for PWM operation:

1. Configure the OCx output for one of the available Peripheral Pin Select pins.
2. Calculate the desired duty cycles and load them into the OCxR register.
3. Calculate the desired period and load it into the OCxRS register.
4. Select the current OCx as the synchronization source by writing '0x1F' to the SYNCSEL<4:0> bits (OCxCON2<4:0>) and '0' to the OCTRIG bit (OCxCON2<7>).
5. Select a clock source by writing to the OCTSEL<2:0> bits (OCxCON1<12:10>).
6. Enable interrupts, if required, for the timer and output compare modules. The output compare interrupt is required for PWM Fault pin utilization.
7. Select the desired PWM mode in the OCM<2:0> bits (OCxCON1<2:0>).
8. Appropriate Fault inputs may be enabled by using the ENFLT<2:0> bits, as described in Register 15-1.
9. If a timer is selected as a clock source, set the selected timer prescale value. The selected timer's prescaler output is used as the clock input for the OCx timer and not the selected timer output.

| **Note:** | This peripheral contains input and output functions that may need to be configured by the Peripheral Pin Select. See **Section 11.4 "Peripheral Pin Select (PPS)"** for more information. |
|---|---|

**NOTES:**

**FIGURE 25-1: ANALOG BLOCK OVERVIEW**



**REGISTER 26-1: ADCON1: A/D CONTROL REGISTER 1**

| R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| ADON | — | ADSIDL | ADSLP | FORM3 | FORM2 | FORM1 | FORM0 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PUMPEN | ADCAL(2) | — | — | — | — | — | PWRLVL |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **ADON:** A/D Module Enable bit
1 = Module is enabled
0 = Module is disabled (registers are still readable and writable)

bit 14 **Unimplemented:** Read as '0'

bit 13 **ADSIDL:** A/D Stop in Idle Control bit
1 = Halts when CPU is in Idle mode
0 = Continues to operate in CPU Idle mode

bit 12 **ADSLP:** A/D Suspend in Sleep Control bit
1 = Continues operation in Sleep mode
0 = Ignores triggers and clocks when CPU is in Sleep mode

bit 11-8 **FORM<3:0>:** Data Output Format bits
1xxx = Unimplemented, do not use
0111 = Signed Fractional (sddd dddd dddd 0000)
0110 = Fractional (dddd dddd dddd 0000)
0101 = Signed Integer (ssss sddd dddd dddd)
0100 = Integer (0000 dddd dddd dddd )
0011 = Signed Fractional (sddd dddd dddd 0000)
0010 = Fractional (dddd dddd dddd 0000)
0001 = Signed Integer (ssss sddd dddd dddd)
0000 = Integer, Raw Data (0000 dddd dddd dddd)

bit 7 **PUMPEN:** Analog Channel Switch Charge Pump Enable bit
1 = Charge pump for switches is enabled, reducing switch impedance(1)
0 = Charge pump for switches is disabled

bit 6 **ADCAL:** A/D Internal Analog Calibration bit(2)
1 = Initiates internal analog calibration
0 = No operation

bit 5-1 **Unimplemented:** Read as '0'

bit 0 **PWRLVL:** Power Level Select bit
1 = Full-Power mode; A/D clock rates from 1 MHz to 10 MHz are allowed
0 = Low-Power mode; A/D clock rates from 1 MHz to 2.5 MHz are allowed

**Note 1:** Use of the channel switch charge pump is recommended when $AV_{DD}$ < 2.5V.
**2:** When set, ADCAL remains set for at least one $T_{AD}$ and is then automatically cleared by hardware. Manually clearing the bit does not necessarily cancel the calibration routine. Calibration is complete when ADSTATH<1> = 1.

**REGISTER 26-17: ADLnMSEL3: A/D SAMPLE LIST n MULTICHANNEL SELECT REGISTER 3 (n = 0 to 3)**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | MSEL<49:48> | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-2 **Unimplemented:** Read as ‘0’

bit 1-0 **MSEL<49:48>:** A/D Channel Select bits

1 = Corresponding channel participates in multichannel operations for Sample List n

0 = Channel does not participate in multichannel operations

**REGISTER 26-18: ADLnMSEL2: A/D SAMPLE LIST n MULTICHANNEL SELECT REGISTER 2 (n = 0 to 3)**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| MSEL<47:40> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| MSEL<39:32> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-0 **MSEL<47:32>:** A/D Channel Select bits

1 = Corresponding channel participates in multichannel operations for Sample List n

0 = Channel does not participate in multichannel operations

**FIGURE 32-3: TYPICAL CONNECTIONS AND INTERNAL CONFIGURATION FOR TIME MEASUREMENT**

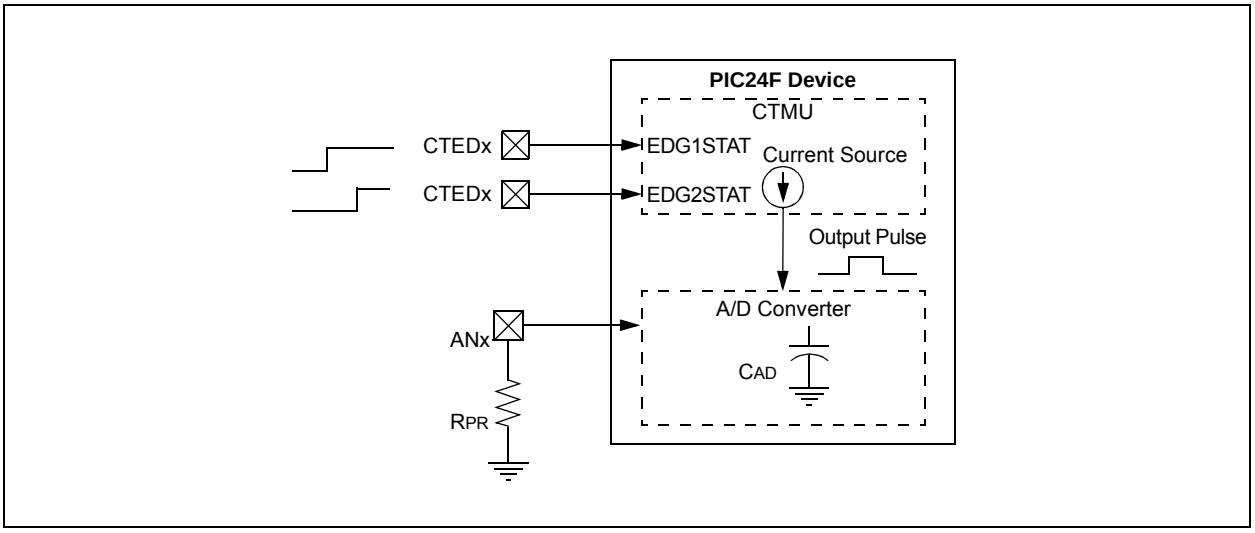
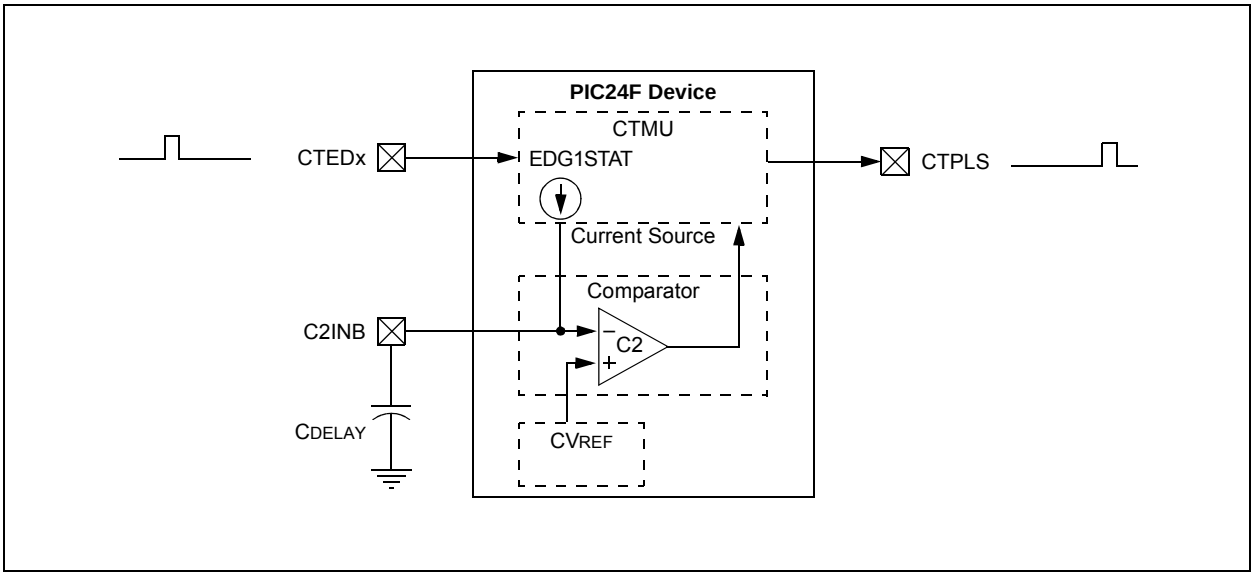



**FIGURE 32-4: TYPICAL CONNECTIONS AND INTERNAL CONFIGURATION FOR PULSE DELAY GENERATION**



**REGISTER 34-3: CW3: FLASH CONFIGURATION WORD 3 (CONTINUED)**

bit 6-0 **WPFP<6:0>:** Write-Protected Code Segment Boundary Page bits(3)
Designates the 512 instruction words page boundary of the protected Code Segment.
If WPEND = 1:
Specifies the lower page boundary of the code-protected segment; the last page being the last implemented page in the device.
If WPEND = 0:
Specifies the upper page boundary of the code-protected segment; Page 0 being the lower boundary.

**Note 1:** Regardless of WPCFG status, if WPEND = 1 or if the WPFP<6:0> bits correspond to the Configuration Word page, the Configuration Word page is protected.

**2:** Ensure that the SCLKI pin is made a digital input while using this configuration (see Table 11-1).

**3:** For the 64K devices (PIC24FJ64GC0XX), maintain WPFP6 as '0'.

**TABLE 37-4: DC CHARACTERISTICS: OPERATING CURRENT (IDD)**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial | | | |
|---|---|---|---|---|---|---|
| **Parameter No.** | **Typical(1)** | **Max** | **Units** | **Operating Temperature** | **VDD** | **Conditions** |
| **Operating Current (IDD)(2)** | | | | | | |
| DC19 | 0.20 | 0.28 | mA | -40°C to +85°C | 2.0V | 0.5 MIPS, FOSC = 1 MHz |
| | 0.21 | 0.28 | mA | -40°C to +85°C | 3.3V | |
| DC20 | 0.38 | 0.52 | mA | -40°C to +85°C | 2.0V | 1 MIPS, FOSC = 2 MHz |
| | 0.39 | 0.52 | mA | -40°C to +85°C | 3.3V | |
| DC23 | 1.5 | 2.0 | mA | -40°C to +85°C | 2.0V | 4 MIPS, FOSC = 8 MHz |
| | 1.5 | 2.0 | mA | -40°C to +85°C | 3.3V | |
| DC24 | 5.6 | 7.6 | mA | -40°C to +85°C | 2.0V | 16 MIPS, FOSC = 32 MHz |
| | 5.7 | 7.6 | mA | -40°C to +85°C | 3.3V | |
| DC31 | 23 | 78 | μA | -40°C to +85°C | 2.0V | LPRC (15.5 KIPS), FOSC = 31 kHz |
| | 25 | 80 | μA | -40°C to +85°C | 3.3V | |

**Note 1:** Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated. Typical parameters are for design guidance only and are not tested.

**2:** The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. No peripheral modules are operating and all of the Peripheral Module Disable (PMD) bits are set.

**TABLE 37-5: DC CHARACTERISTICS: IDLE CURRENT (IIDLE)**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial | | | |
|---|---|---|---|---|---|---|
| **Parameter No.** | **Typical(1)** | **Max** | **Units** | **Operating Temperature** | **VDD** | **Conditions** |
| **Idle Current (IIDLE)** | | | | | | |
| DC40 | 116 | 150 | μA | -40°C to +85°C | 2.0V | 1 MIPS, FOSC = 2 MHz |
| | 123 | 160 | μA | -40°C to +85°C | 3.3V | |
| DC43 | 0.39 | 0.50 | mA | -40°C to +85°C | 2.0V | 4 MIPS, FOSC = 8 MHz |
| | 0.41 | 0.54 | mA | -40°C to +85°C | 3.3V | |
| DC47 | 1.5 | 1.9 | mA | -40°C to +85°C | 2.0V | 16 MIPS, FOSC = 32 MHz |
| | 1.6 | 2.0 | mA | -40°C to +85°C | 3.3V | |
| DC50 | 0.54 | 0.61 | mA | -40°C to +85°C | 2.0V | 4 MIPS (FRC), FOSC = 8 MHz |
| | 0.54 | 0.64 | mA | -40°C to +85°C | 3.3V | |
| DC51 | 17 | 78 | μA | -40°C to +85°C | 2.0V | LPRC (15.5 KIPS), FOSC = 31 kHz |
| | 18 | 80 | μA | -40°C to +85°C | 3.3V | |

**Note 1:** Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**TABLE 37-19: OPERATIONAL AMPLIFIER SPECIFICATIONS**

| **Operating Conditions:** -40°C < TA < +85°C, 2.0V < (A)VDD < 3.6V | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Sym** | **Characteristics** | **Min** | **Typ** | **Max** | **Units** | **Comments** |
| **Op Amp Mode Specifications** | | | | | | | |
| CM20a | SR | Slew Rate | — | 1.2 | — | V/µs | SPDSEL = 1 |
| CM20b | | | — | 0.4 | — | V/µs | SPDSEL = 0 |
| CM23 | GBW | Gain Bandwidth Product | — | 2.5 | — | MHz | SPDSEL = 1 |
| | | | — | 0.5 | — | MHz | SPDSEL = 0 |
| CM33 | VGAIN | DC Open-Loop Gain | — | 80 | — | dB | |
| CM40 | VOFFSET | Input Offset Voltage | — | ±2 | ±14 | mV | |
| CM42 | VCMR | Common-Mode Input Voltage Range | AVSS | — | AVDD | V | |
| CM45 | IB | Input Bias Current | — | — | — | nA | **(Note 1)** |
| CM52 | VOAMAX | Maximum Output Voltage Swing | AVSS + 50 | — | AVDD – 50 | mV | 0.5V input overdrive, no output loading |
| CM53 | IOA | Maximum Continuous Output Current Rating (DC or RMS AC) | — | — | ±6 | mA | This value is not tested in production |
| CM54a | IQOA | AVDD Quiescent Current | — | 190 | — | µA | Module enabled, SPDSEL = 1, no output load |
| CM54b | | | — | 40 | — | µA | Module enabled, SPDSEL = 0, no output load |
| **Comparator Mode Specifications** | | | | | | | |
| CM10a | TRESPL | Large Signal Comparator Response Time | — | 500 | — | ns | SPDSEL = 1, 3V step with 1.5V input overdrive |
| | | | — | 2.6 | — | µs | SPDSEL = 0, 3V step with 1.5V input overdrive |
| CM10b | TRESPS | Small Signal Comparator Response Time | — | 1.6 | — | µs | SPDSEL = 1, 50 mV step with 15 mV input overdrive |
| | | | — | 4.6 | — | µs | SPDSEL = 0, 50 mV step with 15 mV input overdrive |
| CM15 | VCMCR | Common-Mode Input Voltage Range | AVSS | — | AVDD | V | |
| CM16 | TRF | Rise/Fall Time | — | 20 | — | ns | SPDSEL = 1 |

**Note 1:** The op amps use CMOS input circuitry with negligible input bias current. The maximum “effective bias current” is the I/O pin leakage specified by electrical Parameter DI51.

**FIGURE 38-27: PIN VOH vs. IOUT (VDD = 2.0V)**

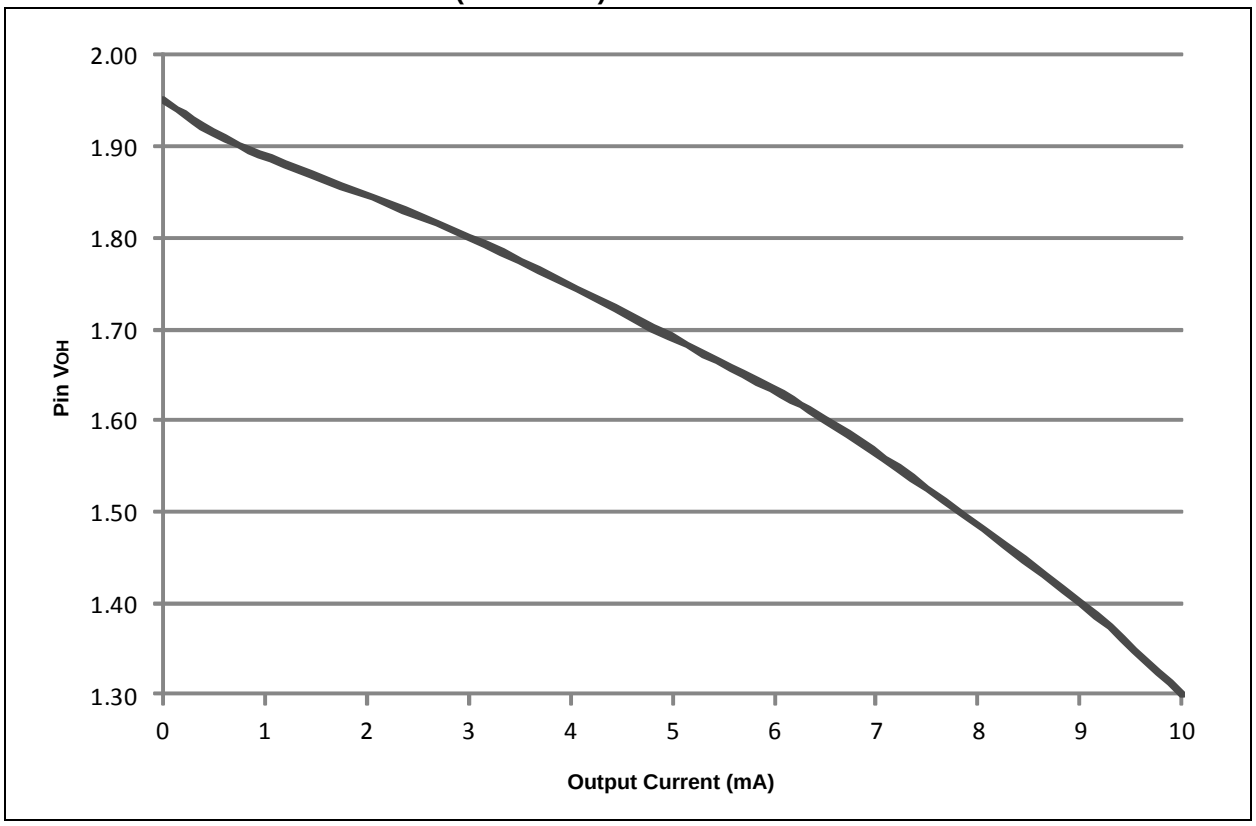
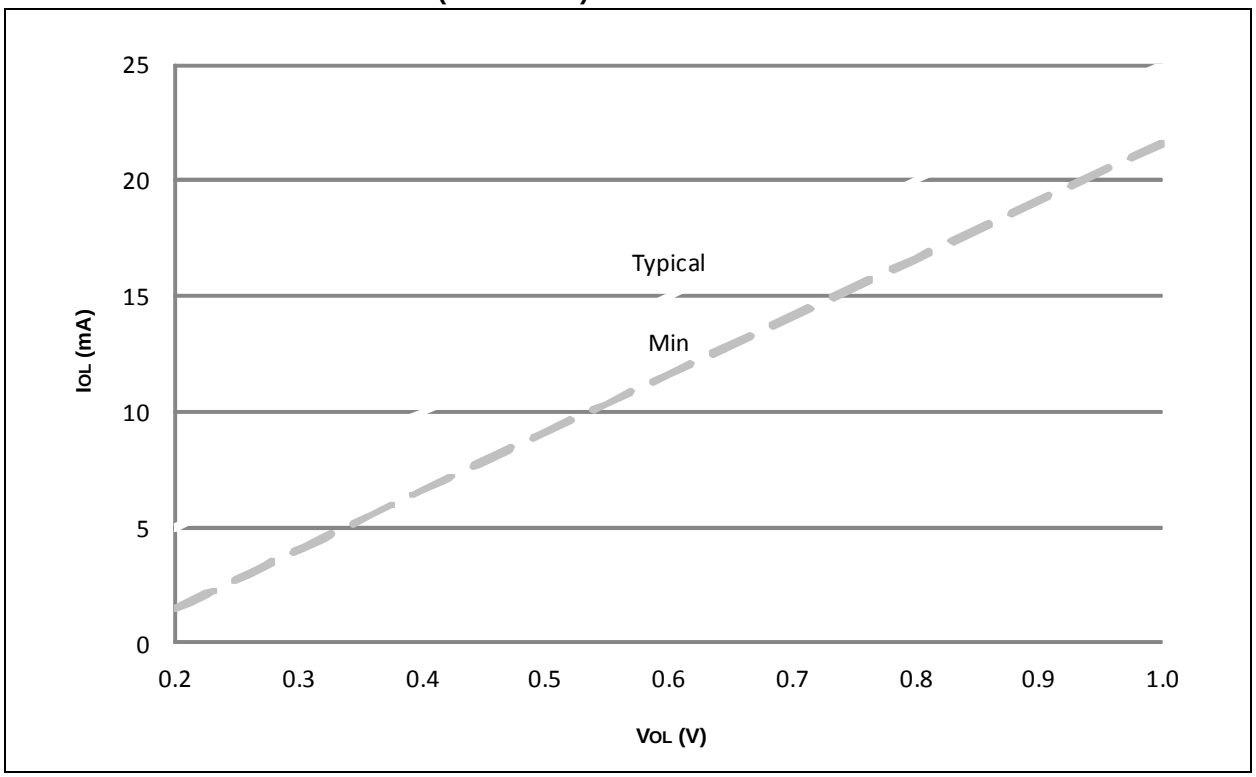



**FIGURE 38-28: IOL vs. PIN VOL (VDD = 3.6V)**



**NOTES:**