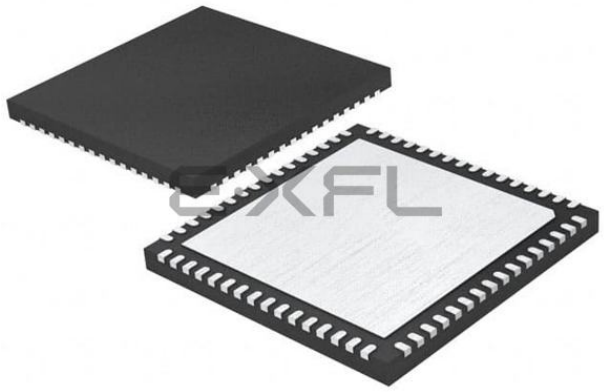
Microchip Technology - PIC24FJ128GC006T-I/MR Datasheet



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, LCD, LVD, POR, PWM, WDT
Number of I/O	53
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 29x12b, 2x16b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj128gc006t-i-mr

TABLE 1-3: PIC24FJ128GC010 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Function	Pin Number/Grid Locator			I/O	Input Buffer	Description
	64-Pin TQFP/QFN	100-Pin TQFP	121-Pin BGA			
RG0	—	90	A5	I/O	ST	PORTG Digital I/Os.
RG1	—	89	E6	I/O	ST	
RG2	37	57	H10	I/O	ST	
RG3	36	56	J11	I/O	ST	
RG6	4	10	E3	I/O	ST	
RG7	5	11	F4	I/O	ST	
RG8	6	12	F2	I/O	ST	
RG9	8	14	F3	I/O	ST	
RG12	—	96	C3	I/O	ST	
RG13	—	97	A3	I/O	ST	
RG14	—	95	C4	I/O	ST	
RG15	—	1	B2	I/O	ST	
RP0	16	25	K2	I/O	ST	Remappable Peripherals (input or output).
RP1	15	24	K1	I/O	ST	
RP2	42	68	E9	I/O	ST	
RP3	44	70	D11	I/O	ST	
RP4	43	69	E10	I/O	ST	
RP5	—	48	K9	I/O	ST	
RP6	17	26	L1	I/O	ST	
RP7	18	27	J3	I/O	ST	
RP10	31	49	L10	I/O	ST	
RP11	46	72	D9	I/O	ST	
RP12	45	71	C11	I/O	ST	
RP13	14	23	J2	I/O	ST	
RP14	29	43	K7	I/O	ST	
RP15	—	53	J10	I/O	ST	
RP16	33	51	K10	I/O	ST	
RP17	32	50	L11	I/O	ST	
RP18	11	20	H1	I/O	ST	
RP19	6	12	F2	I/O	ST	
RP20	53	82	B8	I/O	ST	
RP21	4	10	E3	I/O	ST	
RP22	51	78	B9	I/O	ST	
RP23	50	77	A10	I/O	ST	
RP24	49	76	A11	I/O	ST	
RP25	52	81	C8	I/O	ST	
RP26	5	11	F4	I/O	ST	
RP27	8	14	F3	I/O	ST	
RP28	12	21	H2	I/O	ST	
RP29	30	44	L8	I/O	ST	
RP30	—	52	K11	I/O	ST	
RP31	—	39	L6	I/O	ST	

Legend: TTL = TTL input buffer ST = Schmitt Trigger input buffer
ANA = Analog level input/output I^2C = I^2C/SMBus input buffer

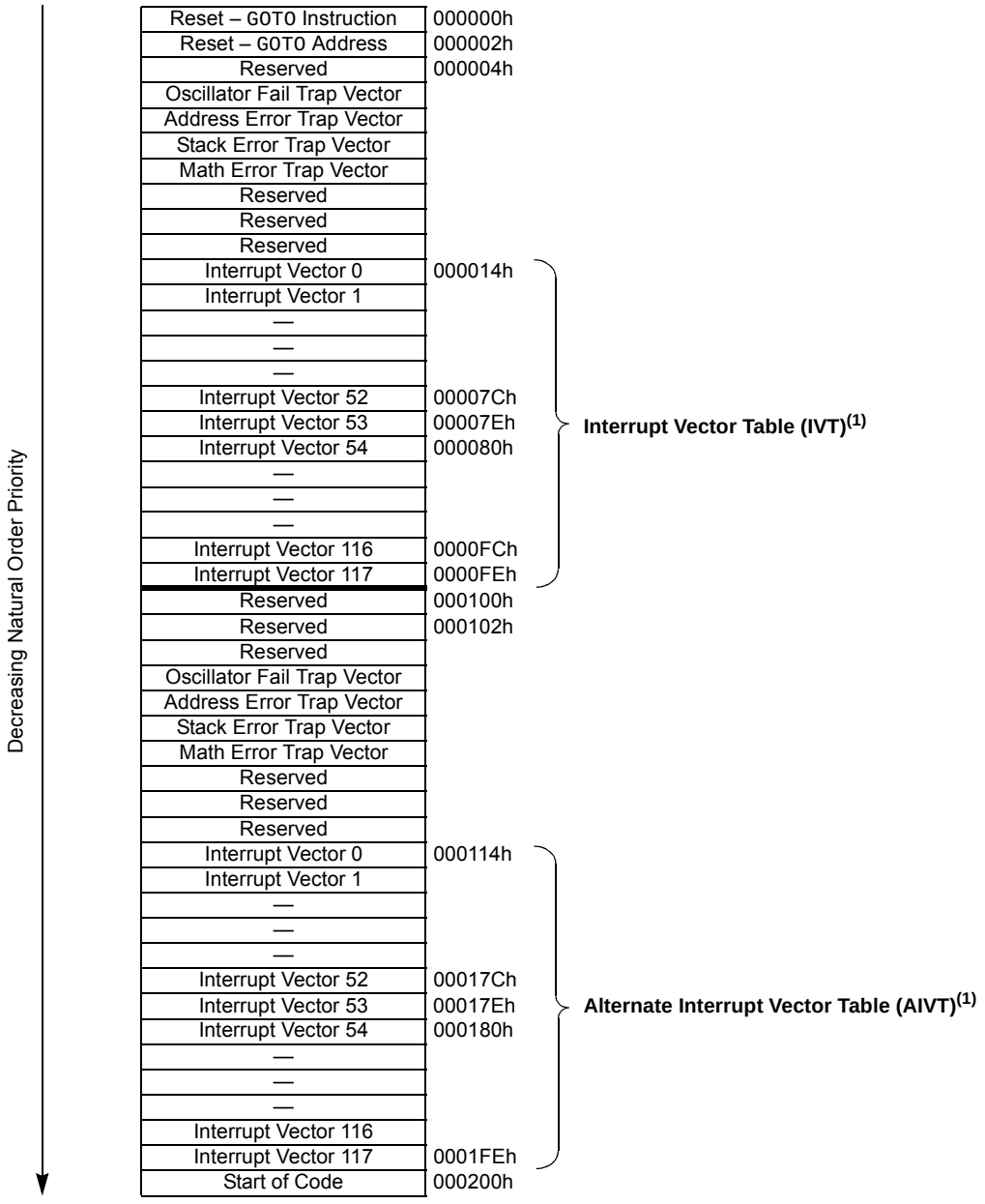
TABLE 4-35: PERIPHERAL PIN SELECT REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPINR0	0680	—	—	INT1R5	INT1R4	INT1R3	INT1R2	INT1R1	INT1R0	—	—	—	—	—	—	—	—	003F
RPINR1	0682	—	—	INT3R5	INT3R4	INT3R3	INT3R2	INT3R1	INT3R0	—	—	INT2R5	INT2R4	INT2R3	INT2R2	INT2R1	INT2R0	3F00
RPINR2	0684	—	—	—	—	—	—	—	—	—	—	INT4R5	INT4R4	INT4R3	INT4R2	INT4R1	INT4R0	3F3F
RPINR7	068E	—	—	IC2R5	IC2R4	IC2R3	IC2R2	IC2R1	IC2R0	—	—	IC1R5	IC1R4	IC1R3	IC1R2	IC1R1	IC1R0	3F3F
RPINR8	0690	—	—	IC4R5	IC4R4	IC4R3	IC4R2	IC4R1	IC4R0	—	—	IC3R5	IC3R4	IC3R3	IC3R2	IC3R1	IC3R0	3F3F
RPINR9	0692	—	—	IC6R5	IC6R4	IC6R3	IC6R2	IC6R1	IC6R0	—	—	IC5R5	IC5R4	IC5R3	IC5R2	IC5R1	IC5R0	3F3F
RPINR10	0694	—	—	IC8R5	IC8R4	IC8R3	IC8R2	IC8R1	IC8R0	—	—	IC7R5	IC7R4	IC7R3	IC7R2	IC7R1	IC7R0	003F
RPINR11	0696	—	—	OCFBR5	OCFBR4	OCFBR3	OCFBR2	OCFBR1	OCFBR0	—	—	OCFAR5	OCFAR4	OCFAR3	OCFAR2	OCFAR1	OCFAR0	3F3F
RPINR15	069E	—	—	IC9R5	IC9R4	IC9R3	IC9R2	IC9R1	IC9R0	—	—	—	—	—	—	—	—	3F00
RPINR17	06A2	—	—	U3RXR5	U3RXR4	U3RXR3	U3RXR2	U3RXR1	U3RXR0	—	—	—	—	—	—	—	—	3F00
RPINR18	06A4	—	—	U1CTSR5	U1CTSR4	U1CTSR3	U1CTSR2	U1CTSR1	U1CTSR0	—	—	U1RXR5	U1RXR4	U1RXR3	U1RXR2	U1RXR1	U1RXR0	3F3F
RPINR19	06A6	—	—	U2CTSR5	U2CTSR4	U2CTSR3	U2CTSR2	U2CTSR1	U2CTSR0	—	—	U2RXR5	U2RXR4	U2RXR3	U2RXR2	U2RXR1	U2RXR0	3F3F
RPINR20	06A8	—	—	SCK1R5	SCK1R4	SCK1R3	SCK1R2	SCK1R1	SCK1R0	—	—	SDI1R5	SDI1R4	SDI1R3	SDI1R2	SDI1R1	SDI1R0	3F3F
RPINR21	06AA	—	—	U3CTSR5	U3CTSR4	U3CTSR3	U3CTSR2	U3CTSR1	U3CTSR0	—	—	SS1R5	SS1R4	SS1R3	SS1R2	SS1R1	SS1R0	3F3F
RPINR22	06AC	—	—	SCK2R5	SCK2R4	SCK2R3	SCK2R2	SCK2R1	SCK2R0	—	—	SDI2R5	SDI2R4	SDI2R3	SDI2R2	SDI2R1	SDI2R0	3F3F
RPINR23	06AE	—	—	TMRCKR5	TMRCKR4	TMRCKR3	TMRCKR2	TMRCKR1	TMRCKR0	—	—	SS2R5	SS2R4	SS2R3	SS2R2	SS2R1	SS2R0	003F
RPINR27	06B6	—	—	U4CTSR5	U4CTSR4	U4CTSR3	U4CTSR2	U4CTSR1	U4CTSR0	—	—	U4RXR5	U4RXR4	U4RXR3	U4RXR2	U4RXR1	U4RXR0	3F3F
RPINR30	06BC	—	—	—	—	—	—	—	—	—	—	MDMIR5	MDMIR4	MDMIR3	MDMIR2	MDMIR1	MDMIR0	003F
RPINR31	06BE	—	—	MDC2R5	MDC2R4	MDC2R3	MDC2R2	MDC2R1	MDC2R0	—	—	MDC1R5	MDC1R4	MDC1R3	MDC1R2	MDC1R1	MDC1R0	3F3F

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: These bits are unimplemented in 64-pin devices, read as '0'.

FIGURE 8-1: PIC24F INTERRUPT VECTOR TABLE



Note 1: See Table 8-2 for the interrupt vector list.

TABLE 8-1: TRAP VECTOR DETAILS

Vector Number	IVT Address	AIVT Address	Trap Source
0	000004h	000104h	Reserved
1	000006h	000106h	Oscillator Failure
2	000008h	000108h	Address Error
3	00000Ah	00010Ah	Stack Error
4	00000Ch	00010Ch	Math Error
5	00000Eh	00010Eh	Reserved
6	000010h	000110h	Reserved
7	000012h	000112h	Reserved

REGISTER 8-17: IEC4: INTERRUPT ENABLE CONTROL REGISTER 4

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	R/W-0
DAC2IE	DAC1IE	CTMUIE	—	—	—	—	HLVDIE
bit 15							bit 8

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	U-0
—	—	—	—	CRCIE	U2ERIE	U1ERIE	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **DAC2IE:** DAC Converter 2 Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 14 **DAC1IE:** DAC Converter 1 Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 13 **CTMUIE:** CTMU Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 12-9 **Unimplemented:** Read as '0'

bit 8 **HLVDIE:** High/Low-Voltage Detect Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 7-4 **Unimplemented:** Read as '0'

bit 3 **CRCIE:** CRC Generator Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 2 **U2ERIE:** UART2 Error Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 1 **U1ERIE:** UART1 Error Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 0 **Unimplemented:** Read as '0'

REGISTER 8-26: IPC5: INTERRUPT PRIORITY CONTROL REGISTER 5

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	IC8IP2	IC8IP1	IC8IP0	—	IC7IP2	IC7IP1	IC7IP0
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0
—	—	—	—	—	INT1IP2	INT1IP1	INT1IP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **IC8IP<2:0>:** Input Capture Channel 8 Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as ‘0’

bit 10-8 **IC7IP<2:0>:** Input Capture Channel 7 Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7-3 **Unimplemented:** Read as ‘0’

bit 2-0 **INT1IP<2:0>:** External Interrupt 1 Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

REGISTER 8-44: IPC26: INTERRUPT PRIORITY CONTROL REGISTER 26

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0
—	—	—	—	—	FSTIP2	FSTIP1	FSTIP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	SDA1IP2	SDA1IP1	SDA1IP0	—	AMP2IP2	AMP2IP1	AMP2IP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-11 **Unimplemented:** Read as '0'

bit 10-8 **FSTIP<2:0>:** FRC Self-Tune Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **SDA1IP<2:0>:** Sigma-Delta A/D Converter Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **AMP2IP<2:0>:** Op Amp 2 Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

REGISTER 15-2: OCxCON2: OUTPUT COMPARE x CONTROL REGISTER 2 (CONTINUED)

bit 4-0 **SYNCSEL<4:0>:** Trigger/Synchronization Source Selection bits
11111 = This OC module(1)
11110 = OCTRIG1 external input
11101 = OCTRIG2 external input
11100 = CTMU(2)
11011 = Pipeline A/D(2)
11010 = Comparator 3(2)
11001 = Comparator 2(2)
11000 = Comparator 1(2)
10111 = Input Capture 8(2)
10110 = Input Capture 7(2)
10101 = Input Capture 6(2)
10100 = Input Capture 5(2)
10011 = Input Capture 4(2)
10010 = Input Capture 3(2)
10001 = Input Capture 2(2)
10000 = Input Capture 1(2)
01111 = Timer5
01110 = Timer4
01101 = Timer3
01100 = Timer2
01011 = Timer1
01010 = Input Capture 9(2)
01001 = Output Compare 9(1)
01000 = Output Compare 8(1)
00111 = Output Compare 7(1)
00110 = Output Compare 6(1)
00101 = Output Compare 5(1)
00100 = Output Compare 4(1)
00011 = Output Compare 3(1)
00010 = Output Compare 2(1)
00001 = Output Compare 1(1)
00000 = Not synchronized to any other module

Note 1: Never use an OC module as its own trigger source, either by selecting this mode or another equivalent SYNCSELx setting.
2: Use these inputs as trigger sources only and never as sync sources.
3: The DCB<1:0> bits are double-buffered in PWM modes only (OCM<2:0> (OCxCON1<2:0>) = 111, 110).

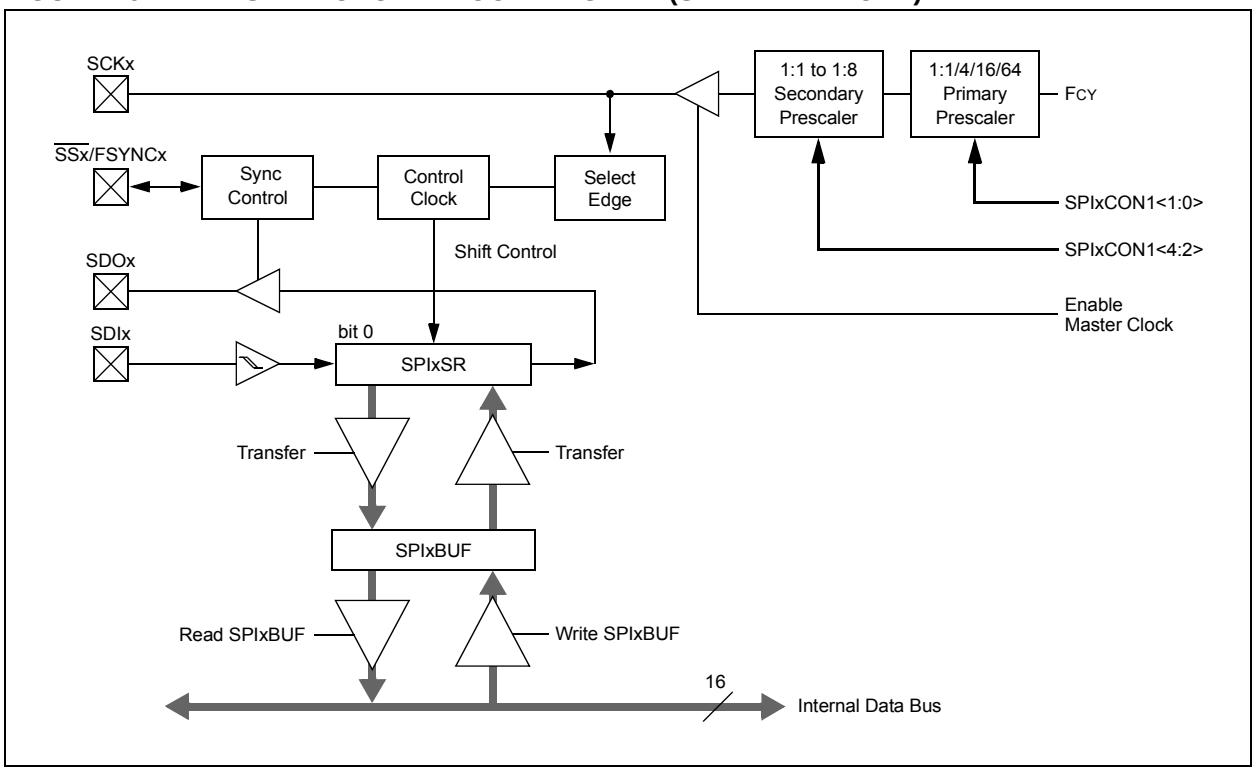
To set up the SPIx module for the Standard Master mode of operation:

1. If using interrupts:
   a) Clear the SPIxIF bit in the respective IFSx register.
   b) Set the SPIxIE bit in the respective IECx register.
   c) Write the SPIxIP<2:0> bits in the respective IPCx register to set the interrupt priority.
2. Write the desired settings to the SPIxCON1 and SPIxCON2 registers with the MSTEN bit (SPIxCON1<5>) = 1.
3. Clear the SPIROV bit (SPIxSTAT<6>).
4. Enable SPI operation by setting the SPIEN bit (SPIxSTAT<15>).
5. Write the data to be transmitted to the SPIxBUF register. Transmission (and reception) will start as soon as data is written to the SPIxBUF register.

To set up the SPIx module for the Standard Slave mode of operation:

1. Clear the SPIxBUF register.
2. If using interrupts:
   a) Clear the SPIxIF bit in the respective IFSx register.
   b) Set the SPIxIE bit in the respective IECx register.
   c) Write the SPIxIP<2:0> bits in the respective IPCx register to set the interrupt priority.
3. Write the desired settings to the SPIxCON1 and SPIxCON2 registers with the MSTEN bit (SPIxCON1<5>) = 0.
4. Clear the SMP bit.
5. If the CKE bit (SPIxCON1<8>) is set, then the SSEN bit (SPIxCON1<7>) must be set to enable the $\overline{SSx}$ pin.
6. Clear the SPIROV bit (SPIxSTAT<6>).
7. Enable SPI operation by setting the SPIEN bit (SPIxSTAT<15>).

FIGURE 16-1: SPIx MODULE BLOCK DIAGRAM (STANDARD MODE)



REGISTER 18-1: UxMODE: UARTx MODE REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
UARTEN(1)	—	USIDL	IREN(2)	RTSMD	—	UEN1	UEN0
bit 15							bit 8

R/W-0, HC	R/W-0	R/W-0, HC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL1	PDSEL0	STSEL
bit 7							bit 0

Legend:	HC = Hardware Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **UARTEN:** UARTx Enable bit(1)
- 1 = UARTx is enabled, all UARTx pins are controlled by UARTx as defined by UEN<1:0>
- 0 = UARTx is disabled, all UARTx pins are controlled by port latches; UARTx power consumption is minimal

bit 14 **Unimplemented:** Read as '0'

bit 13 **USIDL:** UARTx Stop in Idle Mode bit
- 1 = Discontinues module operation when device enters Idle mode
- 0 = Continues module operation in Idle mode

bit 12 **IREN:** IrDA® Encoder and Decoder Enable bit(2)
- 1 = IrDA encoder and decoder are enabled
- 0 = IrDA encoder and decoder are disabled

bit 11 **RTSMD:** Mode Selection for $\overline{\text{UxRTS}}$ Pin bit
- 1 = $\overline{\text{UxRTS}}$ pin is in Simplex mode
- 0 = $\overline{\text{UxRTS}}$ pin is in Flow Control mode

bit 10 **Unimplemented:** Read as '0'

bit 9-8 **UEN<1:0>:** UARTx Enable bits
- 11 = UxTX, UxRX and BCLKx pins are enabled and used; $\overline{\text{UxCTS}}$ pin is controlled by port latches
- 10 = UxTX, UxRX, $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins are enabled and used
- 01 = UxTX, UxRX and $\overline{\text{UxRTS}}$ pins are enabled and used; $\overline{\text{UxCTS}}$ pin is controlled by port latches
- 00 = UxTX and UxRX pins are enabled and used; $\overline{\text{UxCTS}}$ and the $\overline{\text{UxRTS}}$/BCLKx pins are controlled by port latches

bit 7 **WAKE:** Wake-up on Start Bit Detect During Sleep Mode Enable bit
- 1 = UARTx will continue to sample the UxRX pin; interrupt is generated on the falling edge, bit is cleared in hardware on the following rising edge
- 0 = No wake-up is enabled

bit 6 **LPBACK:** UARTx Loopback Mode Select bit
- 1 = Enables Loopback mode
- 0 = Loopback mode is disabled

bit 5 **ABAUD:** Auto-Baud Enable bit
- 1 = Enables baud rate measurement on the next character – requires reception of a Sync field (55h); cleared in hardware upon completion
- 0 = Baud rate measurement is disabled or completed

Note 1: If UARTEN = 1, the peripheral inputs and outputs must be configured to an available RPn/RPIn pin. See **Section 11.4 "Peripheral Pin Select (PPS)"** for more information.

2: This feature is only available for the 16x BRG mode (BRGH = 0).

19.1 Hardware Configuration

19.1.1 DEVICE MODE

19.1.1.1 D+ Pull-up Resistor

PIC24FJ128GC010 family devices have a built-in 1.5 kΩ resistor on the D+ line that is available when the microcontroller is operating in Device mode. This is used to signal an external host that the device is operating in Full-Speed Device mode. It is engaged by setting the USBEN bit (U1CON<0>) and powering up the USB module (USBPWR = 1). If the OTGEN bit (U1OTGCON<2>) is set, then the D+ pull-up is enabled through the DPPULUP bit (U1OTGCON<7>).

19.1.1.2 The VBUS Pin

In order to meet the USB 2.0 specification requirement relating to the back drive voltage on the D+/D- pins, the USB module incorporates VBUS-level sensing comparators. When the comparators detect the VBUS level below the VA_SESS_VLD level, the hardware will automatically disable the D+ pull-up resistor described in **Section 19.1.1.1 "D+ Pull-up Resistor"**. This allows the device to automatically meet the back drive requirement for D+ and D-, even if the application firmware does not explicitly monitor the VBUS level. Therefore, the VBUS microcontroller pin should not be left floating in USB Device mode application designs and should normally be connected to the VBUS pin on the USB connector/cable (either directly or through a small resistance ≤ 100 ohms).

19.1.1.3 Power Modes

Many USB applications will likely have several different sets of power requirements and configuration. The most common power modes encountered are:

- Bus Power Only mode
- Self-Power Only mode
- Dual Power with Self-Power Dominance

Bus Power Only mode (Figure 19-2) is effectively the simplest method. All power for the application is drawn from the USB.

To meet the inrush current requirements of the *"USB 2.0 OTG Specification"*, the total effective capacitance, appearing across VBUS and ground, must be no more than 10 μF.

In the USB Suspend mode, devices must consume no more than 2.5 mA from the 5V VBUS line of the USB cable. During the USB Suspend mode, the D+ or D- pull-up resistor must remain active, which will consume some of the allowed suspend current.

In Self-Power Only mode (Figure 19-3), the USB application provides its own power, with very little power being pulled from the USB. Note that an attach indication is added to indicate when the USB has been connected and the host is actively powering VBUS.

To meet compliance specifications, the USB module (and the D+ or D- pull-up resistor) should not be enabled until the host actively drives VBUS high. One of the 5.5V tolerant I/O pins may be used for this purpose.

The application should never source any current onto the 5V VBUS pin of the USB cable when the USB module is operated in USB Device mode.

The Dual Power mode with Self-Power Dominance (Figure 19-4) allows the application to use internal power primarily, but switch to power from the USB when no internal power is available. Dual power devices must also meet all of the special requirements for inrush current and Suspend mode current previously described, and must not enable the USB module until VBUS is driven high.

FIGURE 19-2: BUS POWER ONLY INTERFACE EXAMPLE

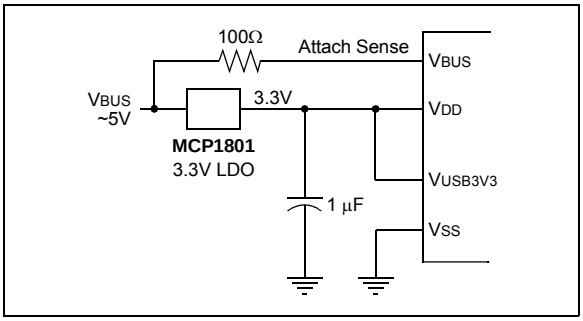


FIGURE 19-3: SELF-POWER ONLY

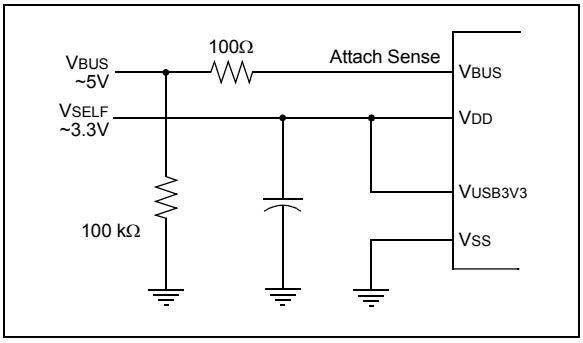
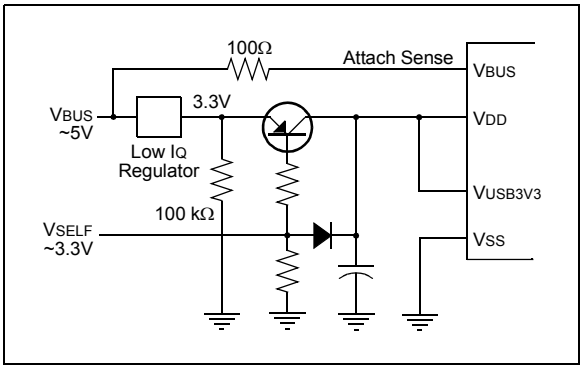


FIGURE 19-4: DUAL POWER EXAMPLE



19.3 USB Interrupts

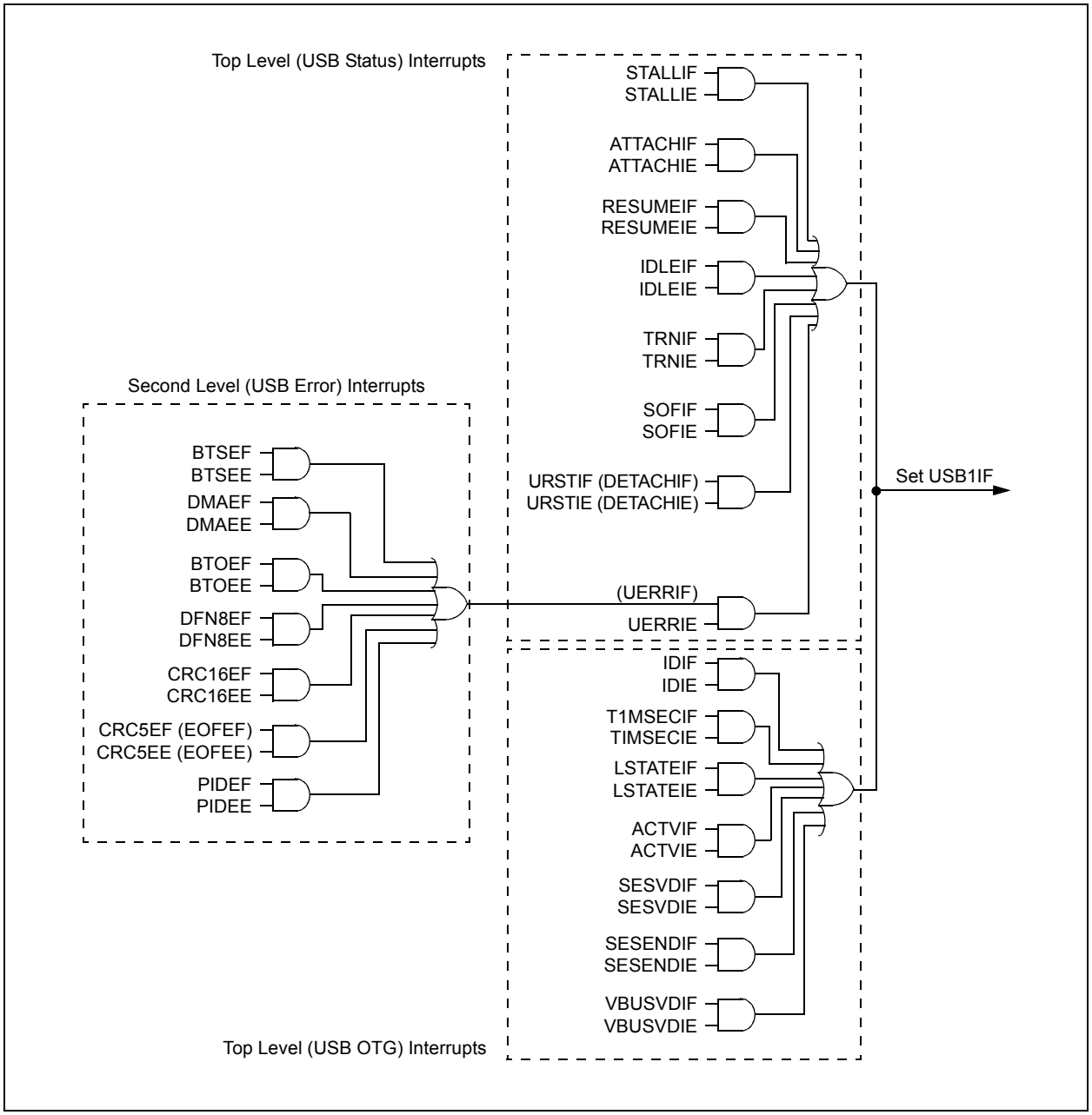
The USB OTG module has many conditions that can be configured to cause an interrupt. All interrupt sources use the same interrupt vector.

Figure 19-8 shows the interrupt logic for the USB module. There are two layers of interrupt registers in the USB module. The top level consists of overall USB status interrupts; these are enabled and flagged in the U1IE and U1IR registers, respectively. The second level consists of USB error conditions, which are enabled and flagged in the U1EIR and U1EIE registers.

An interrupt condition in any of these triggers a USB Error Interrupt Flag (UERRIF) in the top level. Unlike the device-level interrupt flags in the IFSx registers, USB interrupt flags in the U1IR registers can only be cleared by writing a '1' to the bit position.

Interrupts may be used to trap routine events in a USB transaction. Figure 19-9 provides some common events within a USB frame and their corresponding interrupts.

FIGURE 19-8: USB OTG INTERRUPT FUNNEL



REGISTER 22-2: LCDREG: LCD CHARGE PUMP CONTROL REGISTER

RW-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
CPEN	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	RW-1	RW-1	RW-1	RW-1	RW-0	RW-0
—	—	BIAS2	BIAS1	BIAS0	MODE13	CKSEL1	CKSEL0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CPEN:** 3.6V Charge Pump Enable bit
1 = The regulator generates the highest (3.6V) voltage
0 = Highest voltage in the system is supplied externally (AV_{DD})

bit 14-6 **Unimplemented:** Read as '0'

bit 5-3 **BIAS<2:0>:** Regulator Voltage Output Control bits
111 = 3.60V peak (offset on LCDBIAS0 of 0V)
110 = 3.47V peak (offset on LCDBIAS0 of 0.13V)
101 = 3.34V peak (offset on LCDBIAS0 of 0.26V)
100 = 3.21V peak (offset on LCDBIAS0 of 0.39V)
011 = 3.08V peak (offset on LCDBIAS0 of 0.52V)
010 = 2.95V peak (offset on LCDBIAS0 of 0.65V)
001 = 2.82V peak (offset on LCDBIAS0 of 0.78V)
000 = 2.69V peak (offset on LCDBIAS0 of 0.91V)

bit 2 **MODE13:** 1/3 LCD Bias Enable bit
1 = Regulator output supports 1/3 LCD Bias mode
0 = Regulator output supports Static LCD Bias mode

bit 1-0 **CLKSEL<1:0>:** Regulator Clock Select Control bits
11 = SOSC
10 = 8 MHz FRC
01 = 31 kHz LPRC
00 = Disables regulator and floats regulator voltage output

23.3.3 ALRMVAL REGISTER MAPPINGS

REGISTER 23-8: ALMTHDY: ALARM MONTH AND DAY VALUE REGISTER(1)

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0
bit 15							bit 8

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	DAYTEN1	DAYTEN0	DAYONE3	DAYONE2	DAYONE1	DAYONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12 **MTHTEN0:** Binary Coded Decimal Value of Month's Tens Digit bit
Contains a value of '0' or '1'.

bit 11-8 **MTHONE<3:0>:** Binary Coded Decimal Value of Month's Ones Digit bits
Contains a value from 0 to 9.

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **DAYTEN<1:0>:** Binary Coded Decimal Value of Day's Tens Digit bits
Contains a value from 0 to 3.

bit 3-0 **DAYONE<3:0>:** Binary Coded Decimal Value of Day's Ones Digit bits
Contains a value from 0 to 9.

Note 1: A write to this register is only allowed when RTCWREN = 1.

REGISTER 23-9: ALWDHR: ALARM WEEKDAY AND HOURS VALUE REGISTER(1)

U-0	U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x
—	—	—	—	—	WDAY2	WDAY1	WDAY0
bit 15							bit 8

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-11 **Unimplemented:** Read as '0'

bit 10-8 **WDAY<2:0>:** Binary Coded Decimal Value of Weekday Digit bits
Contains a value from 0 to 6.

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **HRTEN<1:0>:** Binary Coded Decimal Value of Hour's Tens Digit bits
Contains a value from 0 to 2.

bit 3-0 **HRONE<3:0>:** Binary Coded Decimal Value of Hour's Ones Digit bits
Contains a value from 0 to 9.

Note 1: A write to this register is only allowed when RTCWREN = 1.

32.4 Measuring Die Temperature

The CTMU can be configured to use the 12-bit Pipeline A/D to measure the die temperature using dedicated A/D Channel 50. Perform the following steps to measure the diode voltage:

- The internal current source must be set for either 5.5 µA (IRNG<1:0> = 0x2) or 55 µA (IRNG<1:0> = 0x3).
- In order to route the current source to the diode, the EDG1STAT and EDG2STAT bits must be equal (either both '0' or both '1').
- The CTMEN bit in the A/D sample list (ADLnCONH<7>) must be set to '0'.
- Due to the high noise floor of the Pipeline A/D, it is recommended to average at least 8 readings of the diode voltage before calculating the temperature.
- The A/D Channel Select bits must be 50 ('0x32') using a single-ended measurement.

The voltage of the diode will vary over temperature according to the graphs shown below. Note that the graphs are different, based on the magnitude of the current source selected. The slopes are nearly linear over the range of -40ºC to +100ºC and the temperature can be calculated as follows:

EQUATION 32-2:

For 5.5 µA Current Source:

$$Tdie = \frac{710\ mV - Vdiode}{1.8}$$

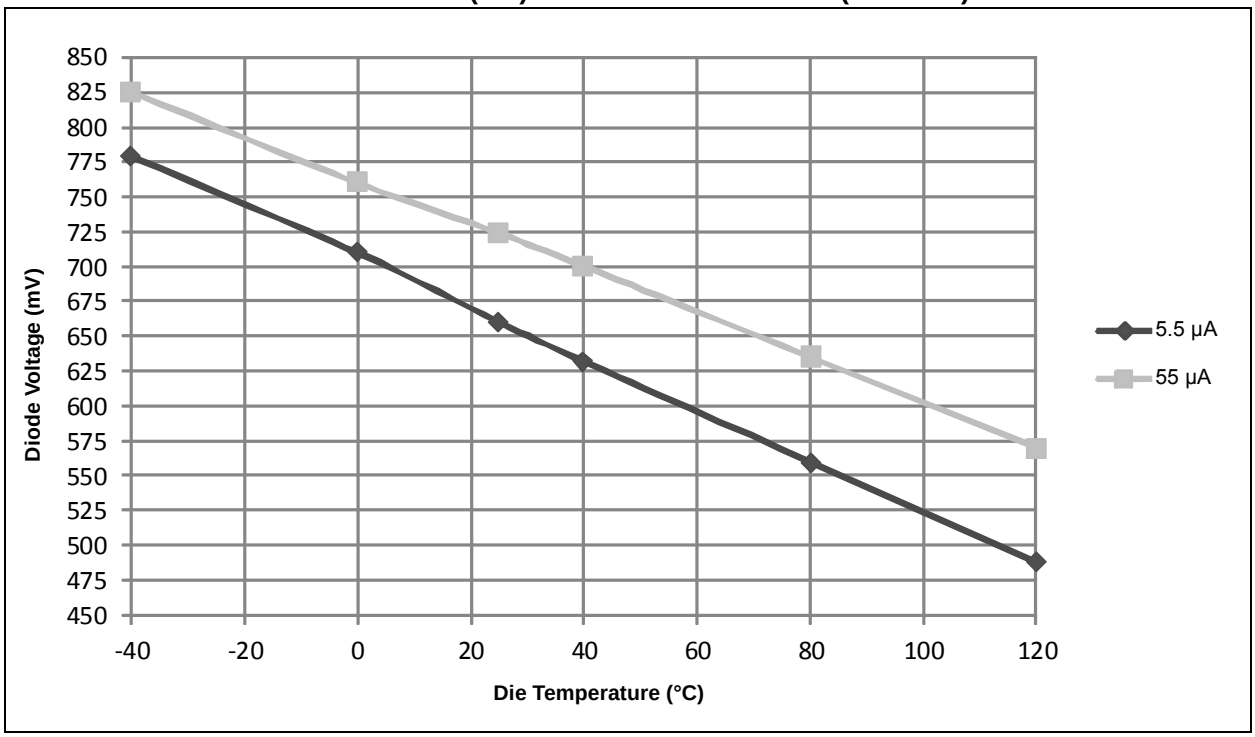
where *Vdiode* is in *mV*, *Tdie* is in ºC

For 55 µA Current Source:

$$Tdie = \frac{760\ mV - Vdiode}{1.55}$$

where *Vdiode* is in *mV*, *Tdie* is in ºC

FIGURE 32-2: DIODE VOLTAGE (mV) vs. DIE TEMPERATURE (TYPICAL)



REGISTER 34-3: CW3: FLASH CONFIGURATION WORD 3 (CONTINUED)

bit 6-0 **WPFP<6:0>:** Write-Protected Code Segment Boundary Page bits(3)
Designates the 512 instruction words page boundary of the protected Code Segment.
If WPEND = 1:
Specifies the lower page boundary of the code-protected segment; the last page being the last implemented page in the device.
If WPEND = 0:
Specifies the upper page boundary of the code-protected segment; Page 0 being the lower boundary.

Note 1: Regardless of WPCFG status, if WPEND = 1 or if the WPFP<6:0> bits correspond to the Configuration Word page, the Configuration Word page is protected.

2: Ensure that the SCLKI pin is made a digital input while using this configuration (see Table 11-1).

3: For the 64K devices (PIC24FJ64GC0XX), maintain WPFP6 as '0'.

34.4 Program Verification and Code Protection

PIC24FJ128GC010 family devices provide two complimentary methods to protect application code from overwrites and erasures. These also help to protect the device from inadvertent configuration changes during run time.

34.4.1 GENERAL SEGMENT PROTECTION

For all devices in the PIC24FJ128GC010 family, the on-chip program memory space is treated as a single block, known as the General Segment (GS). Code protection for this block is controlled by one Configuration bit, GCP. This bit inhibits external reads and writes to the program memory space. It has no direct effect in normal execution mode.

Write protection is controlled by the GWRP bit in the Configuration Word. When GWRP is programmed to '0', internal write and erase operations to program memory are blocked.

34.4.2 CODE SEGMENT PROTECTION

In addition to global General Segment protection, a separate subrange of the program memory space can be individually protected against writes and erases. This area can be used for many purposes where a separate block of write and erase-protected code is needed, such as bootloader applications. Unlike common boot block implementations, the specially protected segment in the PIC24FJ128GC010 family devices can be located by the user anywhere in the program space and configured in a wide range of sizes.

Code Segment (CS) protection provides an added level of protection to a designated area of program memory by disabling the NVM safety interlock whenever a write or erase address falls within a specified range. It does not override General Segment protection, controlled by the GCP or GWRP bit. For example, if GCP and GWRP are enabled, enabling segmented code protection for the bottom half of program memory does not undo General Segment protection for the top half.

The size and type of protection for the segmented code range are configured by the WPFPx, WPEND, WPCFG and WPDIS bits in Configuration Word 3. Code Segment protection is enabled by programming the WPDIS bit (= 0). The WPFPx bits specify the size of the segment to be protected by specifying the 512-word code page that is the start or end of the protected segment. The specified region is inclusive, therefore, this page will also be protected.

The WPEND bit determines if the protected segment uses the top or bottom of the program space as a boundary. Programming WPEND (= 0) sets the bottom of program memory (000000h) as the lower boundary of the protected segment. Leaving WPEND unprogrammed (= 1) protects the specified page through the last page of implemented program memory, including the Configuration Word locations.

A separate bit, WPCFG, is used to protect the last page of program space, including the Flash Configuration Words. Programming WPCFG (= 0) protects the last page in addition to the pages selected by the WPEND and WPFP<6:0> bits' setting. This is useful in circumstances where write protection is needed for both the Code Segment in the bottom of the memory and the Flash Configuration Words.

The various options for Code Segment protection are shown in Table 34-2.

TABLE 34-2: CODE SEGMENT PROTECTION CONFIGURATION OPTIONS

Segment Configuration Bits			Write/Erase Protection of Code Segment
WPDIS	WPEND	WPCFG	
1	x	x	No additional protection is enabled; all program memory protection is configured by GCP and GWRP.
0	1	x	Addresses from the first address of the code page are defined by WPFP<6:0> through the end of implemented program memory (inclusive); erase/write-protected, including Flash Configuration Words.
0	0	1	Address, 000000h, through the last address of the code page is defined by WPFP<6:0> (inclusive); erase/write-protected.
0	0	0	Address, 000000h, through the last address of the code page is defined by WPFP<6:0> (inclusive); erase/write-protected and the last page, including Flash Configuration Words, are erase/write-protected.

TABLE 37-11: INTERNAL VOLTAGE REGULATOR SPECIFICATIONS

Operating Conditions: -40°C < TA < +85°C (unless otherwise stated)							
Param No.	**Symbol**	**Characteristics**	**Min**	**Typ**	**Max**	**Units**	**Comments**
DVR10	VBG	Internal Band Gap Reference	—	1.2	—	V	
DVR11	TBG	Band Gap Reference Start-up Time	—	1	—	ms	
DVR20	VRGOUT	Regulator Output Voltage	—	1.8	—	V	VDD > 2.0V
DVR21	CEFC	External Filter Capacitor Value	4.7	10	—	µF	Series Resistance < 3Ω recommended; < 5Ω required
DVR25	TVREG	Start-up Time	—	10	—	µs	PMSLP = 1 with any POR or BOR
DVR30	VLVR	Low-Voltage Regulator Output Voltage	—	1.2	—	V	RETEN = 1, $\overline{\text{LPCFG}}$ = 0

TABLE 37-12: BAND GAP REFERENCE (BGBUFn) SPECIFICATIONS

Operating Conditions: -40°C < TA < +85°C, 2.0V < (A)VDD < 3.6V(1)							
Param No.	**Sym**	**Characteristics**	**Min**	**Typ**	**Max**	**Units**	**Comments**
DBG01		Recommended Output Capacitance for Optimal Transient Response	—	—	22	µF	BGBUF1 or BGBUF2
DBG02		Output Voltage	1.140	1.200	1.260	V	BUFREF<1:0> = 00, 2.0V < AVDD < 3.6V
DBG03			1.945	2.048	2.151	V	BUFREF<1:0> = 01(2)
DBG04			2.432	2.560	2.688	V	BUFREF<1:0> = 10(2)
DBG05			2.918	3.072	3.226	V	BUFREF<1:0> = 11(2)
DBG07		DC Output Resistance	20	—	—	Ω	BUFREF<1:0> = 00, 2.0V < AVDD ≤ 2.5V
DBG08			20	—	—	Ω	BUFREF<1:0> = 00, 2.5V < AVDD < 3.6V
DBG09			20	—	—	Ω	BUFREF<1:0> = 01, 10 or 11(2)
DBG10		Maximum Continuous DC Output Current Rating	—	—	1	mA	This value is not tested in production(3)
DBG11		Module Start-up Time from Disabled State	—	5	—	ms	Time from BUFEN and BUFOE = 1 to output stable, CLOAD = 20 µF
DBG12		Module Start-up Time from Standby Mode	—	100	—	µs	Time from BUFSTBY = 0 to output stable
DBG14		AVDD Active Current	—	100	—	µA	Module enabled, BUFOE = 1

Note 1: No DC loading on module unless otherwise stated.

2: For BUFREF<1:0> ≠ 00, (Reference Output Max + 100 mV) < AVDD < 3.6V.

3: To minimize voltage error, the DC loading on the BGBUFn output pins should be <100 µA.

FIGURE 38-7: THD vs. OSR (V_{DD} = 3.3V, V_{REF} = 2.0V, F_{IN} = 25 Hz, +25°C)

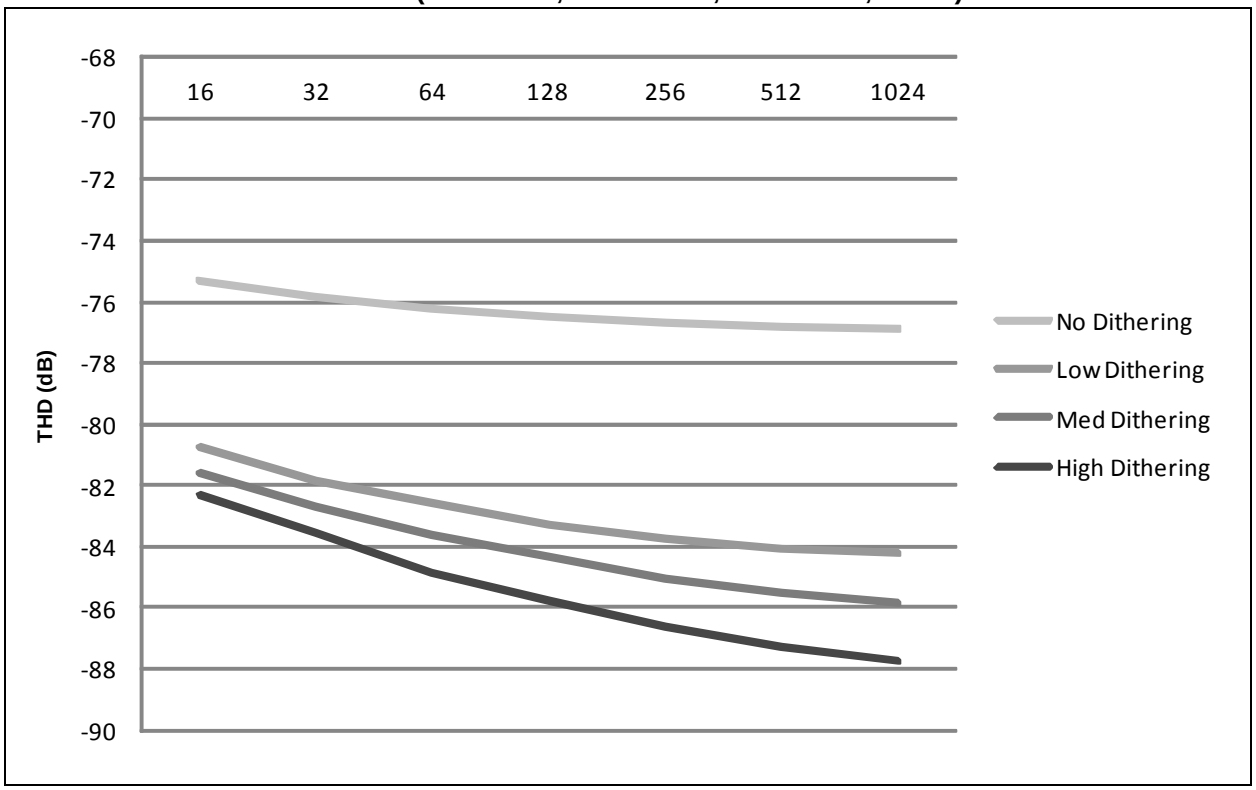


FIGURE 38-8: 0.5 MIPS/1 MIPS/LPRC I_{DD} vs. V_{DD} (RUN MODE)

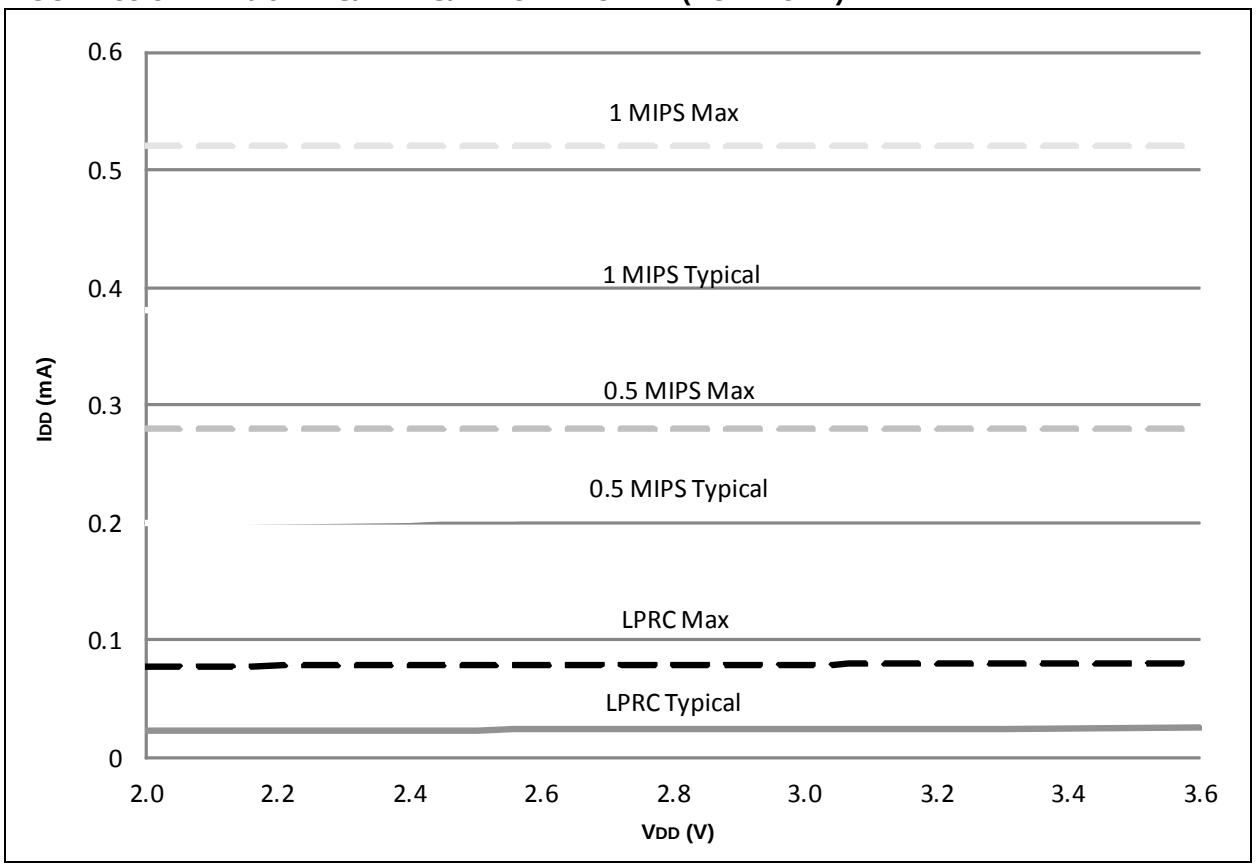


FIGURE 38-47: 10-BIT DAC OFFSET vs. TEMPERATURE

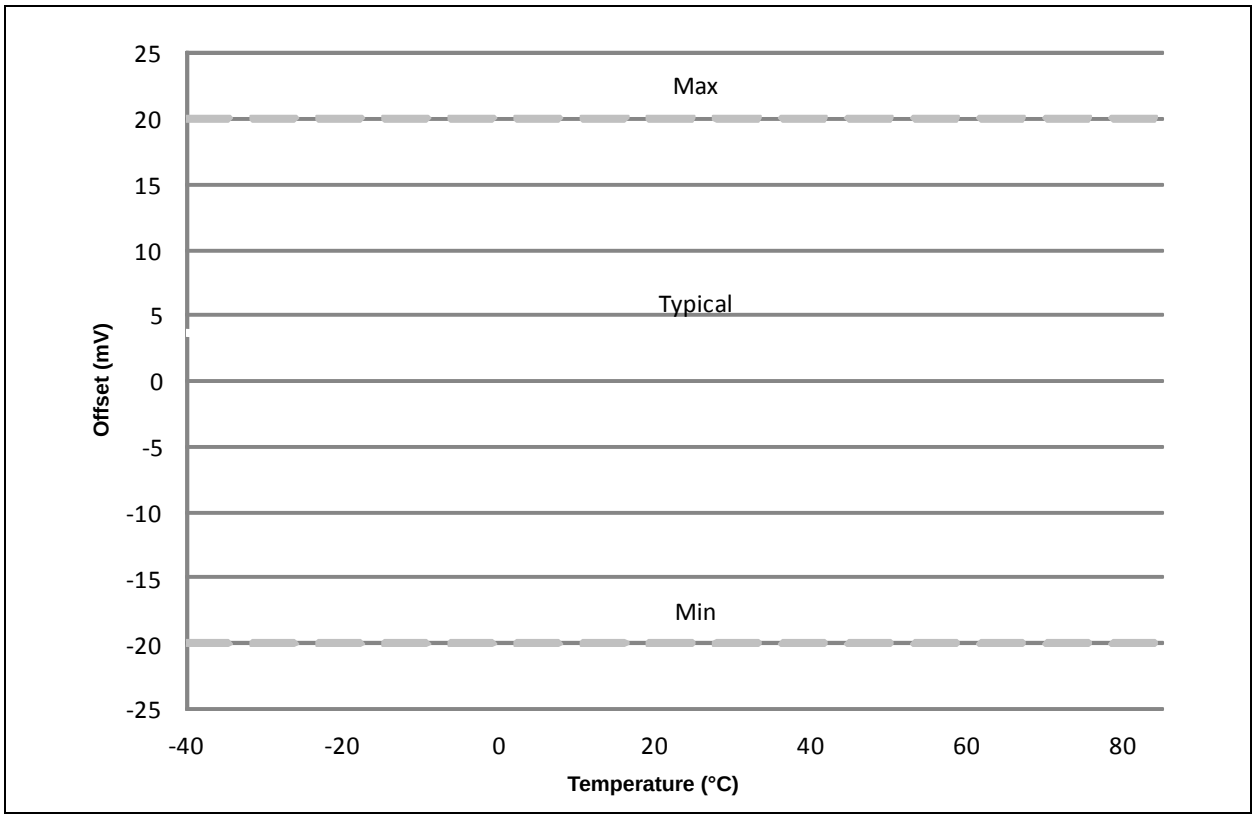
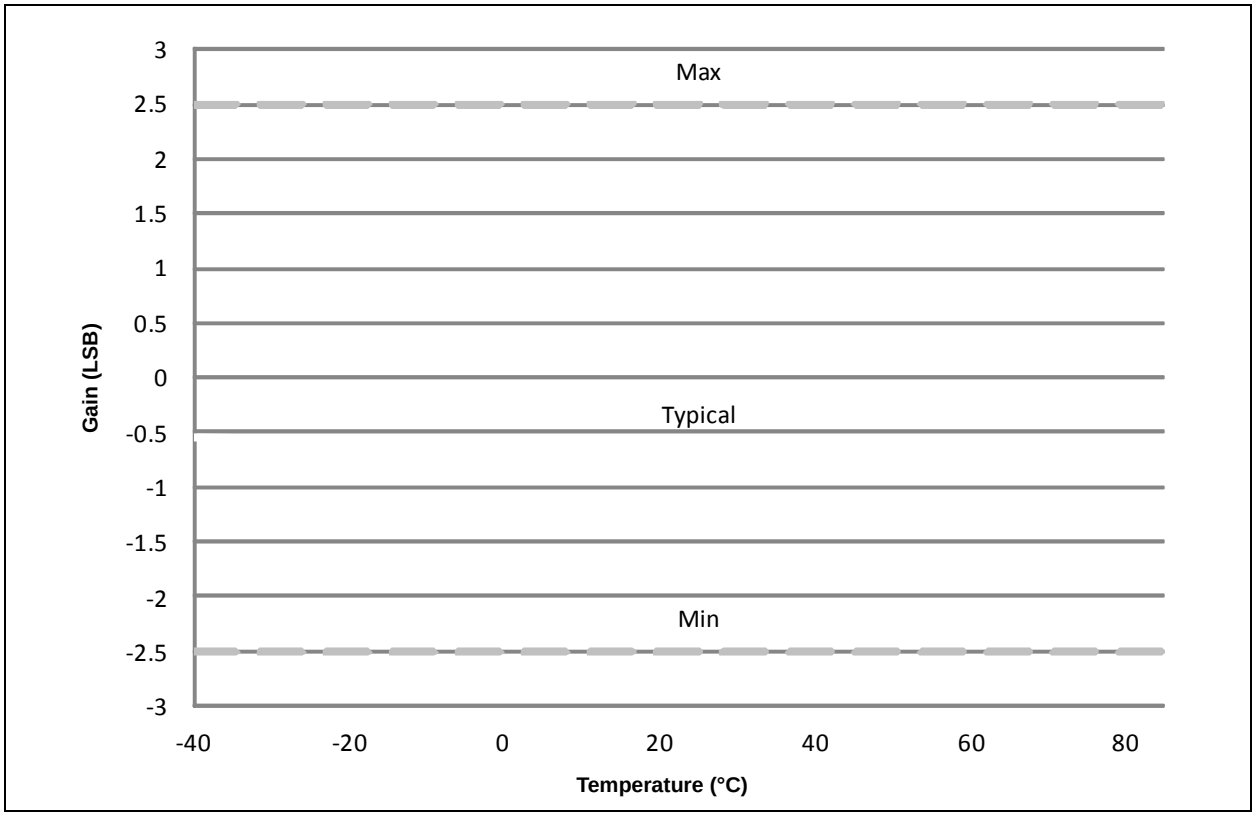


FIGURE 38-48: 10-BIT DAC GAIN vs. TEMPERATURE



NOTES: