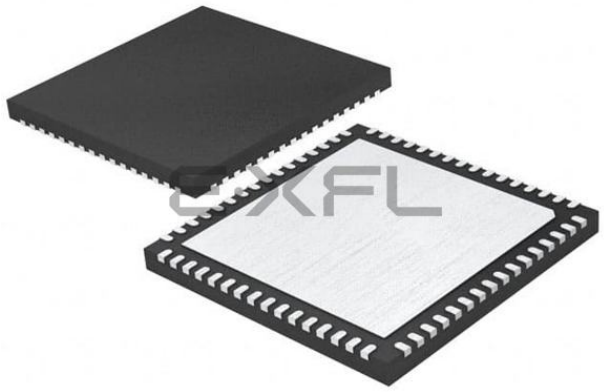

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Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
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Data Converters	A/D 29x12b, 2x16b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
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Supplier Device Package	64-VQFN (9x9)
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TABLE 4-8: OUTPUT COMPARE REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
OC1CON1	0190	—	—	OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0	ENFLT2	ENFLT1	ENFLT0	OCFLT2	OCFLT1	OCFLT0	TRIGMODE	OCM2	OCM1	OCM0	0000
OC1CON2	0192	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	DCB1	DCB0	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000C
OC1RS	0194	Output Compare 1 Secondary Register																0000
OC1R	0196	Output Compare 1 Register																0000
OC1TMR	0198	Timer Value 1 Register																xxxx
OC2CON1	019A	—	—	OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0	ENFLT2	ENFLT1	ENFLT0	OCFLT2	OCFLT1	OCFLT0	TRIGMODE	OCM2	OCM1	OCM0	0000
OC2CON2	019C	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	DCB1	DCB0	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000C
OC2RS	019E	Output Compare 2 Secondary Register																0000
OC2R	01A0	Output Compare 2 Register																0000
OC2TMR	01A2	Timer Value 2 Register																xxxx
OC3CON1	01A4	—	—	OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0	ENFLT2	ENFLT1	ENFLT0	OCFLT2	OCFLT1	OCFLT0	TRIGMODE	OCM2	OCM1	OCM0	0000
OC3CON2	01A6	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	DCB1	DCB0	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000C
OC3RS	01A8	Output Compare 3 Secondary Register																0000
OC3R	01AA	Output Compare 3 Register																0000
OC3TMR	01AC	Timer Value 3 Register																xxxx
OC4CON1	01AE	—	—	OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0	ENFLT2	ENFLT1	ENFLT0	OCFLT2	OCFLT1	OCFLT0	TRIGMODE	OCM2	OCM1	OCM0	0000
OC4CON2	01B0	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	DCB1	DCB0	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000C
OC4RS	01B2	Output Compare 4 Secondary Register																0000
OC4R	01B4	Output Compare 4 Register																0000
OC4TMR	01B6	Timer Value 4 Register																xxxx
OC5CON1	01B8	—	—	OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0	ENFLT2	ENFLT1	ENFLT0	OCFLT1	OCFLT1	OCFLT0	TRIGMODE	OCM2	OCM1	OCM0	0000
OC5CON2	01BA	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	DCB1	DCB0	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000C
OC5RS	01BC	Output Compare 5 Secondary Register																0000
OC5R	01BE	Output Compare 5 Register																0000
OC5TMR	01C0	Timer Value 5 Register																xxxx
OC6CON1	01C2	—	—	OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0	ENFLT2	ENFLT1	ENFLT0	OCFLT2	OCFLT1	OCFLT0	TRIGMODE	OCM2	OCM1	OCM0	0000
OC6CON2	01C4	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	DCB1	DCB0	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000C
OC6RS	01C6	Output Compare 6 Secondary Register																0000
OC6R	01C8	Output Compare 6 Register																0000
OC6TMR	01CA	Timer Value 6 Register																xxxx

Legend: — = unimplemented, read as '0'; x = unknown value on Reset. Reset values are shown in hexadecimal.

TABLE 4-25: 12-BIT PIPELINE A/D CONVERTER REGISTER MAP (CONTINUED)

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
ADTBL0	0300	UCTMU	DIFF	—	—	—	—	—	—	—	ADCH6	ADCH5	ADCH4	ADCH3	ADCH2	ADCH1	ADCH0	0000
ADTBL1	0302	UCTMU	DIFF	—	—	—	—	—	—	—	ADCH6	ADCH5	ADCH4	ADCH3	ADCH2	ADCH1	ADCH0	0000
ADTBL2	0304	UCTMU	DIFF	—	—	—	—	—	—	—	ADCH6	ADCH5	ADCH4	ADCH3	ADCH2	ADCH1	ADCH0	0000
ADTBL3	0306	UCTMU	DIFF	—	—	—	—	—	—	—	ADCH6	ADCH5	ADCH4	ADCH3	ADCH2	ADCH1	ADCH0	0000
ADTBL4	0308	UCTMU	DIFF	—	—	—	—	—	—	—	ADCH6	ADCH5	ADCH4	ADCH3	ADCH2	ADCH1	ADCH0	0000
ADTBL5	030A	UCTMU	DIFF	—	—	—	—	—	—	—	ADCH6	ADCH5	ADCH4	ADCH3	ADCH2	ADCH1	ADCH0	0000
ADTBL6	030C	UCTMU	DIFF	—	—	—	—	—	—	—	ADCH6	ADCH5	ADCH4	ADCH3	ADCH2	ADCH1	ADCH0	0000
ADTBL7	030E	UCTMU	DIFF	—	—	—	—	—	—	—	ADCH6	ADCH5	ADCH4	ADCH3	ADCH2	ADCH1	ADCH0	0000
ADTBL8	0310	UCTMU	DIFF	—	—	—	—	—	—	—	ADCH6	ADCH5	ADCH4	ADCH3	ADCH2	ADCH1	ADCH0	0000
ADTBL9	0312	UCTMU	DIFF	—	—	—	—	—	—	—	ADCH6	ADCH5	ADCH4	ADCH3	ADCH2	ADCH1	ADCH0	0000
ADTBL10	0314	UCTMU	DIFF	—	—	—	—	—	—	—	ADCH6	ADCH5	ADCH4	ADCH3	ADCH2	ADCH1	ADCH0	0000
ADTBL11	0316	UCTMU	DIFF	—	—	—	—	—	—	—	ADCH6	ADCH5	ADCH4	ADCH3	ADCH2	ADCH1	ADCH0	0000
ADTBL12	0318	UCTMU	DIFF	—	—	—	—	—	—	—	ADCH6	ADCH5	ADCH4	ADCH3	ADCH2	ADCH1	ADCH0	0000
ADTBL13	031A	UCTMU	DIFF	—	—	—	—	—	—	—	ADCH6	ADCH5	ADCH4	ADCH3	ADCH2	ADCH1	ADCH0	0000
ADTBL14	031C	UCTMU	DIFF	—	—	—	—	—	—	—	ADCH6	ADCH5	ADCH4	ADCH3	ADCH2	ADCH1	ADCH0	0000
ADTBL15	031E	UCTMU	DIFF	—	—	—	—	—	—	—	ADCH6	ADCH5	ADCH4	ADCH3	ADCH2	ADCH1	ADCH0	0000
ADTBL16	0320	UCTMU	DIFF	—	—	—	—	—	—	—	ADCH6	ADCH5	ADCH4	ADCH3	ADCH2	ADCH1	ADCH0	0000
ADTBL17	0322	UCTMU	DIFF	—	—	—	—	—	—	—	ADCH6	ADCH5	ADCH4	ADCH3	ADCH2	ADCH1	ADCH0	0000
ADTBL18	0324	UCTMU	DIFF	—	—	—	—	—	—	—	ADCH6	ADCH5	ADCH4	ADCH3	ADCH2	ADCH1	ADCH0	0000
ADTBL19	0326	UCTMU	DIFF	—	—	—	—	—	—	—	ADCH6	ADCH5	ADCH4	ADCH3	ADCH2	ADCH1	ADCH0	0000
ADTBL20	0328	UCTMU	DIFF	—	—	—	—	—	—	—	ADCH6	ADCH5	ADCH4	ADCH3	ADCH2	ADCH1	ADCH0	0000
ADTBL21	032A	UCTMU	DIFF	—	—	—	—	—	—	—	ADCH6	ADCH5	ADCH4	ADCH3	ADCH2	ADCH1	ADCH0	0000
ADTBL22	032C	UCTMU	DIFF	—	—	—	—	—	—	—	ADCH6	ADCH5	ADCH4	ADCH3	ADCH2	ADCH1	ADCH0	0000
ADTBL23	032E	UCTMU	DIFF	—	—	—	—	—	—	—	ADCH6	ADCH5	ADCH4	ADCH3	ADCH2	ADCH1	ADCH0	0000
ADTBL24	0330	UCTMU	DIFF	—	—	—	—	—	—	—	ADCH6	ADCH5	ADCH4	ADCH3	ADCH2	ADCH1	ADCH0	0000
ADTBL25	0332	UCTMU	DIFF	—	—	—	—	—	—	—	ADCH6	ADCH5	ADCH4	ADCH3	ADCH2	ADCH1	ADCH0	0000
ADTBL26	0334	UCTMU	DIFF	—	—	—	—	—	—	—	ADCH6	ADCH5	ADCH4	ADCH3	ADCH2	ADCH1	ADCH0	0000
ADTBL27	0336	UCTMU	DIFF	—	—	—	—	—	—	—	ADCH6	ADCH5	ADCH4	ADCH3	ADCH2	ADCH1	ADCH0	0000
ADTBL28	0338	UCTMU	DIFF	—	—	—	—	—	—	—	ADCH6	ADCH5	ADCH4	ADCH3	ADCH2	ADCH1	ADCH0	0000
ADTBL29	033A	UCTMU	DIFF	—	—	—	—	—	—	—	ADCH6	ADCH5	ADCH4	ADCH3	ADCH2	ADCH1	ADCH0	0000
ADTBL30	033C	UCTMU	DIFF	—	—	—	—	—	—	—	ADCH6	ADCH5	ADCH4	ADCH3	ADCH2	ADCH1	ADCH0	0000
ADTBL31	033E	UCTMU	DIFF	—	—	—	—	—	—	—	ADCH6	ADCH5	ADCH4	ADCH3	ADCH2	ADCH1	ADCH0	0000

Legend: — = unimplemented, read as '0'; r = reserved, do not modify. Reset values are shown in hexadecimal.

TABLE 4-29: PARALLEL MASTER/SLAVE PORT REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMCON1	0600	PMPEN	—	PSIDL	ADRMUX1	ADRMUX0	—	MODE1	MODE0	CSF1	CSF0	ALP	ALMODE	—	BUSKEEP	IRQM1	IRQM0	0000
PMCON2	0602	BUSY	—	ERROR	TIMEOUT	—	—	—	—	RADDR23	RADDR22	RADDR21	RADDR20	RADDR19	RADDR18	RADDR17	RADDR16	0000
PMCON3	0604	PTWREN	PTRDEN	PTBE1EN	PTBE0EN	—	AWAITM1	AWAITM0	AWAITE	—	PTEN22	PTEN21	PTEN20	PTEN19	PTEN18	PTEN17	PTEN16	0000
PMCON4	0606	PTEN<15:0>																0000
PMCS1CF	0608	CSDIS	CSP	CSPTEN	BEP	—	WRSP	RDSP	SM	ACKP	PTSZ1	PTSZ0	—	—	—	—	—	0000
PMCS1BS	060A	BASE<23:15>									—	—	—	—	—	—	—	0200
PMCS1MD	060C	ACKM1	ACKM0	AMWAIT2	AMWAIT1	AMWAIT0	—	—	—	DWAITB1	DWAITB0	DWAITM3	DWAITM2	DWAITM1	DWAITM0	DWAITE1	DWAITE0	0000
PMCS2CF	060E	CSDIS	CSP	CSPTEN	BEP	—	WRSP	RDSP	SM	ACKP	PTSZ1	PTSZ0	—	—	—	—	—	0000
PMCS2BS	0610	BASE<23:15>									—	—	—	—	—	—	—	0600
PMCS2MD	0612	ACKM1	ACKM0	AMWAIT2	AMWAIT1	AMWAIT0	—	—	—	DWAITB1	DWAITB0	DWAITM3	DWAITM2	DWAITM1	DWAITM0	DWAITE1	DWAITE0	0000
PMDOUT1	0614	Data Out Register 1<15:8>								Data Out Register 1<7:0>								xxxx
PMDOUT2	0616	Data Out Register 2<15:8>								Data Out Register 2<7:0>								xxxx
PMDIN1	0618	Data In Register 1<15:8>								Data In Register 1<7:0>								xxxx
PMDIN2	061A	Data In Register 2<15:8>								Data In Register 2<7:0>								xxxx
PMSTAT	061C	IBF	IBOV	—	—	IB3F	IB2F	IB1F	IB0F	OBE	OBUF	—	—	OB3E	OB2E	OB1E	OB0E	008F

Legend: — = unimplemented, read as '0'; x = unknown value on Reset. Reset values are shown in hexadecimal.

TABLE 4-30: REAL-TIME CLOCK AND CALENDAR (RTCC) REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
ALRMVAL	0620	Alarm Value Register Window Based on ALRMPTR<1:0>																xxxx
ALCFGRPT	0622	ALRMEN	CHIME	AMASK3	AMASK2	AMASK1	AMASK0	ALRMPTR1	ALRMPTR0	ARPT7	ARPT6	ARPT5	ARPT4	ARPT3	ARPT2	ARPT1	ARPT0	0000
RTCVAL	0624	RTCC Value Register Window Based on RTCPTR<1:0>																xxxx
RCFGCAL	0626	RTCEN	—	RTCWREN	RTCSYNC	HALFSEC	RTCOE	RTCPTR1	RTCPTR0	CAL7	CAL6	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0	**Note 1**
RTCPWC	0628	PWCEN	PWCPOL	PWCPRE	PWSPRE	RTCLK1	RTCLK0	RTCOUT1	RTCOUT0	—	—	—	—	—	—	—	—	**Note 1**

Legend: — = unimplemented, read as '0'; x = unknown value on Reset. Reset values are shown in hexadecimal.
Note 1: The status of the RCFGCAL and RTCPWR registers on POR is '0000', and on other Resets, it is unchanged

TABLE 4-31: DATA SIGNAL MODULATOR (DSM) REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
MDCON	062A	MDEN	—	MDSIDL	—	—	—	—	—	—	MDOE	MDSLR	MDOPOL	—	—	—	MDBIT	0020
MDSRC	062C	—	—	—	—	—	—	—	—	SODIS	—	—	—	MS3	MS2	MS1	MS0	000x
MDCAR	062E	CHODIS	CHPOL	CHSYNC	—	CH3	CH2	CH1	CH0	CLODIS	CLPOL	CLSYNC	—	CL3	CL2	CL1	CL0	0000

Legend: — = unimplemented, read as '0'; x = unknown value on Reset. Reset values are shown in hexadecimal.

5.1 Summary of DMA Operations

The DMA controller is capable of moving data between addresses according to a number of different parameters. Each of these parameters can be independently configured for any transaction. In addition, any or all of the DMA channels can independently perform a different transaction at the same time. Transactions are classified by these parameters:

- Source and destination (SFRs and data RAM)
- Data size (byte or word)
- Trigger source
- Transfer mode (One-Shot, Repeated or Continuous)
- Addressing modes (Fixed Address or Address Blocks, with or without Address Increment/ Decrement)

In addition, the DMA controller provides channel priority arbitration for all channels.

5.1.1 SOURCE AND DESTINATION

Using the DMA controller, data may be moved between any two addresses in the Data Space. The SFR space (0000h to 07FFh), or the data RAM space (0800h to FFFFh) can serve as either the source or the destination. Data can be moved between these areas in either direction, or between addresses in either area. The four different combinations are shown in Figure 5-2.

If it is necessary to protect areas of data RAM, the DMA controller allows the user to set upper and lower address boundaries for operations in the Data Space above the SFR space. The boundaries are set by the DMAH and DMAL Limit registers. If a DMA channel attempts an operation outside of the address boundaries, the transaction is terminated and an interrupt is generated.

5.1.2 DATA SIZE

The DMA controller can handle both 8-bit and 16-bit transactions. Size is user-selectable using the SIZE bit (DMACHn<1>). By default, each channel is configured for word-size transactions. When byte-size transactions are chosen, the LSb of the source and/or destination address determines if the data represents the upper or lower byte of the data RAM location.

5.1.3 TRIGGER SOURCE

The DMA controller can use 63 of the device's interrupt sources to initiate a transaction. The DMA trigger sources occur in reverse order of their natural interrupt priority and are shown in Table 5-1.

These sources cannot be used as DMA triggers:

- Input Capture 8 and 9
- Output Compare 7, 8 and 9
- USB

Since the source and destination addresses for any transaction can be programmed independently of the trigger source, the DMA controller can use any trigger to perform an operation on any peripheral. This also allows DMA channels to be cascaded to perform more complex transfer operations.

5.1.4 TRANSFER MODE

The DMA controller supports four types of data transfers, based on the volume of data to be moved for each trigger.

- One-Shot: A single transaction occurs for each trigger.
- Continuous: A series of back-to-back transactions occur for each trigger. The number of transactions is determined by the DMACNTn Transaction Counter register.
- Repeated One-Shot: A single transaction is performed repeatedly, once per trigger, until the DMA channel is disabled.
- Repeated Continuous: A series of transactions are performed repeatedly, one cycle per trigger, until the DMA channel is disabled.

All transfer modes allow the option to have the source and destination addresses, and counter value automatically reloaded after the completion of a transaction. Repeated mode transfers do this automatically.

5.1.5 ADDRESSING MODES

The DMA controller also supports transfers between single addresses or address ranges. The four basic options are:

- Fixed-to-Fixed: Between two constant addresses
- Fixed-to-Block: From a constant source address to a range of destination addresses
- Block-to-Fixed: From a range of source addresses to a single, constant destination address
- Block-to-Block: From a range to source addresses to a range of destination addresses

The option to select auto-increment or auto-decrement of source and/or destination addresses is available for Block Addressing modes.

TABLE 8-2: IMPLEMENTED INTERRUPT VECTORS (CONTINUED)

Interrupt Source	Vector Number	IVT Address	AIVT Address	Interrupt Bit Locations		
				Flag	Enable	Priority
Enhanced Parallel Master Port (EPMP)	45	00006Eh	00016Eh	IFS2<13>	IEC2<13>	IPC11<6:4>
Real-Time Clock and Calendar (RTCC)	62	000090h	000190h	IFS3<14>	IEC3<14>	IPC15<10:8>
SPI1 Error	9	000026h	000126h	IFS0<9>	IEC0<9>	IPC2<6:4>
SPI1 Event	10	000028h	000128h	IFS0<10>	IEC0<10>	IPC2<10:8>
SPI2 Error	32	000054h	000154h	IFS2<0>	IEC2<0>	IPC8<2:0>
SPI2 Event	33	000056h	000156h	IFS2<1>	IEC2<1>	IPC8<6:4>
Timer1	3	00001Ah	00011Ah	IFS0<3>	IEC0<3>	IPC0<14:12>
Timer2	7	000022h	000122h	IFS0<7>	IEC0<7>	IPC1<14:12>
Timer3	8	000024h	000124h	IFS0<8>	IEC0<8>	IPC2<2:0>
Timer4	27	00004Ah	00014Ah	IFS1<11>	IEC1<11>	IPC6<14:12>
Timer5	28	00004Ch	00014Ch	IFS1<12>	IEC1<12>	IPC7<2:0>
UART1 Error	65	000096h	000196h	IFS4<1>	IEC4<1>	IPC16<6:4>
UART1 Receiver	11	00002Ah	00012Ah	IFS0<11>	IEC0<11>	IPC2<14:12>
UART1 Transmitter	12	00002Ch	00012Ch	IFS0<12>	IEC0<12>	IPC3<2:0>
UART2 Error	66	000098h	000198h	IFS4<2>	IEC4<2>	IPC16<10:8>
UART2 Receiver	30	000050h	000150h	IFS1<14>	IEC1<14>	IPC7<10:8>
UART2 Transmitter	31	000052h	000152h	IFS1<15>	IEC1<15>	IPC7<14:12>
UART3 Error	81	0000B6h	0001B6h	IFS5<1>	IEC5<1>	IPC20<6:4>
UART3 Receiver	82	0000B8h	0001B8h	IFS5<2>	IEC5<2>	IPC20<10:8>
UART3 Transmitter	83	0000BAh	0001BAh	IFS5<3>	IEC5<3>	IPC20<14:12>
UART4 Error	87	0000C2h	0001C2h	IFS5<7>	IEC5<7>	IPC21<14:12>
UART4 Receiver	88	0000C4h	0001C4h	IFS5<8>	IEC5<8>	IPC22<2:0>
UART4 Transmitter	89	0000C6h	0001C6h	IFS5<9>	IEC5<9>	IPC22<6:4>
USB	86	0000C0h	0001C0h	IFS5<6>	IEC5<6>	IPC21<10:8>

REGISTER 11-6: ANSF: PORTF ANALOG FUNCTION SELECTION REGISTER

U-0	U-0	R/W-1	U-0	U-0	U-0	U-0	R/W-1
—	—	ANSF13(1)	—	—	—	—	ANSF8(1)
bit 15							bit 8

R/W-1	U-0	R/W-1	R/W-1	R/W-1	R/W-1	U-0	R/W-1
ANSF7	—	ANSF<5:2>(1)				—	ANSF0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **ANSF13:** Analog Function Selection bit(1)
1 = Pin is configured in Analog mode; I/O port read is disabled
0 = Pin is configured in Digital mode; I/O port read is enabled

bit 12-9 **Unimplemented:** Read as '0'

bit 8-7 **ANSF<8:7>:** Analog Function Selection bits(1)
1 = Pin is configured in Analog mode; I/O port read is disabled
0 = Pin is configured in Digital mode; I/O port read is enabled

bit 6 **Unimplemented:** Read as '0'

bit 5-2 **ANSF<5:2>:** Analog Function Selection bits(1)
1 = Pin is configured in Analog mode; I/O port read is disabled
0 = Pin is configured in Digital mode; I/O port read is enabled

bit 1 **Unimplemented:** Read as '0'

bit 0 **ANSF0:** Analog Function Selection bit
1 = Pin is configured in Analog mode; I/O port read is disabled
0 = Pin is configured in Digital mode; I/O port read is enabled

Note 1: The ANSF<13,8,2> bits are not available in 64-pin devices.

REGISTER 11-40: RPOR12: PERIPHERAL PIN SELECT OUTPUT REGISTER 12

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP25R5	RP25R4	RP25R3	RP25R2	RP25R1	RP25R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP24R5	RP24R4	RP24R3	RP24R2	RP24R1	RP24R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RP25R<5:0>:** RP25 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP25 (see Table 11-4 for peripheral function numbers).

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP24R<5:0>:** RP24 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP24 (see Table 11-4 for peripheral function numbers).

REGISTER 11-41: RPOR13: PERIPHERAL PIN SELECT OUTPUT REGISTER 13

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP27R5	RP27R4	RP27R3	RP27R2	RP27R1	RP27R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP26R5	RP26R4	RP26R3	RP26R2	RP26R1	RP26R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RP27R<5:0>:** RP27 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP27 (see Table 11-4 for peripheral function numbers).

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP26R<5:0>:** RP26 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP26 (see Table 11-4 for peripheral function numbers).

REGISTER 13-1: TxCON: TIMER2 AND TIMER4 CONTROL REGISTER(1) (CONTINUED)

bit 3 **T32:** 32-Bit Timer Mode Select bit(3)
1 = Timerx and Timery form a single 32-bit timer
0 = Timerx and Timery act as two 16-bit timers
In 32-bit mode, T3CON control bits do not affect 32-bit timer operation.

bit 2 **Unimplemented:** Read as '0'

bit 1 **TCS:** Timerx Clock Source Select bit(2)
1 = Timer source is selected by TIECS<1:0>
0 = Internal clock (FOSC/2)

bit 0 **Unimplemented:** Read as '0'

Note 1: Changing the value of TxCON while the timer is running (TON = 1) causes the timer prescale counter to reset and is not recommended.

2: If TCS = 1 and TIECS<1:0> = x1, the selected external timer input (TMRCK or TxCK) must be configured to an available RPn/RPIn pin. For more information, see **Section 11.4 "Peripheral Pin Select (PPS)"**.

3: In T4CON, the T45 bit is implemented instead of T32 to select 32-bit mode. In 32-bit mode, the T3CON or T5CON control bits do not affect 32-bit timer operation.

REGISTER 14-1: ICxCON1: INPUT CAPTURE x CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
—	—	ICSIDL	ICTSEL2	ICTSEL1	ICTSEL0	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R-0, HSC	R-0, HSC	R/W-0	R/W-0	R/W-0
—	ICI1	ICI0	ICOV	ICBNE	ICM2(1)	ICM1(1)	ICM0(1)
bit 7							bit 0

Legend:	HSC = Hardware Settable/Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **ICSIDL:** Input Capture x Module Stop in Idle Control bit
1 = Input capture module halts in CPU Idle mode
0 = Input capture module continues to operate in CPU Idle mode

bit 12-10 **ICTSEL<2:0>:** Input Capture x Timer Select bits
111 = System clock (FOSC/2)
110 = Reserved
101 = Reserved
100 = Timer1
011 = Timer5
010 = Timer4
001 = Timer2
000 = Timer3

bit 9-7 **Unimplemented:** Read as '0'

bit 6-5 **ICI<1:0>:** Select Number of Captures per Interrupt bits
11 = Interrupt on every fourth capture event
10 = Interrupt on every third capture event
01 = Interrupt on every second capture event
00 = Interrupt on every capture event

bit 4 **ICOV:** Input Capture x Overflow Status Flag bit (read-only)
1 = Input capture overflow has occurred
0 = No input capture overflow has occurred

bit 3 **ICBNE:** Input Capture x Buffer Empty Status bit (read-only)
1 = Input capture buffer is not empty, at least one more capture value can be read
0 = Input capture buffer is empty

bit 2-0 **ICM<2:0>:** Input Capture x Mode Select bits(1)
111 = Interrupt mode: Input capture functions as an interrupt pin only when the device is in Sleep or Idle mode (rising edge detect only, all other control bits are not applicable)
110 = Unused (module is disabled)
101 = Prescaler Capture mode: Capture on every 16th rising edge
100 = Prescaler Capture mode: Capture on every 4th rising edge
011 = Simple Capture mode: Capture on every rising edge
010 = Simple Capture mode: Capture on every falling edge
001 = Edge Detect Capture mode: Capture on every edge (rising and falling); ICI<1:0> bits do not control interrupt generation for this mode
000 = Input Capture x module is turned off

Note 1: The ICx input must also be configured to an available RPn/RPIn pin. For more information, see **Section 11.4 "Peripheral Pin Select (PPS)"**.

BDs have a fixed relationship to a particular endpoint, depending on the buffering configuration. Table 19-2 provides the mapping of BDs to endpoints. This relationship also means that gaps may occur in the BDT if endpoints are not enabled contiguously. This, theoretically, means that the BDs for disabled endpoints could be used as buffer space. In practice, users should avoid using such spaces in the BDT unless a method of validating BD addresses is implemented.

19.2.1 BUFFER OWNERSHIP

Because the buffers and their BDs are shared between the CPU and the USB module, a simple semaphore mechanism is used to distinguish which is allowed to update the BD and associated buffers in memory. This is done by using the UOWN bit as a semaphore to distinguish which is allowed to update the BD and associated buffers in memory. UOWN is the only bit that is shared between the two configurations of BDnSTAT.

When UOWN is clear, the BD entry is “owned” by the microcontroller core. When the UOWN bit is set, the BD entry and the buffer memory are “owned” by the USB peripheral. The core should not modify the BD or its corresponding data buffer during this time. Note that the microcontroller core can still read BDnSTAT while the SIE owns the buffer and vice versa.

The Buffer Descriptors have a different meaning based on the source of the register update. Register 19-1 and Register 19-2 show the differences in BDnSTAT depending on its current “ownership”.

When UOWN is set, the user can no longer depend on the values that were written to the BDs. From this point, the USB module updates the BDs as necessary, overwriting the original BD values. The BDnSTAT register is updated by the SIE with the token PID and the transfer count is updated.

19.2.2 DMA INTERFACE

The USB OTG module uses a dedicated DMA to access both the BDT and the endpoint data buffers. Since part of the address space of the DMA is dedicated to the Buffer Descriptors, a portion of the memory connected to the DMA must comprise a contiguous address space, properly mapped for the access by the module.

TABLE 19-2: ASSIGNMENT OF BUFFER DESCRIPTORS FOR THE DIFFERENT BUFFERING MODES

Endpoint	BDs Assigned to Endpoint							
	Mode 0 (No Ping-Pong)		Mode 1 (Ping-Pong on EP0 OUT)		Mode 2 (Ping-Pong on All EPs)		Mode 3 (Ping-Pong on All Other EPs, Except EP0)	
	Out	In	Out	In	Out	In	Out	In
0	0	1	0 (E), 1 (O)	2	0 (E), 1 (O)	2 (E), 3 (O)	0	1
1	2	3	3	4	4 (E), 5 (O)	6 (E), 7 (O)	2 (E), 3 (O)	4 (E), 5 (O)
2	4	5	5	6	8 (E), 9 (O)	10 (E), 11 (O)	6 (E), 7 (O)	8 (E), 9 (O)
3	6	7	7	8	12 (E), 13 (O)	14 (E), 15 (O)	10 (E), 11 (O)	12 (E), 13 (O)
4	8	9	9	10	16 (E), 17 (O)	18 (E), 19 (O)	14 (E), 15 (O)	16 (E), 17 (O)
5	10	11	11	12	20 (E), 21 (O)	22 (E), 23 (O)	18 (E), 19 (O)	20 (E), 21 (O)
6	12	13	13	14	24 (E), 25 (O)	26 (E), 27 (O)	22 (E), 23 (O)	24 (E), 25 (O)
7	14	15	15	16	28 (E), 29 (O)	30 (E), 31 (O)	26 (E), 27 (O)	28 (E), 29 (O)
8	16	17	17	18	32 (E), 33 (O)	34 (E), 35 (O)	30 (E), 31 (O)	32 (E), 33 (O)
9	18	19	19	20	36 (E), 37 (O)	38 (E), 39 (O)	34 (E), 35 (O)	36 (E), 37 (O)
10	20	21	21	22	40 (E), 41 (O)	42 (E), 43 (O)	38 (E), 39 (O)	40 (E), 41 (O)
11	22	23	23	24	44 (E), 45 (O)	46 (E), 47 (O)	42 (E), 43 (O)	44 (E), 45 (O)
12	24	25	25	26	48 (E), 49 (O)	50 (E), 51 (O)	46 (E), 47 (O)	48 (E), 49 (O)
13	26	27	27	28	52 (E), 53 (O)	54 (E), 55 (O)	50 (E), 51 (O)	52 (E), 53 (O)
14	28	29	29	30	56 (E), 57 (O)	58 (E), 59 (O)	54 (E), 55 (O)	56 (E), 57 (O)
15	30	31	31	32	60 (E), 61 (O)	62 (E), 63 (O)	58 (E), 59 (O)	60 (E), 61 (O)

Legend: (E) = Even transaction buffer, (O) = Odd transaction buffer

REGISTER 22-3: LCDPS: LCD PHASE REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
WFT	BIASMD	LCDA	WA	LP3	LP2	LP1	LP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **WFT:** Waveform Type Select bit
1 = Type-B waveform (phase changes on each frame boundary)
0 = Type-A waveform (phase changes within each common type)

bit 6 **BIASMD:** Bias Mode Select bit
When LMUX<2:0> = 000 or 011 through 111:
0 = Static Bias mode (do not set this bit to '1')
When LMUX<2:0> = 001 or 010:
1 = 1/2 Bias mode
0 = 1/3 Bias mode

bit 5 **LCDA:** LCD Active Status bit
1 = LCD driver module is active
0 = LCD driver module is inactive

bit 4 **WA:** LCD Write Allow Status bit
1 = Write into the LCDDATAx registers is allowed
0 = Write into the LCDDATAx registers is not allowed

bit 3-0 **LP<3:0>:** LCD Prescaler Select bits
1111 = 1:16
1110 = 1:15
1101 = 1:14
1100 = 1:13
1011 = 1:12
1010 = 1:11
1001 = 1:10
1000 = 1:9
0111 = 1:8
0110 = 1:7
0101 = 1:6
0100 = 1:5
0011 = 1:4
0010 = 1:3
0001 = 1:2
0000 = 1:1

23.3.2 RTCVAL REGISTER MAPPINGS

REGISTER 23-4: YEAR: YEAR VALUE REGISTER(1)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
YRTEN3	YRTEN2	YRTEN2	YRTEN1	YRONE3	YRONE2	YRONE1	YRONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-4 **YRTEN<3:0>:** Binary Coded Decimal Value of Year's Tens Digit bits
Contains a value from 0 to 9.

bit 3-0 **YRONE<3:0>:** Binary Coded Decimal Value of Year's Ones Digit bits
Contains a value from 0 to 9.

Note 1: A write to the YEAR register is only allowed when RTCWREN = 1.

REGISTER 23-5: MTHDY: MONTH AND DAY VALUE REGISTER(1)

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0
bit 15							bit 8

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	DAYTEN1	DAYTEN0	DAYONE3	DAYONE2	DAYONE1	DAYONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12 **MTHTEN0:** Binary Coded Decimal Value of Month's Tens Digit bit
Contains a value of '0' or '1'.

bit 11-8 **MTHONE<3:0>:** Binary Coded Decimal Value of Month's Ones Digit bits
Contains a value from 0 to 9.

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **DAYTEN<1:0>:** Binary Coded Decimal Value of Day's Tens Digit bits
Contains a value from 0 to 3.

bit 3-0 **DAYONE<3:0>:** Binary Coded Decimal Value of Day's Ones Digit bits
Contains a value from 0 to 9.

Note 1: A write to this register is only allowed when RTCWREN = 1.

30.0 TRIPLE COMPARATOR MODULE

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"Scalable Comparator Module"** (DS39734) which is available from the Microchip web site (www.microchip.com). The information in this data sheet supersedes the information in the FRM.

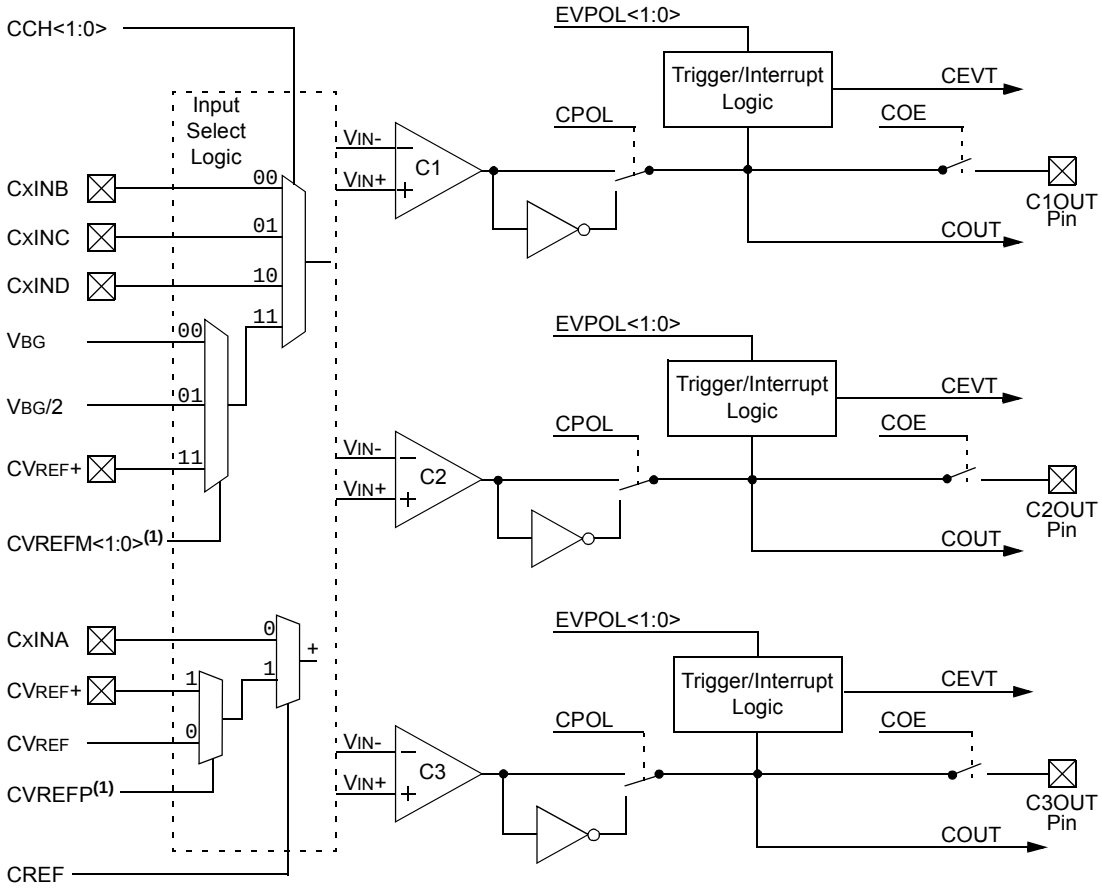
The triple comparator module provides three dual input comparators. The inputs to the comparator can be configured to use any one of five external analog inputs (CxINA, CxINB, CxINC, CxIND and VREF+) and a voltage reference input from one of the internal band gap references or the comparator voltage reference generator (VBG, VBG/2, VBG/6 and CVREF).

The comparator outputs may be directly connected to the CxOUT pins. When the respective COE equals '1', the I/O pad logic makes the unsynchronized output of the comparator available on the pin.

A simplified block diagram of the module in shown in Figure 30-1. Diagrams of the possible individual comparator configurations are shown in Figure 30-2.

Each comparator has its own control register, CMxCON (Register 30-1), for enabling and configuring its operation. The output and event status of all three comparators is provided in the CMSTAT register (Register 30-2).

FIGURE 30-1: TRIPLE COMPARATOR MODULE BLOCK DIAGRAM



Note 1: Refer to the CVRCON register (Register 31-1) for bit details.

REGISTER 30-1: CMxCON: COMPARATOR x CONTROL REGISTERS (COMPARATORS 1 THROUGH 3)

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0, HS	R-0, HSC
CON	COE	CPOL	—	—	—	CEVT	COUT
bit 15							bit 8

R/W-0	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0
EVPOL1(1)	EVPOL0(1)	—	CREF	—	—	CCH1	CCH0
bit 7							bit 0

Legend:	HS = Hardware Settable bit	HSC = Hardware Settable/Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CON:** Comparator Enable bit
1 = Comparator is enabled
0 = Comparator is disabled

bit 14 **COE:** Comparator Output Enable bit
1 = Comparator output is present on the CxOUT pin
0 = Comparator output is internal only

bit 13 **CPOL:** Comparator Output Polarity Select bit
1 = Comparator output is inverted
0 = Comparator output is not inverted

bit 12-10 **Unimplemented:** Read as '0'

bit 9 **CEVT:** Comparator Event bit
1 = Comparator event that is defined by EVPOL<1:0> has occurred; subsequent triggers and interrupts are disabled until the bit is cleared
0 = Comparator event has not occurred

bit 8 **COUT:** Comparator Output bit
When CPOL = 0:
1 = VIN+ > VIN-
0 = VIN+ < VIN-
When CPOL = 1:
1 = VIN+ < VIN-
0 = VIN+ > VIN-

bit 7-6 **EVPOL<1:0>:** Trigger/Event/Interrupt Polarity Select bits(1)
11 = Trigger/event/interrupt is generated on any change of the comparator output (while CEVT = 0)
10 = Trigger/event/interrupt is generated on the high-to-low transition of the comparator output
01 = Trigger/event/interrupt is generated on the low-to-high transition of the comparator output
00 = Trigger/event/interrupt generation is disabled

bit 5 **Unimplemented:** Read as '0'

bit 4 **CREF:** Comparator Reference Select bits (non-inverting input)
1 = Non-inverting input connects to the internal CVREF voltage
0 = Non-inverting input connects to the CxINA pin

bit 3-2 **Unimplemented:** Read as '0'

Note 1: If the EVPOL<1:0> bits are set to a value other than '00', the first interrupt generated will occur on any transition of COUT. Subsequent interrupts will occur based on the EVPOLx bits setting.

NOTES:

32.0 CHARGE TIME MEASUREMENT UNIT (CTMU)

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the Charge Measurement Unit, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"Charge Time Measurement Unit (CTMU) and CTMU Operation with Threshold Detect"** (DS30009743) which is available from the Microchip web site (www.microchip.com). The information in this data sheet supersedes the information in the FRM.

The Charge Time Measurement Unit (CTMU) is a flexible analog module that provides charge measurement, accurate differential time measurement between pulse sources and asynchronous pulse generation. Its key features include:

- Thirteen External Edge Input Trigger Sources
- Polarity Control for each Edge Source
- Control of Edge Sequence
- Control of Response to Edge Levels or Edge Transitions
- Time Measurement Resolution of One Nanosecond
- Accurate Current Source suitable for Capacitive Measurement

Together with other on-chip analog modules, the CTMU can be used to precisely measure time, measure capacitance, measure relative changes in capacitance or generate output pulses that are independent of the system clock. The CTMU module is ideal for interfacing with capacitive-based touch sensors.

The CTMU is controlled through three registers: CTMUCON1, CTMUCON2 and CTMUICON. CTMUCON1 enables the module and controls the mode of operation of the CTMU, as well as controlling edge sequencing. CTMUCON2 controls edge source selection and edge source polarity selection. The CTMUICON register selects the current range of current source and trims the current.

32.1 Measuring Capacitance

The CTMU module measures capacitance by generating an output pulse with a width equal to the time between edge events on two separate input channels. The pulse edge events to both input channels can be selected from four sources: two internal peripheral modules (OC1 and Timer1) and up to 13 external pins (CTEDG1 through CTEDG13). This pulse is used with the module's precision current source to calculate capacitance according to the relationship:

EQUATION 32-1:

$$I = C \cdot \frac{dV}{dT}$$

For capacitance measurements, the A/D Converter samples an external Capacitor (CAPP) on one of its input channels after the CTMU output's pulse. A Precision Resistor (RPR) provides current source calibration on a second A/D channel. After the pulse ends, the converter determines the voltage on the capacitor. The actual calculation of capacitance is performed in software by the application.

Figure 32-1 illustrates the external connections used for capacitance measurements, and how the CTMU and A/D modules are related in this application. This example also shows the edge events coming from Timer1, but other configurations using external edge sources are possible. A detailed discussion on measuring capacitance and time with the CTMU module is provided in the *"dsPIC33/PIC24 Family Reference Manual",* **"Charge Time Measurement Unit (CTMU) and CTMU Operation with Threshold Detect"** (DS30009743).

Note: Only odd numbered ANx channels (AN1, AN3 to AN15) are connected to the CTMU during single-ended measurements.

REGISTER 32-2: CTMUCON2: CTMU CONTROL REGISTER 2 (CONTINUED)

bit 5-2 **EDG2SEL<3:0>:** Edge 2 Source Select bits
1111 = Edge 2 source is the Comparator 3 output
1110 = Edge 2 source is the Comparator 2 output
1101 = Edge 2 source is the Comparator 1 output
1100 = Unimplemented, do not use
1011 = Edge 2 source is IC3
1010 = Edge 2 source is IC2
1001 = Edge 2 source is IC1
1000 = Edge 2 source is CTED13
0111 = Edge 2 source is CTED12
0110 = Edge 2 source is CTED11(1)
0101 = Edge 2 source is CTED10(1)
0100 = Edge 2 source is CTED9
0011 = Edge 2 source is CTED1
0010 = Edge 2 source is CTED2
0001 = Edge 2 source is OC1
0000 = Edge 2 source is Timer1

bit 1-0 **Unimplemented:** Read as '0'

Note 1: Edge sources, CTED3, CTED7, CTED10 and CTED11, are available in 100-pin devices only.

FIGURE 38-37: 12-BIT PIPELINE A/D INL vs. SAMPLE RATE

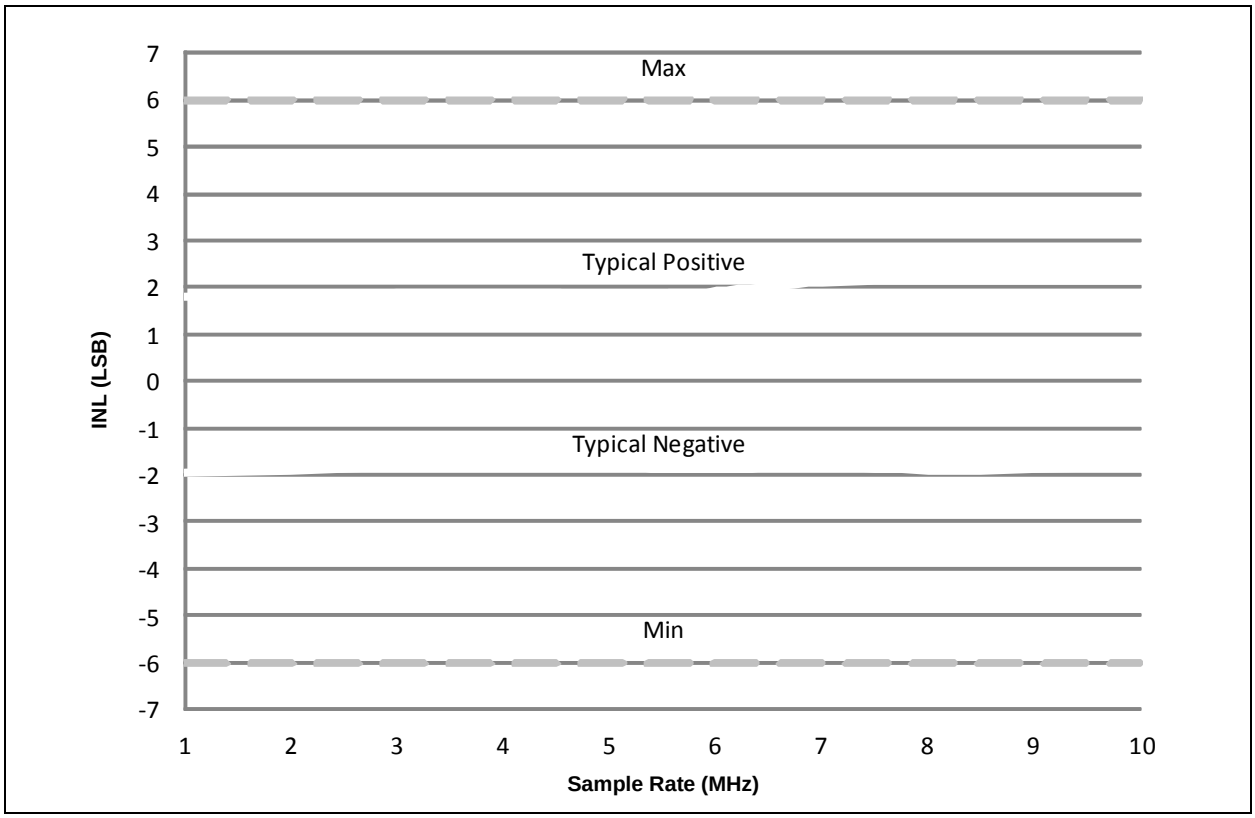
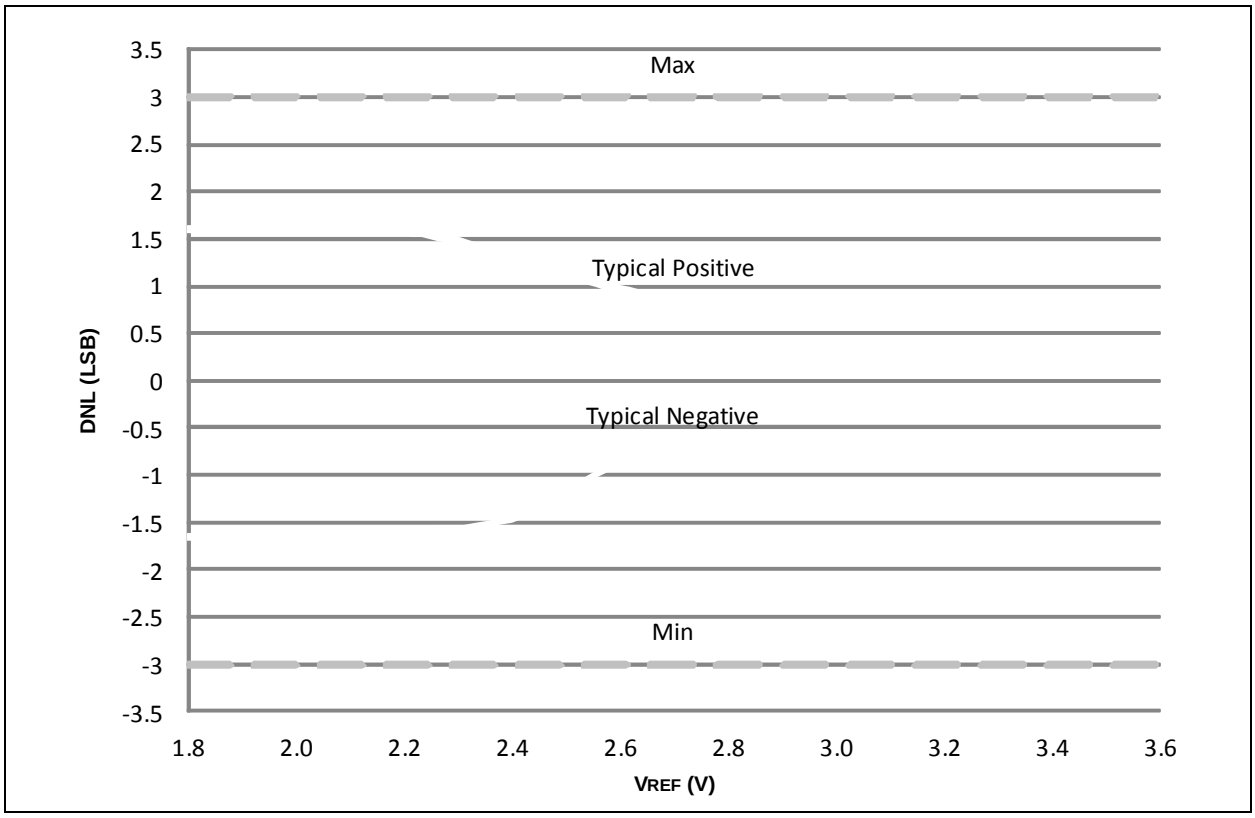
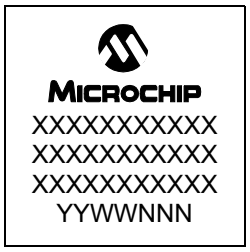


FIGURE 38-38: 12-BIT PIPELINE A/D DNL vs. VREF

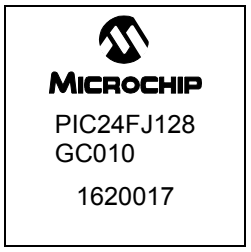


39.2 Package Marking Information (Continued)

121-BGA (10x10x1.1 mm)



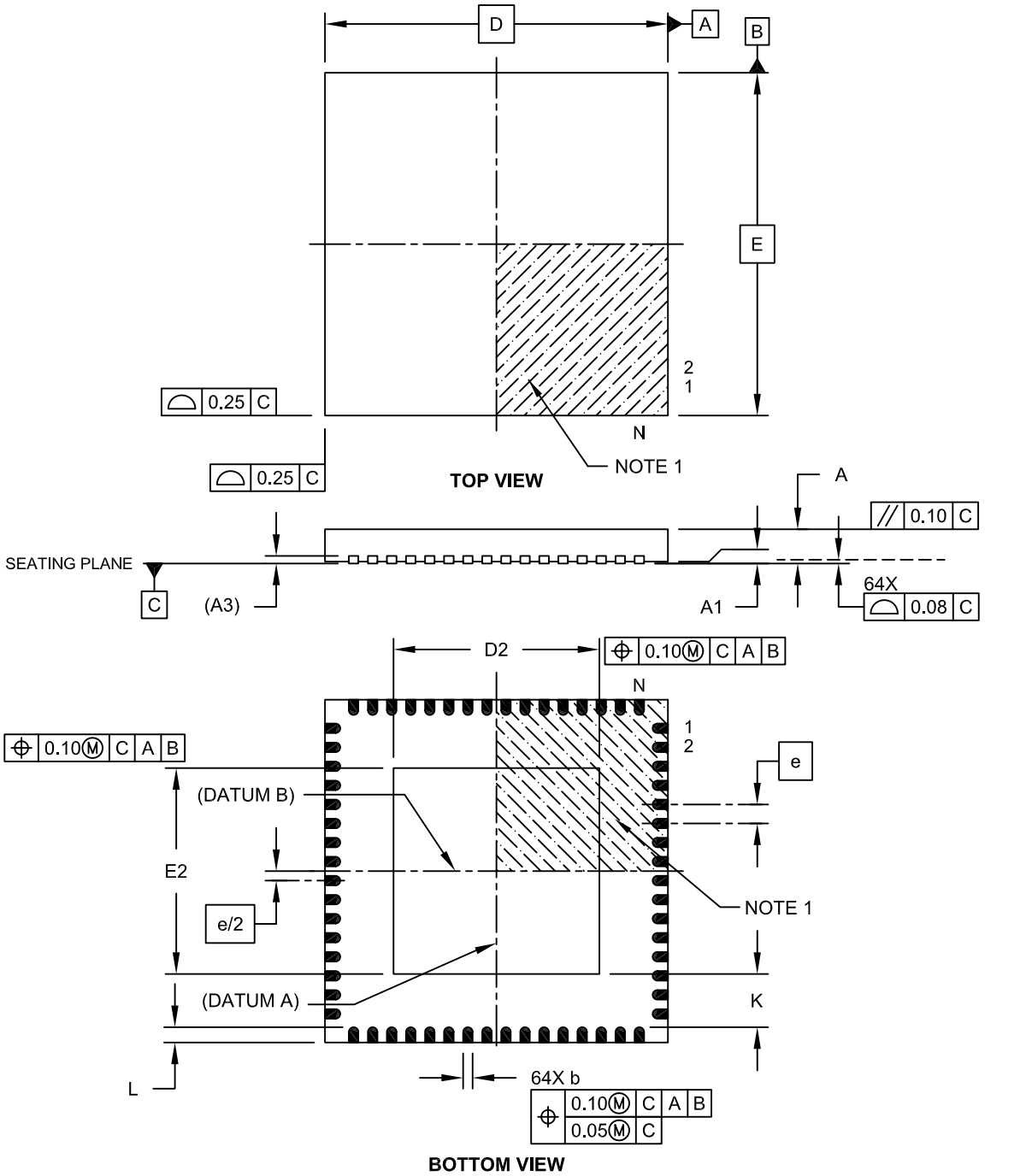
Example



39.3 Package Details

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body with 5.40 x 5.40 Exposed Pad [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-154A Sheet 1 of 2