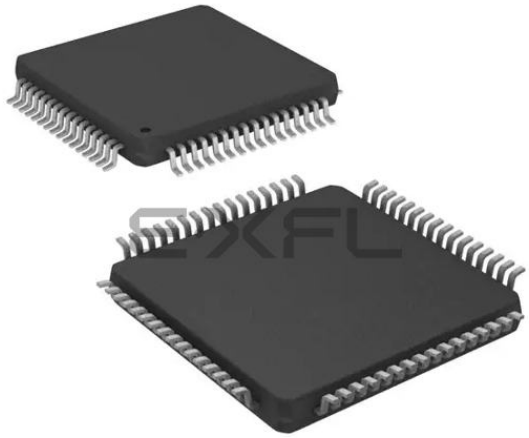

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, LCD, LVD, POR, PWM, WDT
Number of I/O	53
Program Memory Size	64KB (22K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 29x12b, 2x16b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj64gc006t-i-pt

TABLE 1-2: DEVICE FEATURES FOR THE PIC24FJ128GC010 FAMILY: 100/121-PIN DEVICES

Features	PIC24FJ64GC010	PIC24FJ128GC010
Operating Frequency	DC – 32 MHz	
Program Memory (bytes)	64K	128K
Program Memory (instructions)	22,016	44,032
Data Memory (bytes)	8K	
Interrupt Sources (soft vectors/ NMI traps)	66 (62/4)	
I/O Ports	Ports A, B, C, D, E, F, G	
Total I/O Pins	85	
Remappable Pins	44 (32 I/Os, 12 input only)	
Timers: Total Number (16-bit)	5(1)	
32-Bit (from paired 16-bit timers)	2	
Input Capture w/Timer Channels	9(1)	
Output Compare/PWM Channels	9(1)	
Input Change Notification Interrupt	82	
Serial Communications: UART	4(1)	
SPI (3-wire/4-wire)	2(1)	
I^2C	2	
Digital Signal Modulator	Yes	
Parallel Communications (EPMP/PSP)	Yes	
JTAG Boundary Scan	Yes	
12-Bit Pipeline Analog-to-Digital Converter (A/D) (input channels)	50	
Sigma-Delta Analog-to-Digital Converter (A/D) (differential channels)	2	
Digital-to-Analog Converter (DAC)	2	
Operational Amplifiers	2	
Analog Comparators	3	
CTMU Interface	Yes	
LCD Controller (available pixels)	472 (59 SEG x 8 COM)	
Resets (and delays)	Core POR, VDD POR, VBAT POR, BOR, RESET Instruction, MCLR, WDT, Illegal Opcode, REPEAT Instruction, Hardware Traps, Configuration Word Mismatch (OST, PLL Lock)	
Instruction Set	76 Base Instructions, Multiple Addressing Mode Variations	
Packages	100-Pin TQFP and 121-Pin BGA	

Note 1: Peripherals are accessible through remappable pins.

TABLE 1-3: PIC24FJ128GC010 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Function	Pin Number/Grid Locator			I/O	Input Buffer	Description
	64-Pin TQFP/QFN	100-Pin TQFP	121-Pin BGA			
PMA8	32	50	L11	O	—	Parallel Master Port Address (bits<22:2>).
PMA9	31	49	L10	O	—	
PMA10	28	42	L7	O	—	
PMA11	27	41	J7	O	—	
PMA12	33	51	K10	O	—	
PMA13	42	68	E9	O	—	
PMA14	45	71	C11	O	—	
PMA15	44	70	D11	O	—	
PMA16	—	95	C4	O	—	
PMA17	—	92	B5	O	—	
PMA18	—	40	K6	O	—	
PMA19	—	19	G2	O	—	
PMA20	—	59	G10	O	—	
PMA21	—	60	G11	O	—	
PMA22	—	66	E11	O	—	
PMACK1	50	77	A10	I	ST/TTL	Parallel Master Port Acknowledge Input 1.
PMACK2	43	69	E10	I	ST/TTL	Parallel Master Port Acknowledge Input 2.
PMBE0	51	78	B9	O	—	Parallel Master Port Byte Enable 0 Strobe.
PMBE1	—	67	E8	O	—	Parallel Master Port Byte Enable 1 Strobe.
PMCS1	—	18	G1	I/O	ST/TTL	Parallel Master Port Chip Select 1 Strobe.
PMCS2	—	9	K10	O	—	Parallel Master Port Chip Select 2 Strobe.
PMD0	60	93	A4	I/O	ST/TTL	Parallel Master Port Data (Demultiplexed Master mode) or Address/Data (Multiplexed Master modes).
PMD1	61	94	B4	I/O	ST/TTL	
PMD2	62	98	B3	I/O	ST/TTL	
PMD3	63	99	A2	I/O	ST/TTL	
PMD4	64	100	A1	I/O	ST/TTL	
PMD5	1	3	D3	I/O	ST/TTL	
PMD6	2	4	C1	I/O	ST/TTL	
PMD7	3	5	D2	I/O	ST/TTL	
PMD8	—	90	A5	I/O	ST/TTL	
PMD9	—	89	E6	I/O	ST/TTL	
PMD10	—	88	A6	I/O	ST/TTL	
PMD11	—	87	B6	I/O	ST/TTL	
PMD12	—	79	A9	I/O	ST/TTL	
PMD13	—	80	D8	I/O	ST/TTL	
PMD14	—	83	D7	I/O	ST/TTL	
PMD15	—	84	C7	I/O	ST/TTL	
PMRD	53	82	B8	O	—	Parallel Master Port Read Strobe.
PMWR	52	81	C8	O	—	Parallel Master Port Write Strobe.
PWRLCLK	48	74	B11	I	ST/TTL	Power Line (50 Hz/60 Hz) External Clock Input for RTCC.

Legend: TTL = TTL input buffer
ANA = Analog level input/output
ST = Schmitt Trigger input buffer
I^2C = I^2C/SMBus input buffer

3.2 CPU Control Registers

REGISTER 3-1: SR: ALU STATUS REGISTER(1)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	DC
bit 15							bit 8

R/W-0(2)	R/W-0(2)	R/W-0(2)	R-0	R/W-0	R/W-0	R/W-0,	R/W-0
IPL2(3)	IPL1(3)	IPL0(3)	RA	N	OV	Z	C
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-9 **Unimplemented:** Read as '0'

bit 8 **DC:** ALU Half Carry/Borrow bit
1 = A carry out from the 4th low-order bit (for byte-sized data) or 8th low-order bit (for word-sized data) of the result occurred
0 = No carry out from the 4th or 8th low-order bit of the result has occurred

bit 7-5 **IPL<2:0>:** CPU Interrupt Priority Level (IPL) Status bits(2,3)
111 = CPU Interrupt Priority Level is 7 (15); user interrupts are disabled
110 = CPU Interrupt Priority Level is 6 (14)
101 = CPU Interrupt Priority Level is 5 (13)
100 = CPU Interrupt Priority Level is 4 (12)
011 = CPU Interrupt Priority Level is 3 (11)
010 = CPU Interrupt Priority Level is 2 (10)
001 = CPU Interrupt Priority Level is 1 (9)
000 = CPU Interrupt Priority Level is 0 (8)

bit 4 **RA:** REPEAT Loop Active bit
1 = REPEAT loop is in progress
0 = REPEAT loop is not in progress

bit 3 **N:** ALU Negative bit
1 = Result was negative
0 = Result was not negative (zero or positive)

bit 2 **OV:** ALU Overflow bit
1 = Overflow occurred for signed (2's complement) arithmetic in this arithmetic operation
0 = No overflow has occurred

bit 1 **Z:** ALU Zero bit
1 = An operation resulted in the ALU having a value of zero.
0 = An operation resulted in the ALU having a non-zero value.

bit 0 **C:** ALU Carry/$\overline{\text{Borrow}}$ bit
1 = A carry out from the Most Significant bit (MSb) of the result occurred
0 = No carry out from the Most Significant bit of the result occurred

Note 1: ALU result flags are not affected for every operation. See Table 36-2 for details.
2: The IPLx Status bits are read-only when NSTDIS (INTCON1<15>) = 1.
3: The IPLx Status bits are concatenated with the IPL3 (CORCON<3>) bit to form the CPU Interrupt Priority Level (IPL). The value in parentheses indicates the IPL when IPL3 = 1.

REGISTER 8-2: CORCON: CPU CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R/C-0	r-1	U-0	U-0
—	—	—	—	IPL3(1)	—	—	—
bit 7							bit 0

Legend:	r = Reserved bit	C = Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-4 **Unimplemented:** Read as '0'

bit 3 **IPL3:** CPU Interrupt Priority Level Status bit(1)
1 = CPU Interrupt Priority Level is greater than 7
0 = CPU Interrupt Priority Level is 7 or less

bit 2 **Reserved:** Read as '1'

bit 1-0 **Unimplemented:** Read as '0'

Note 1: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level; see Register 3-2 for bit description.

REGISTER 8-21: IPC0: INTERRUPT PRIORITY CONTROL REGISTER 0

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	T1IP2	T1IP1	T1IP0	—	OC1IP2	OC1IP1	OC1IP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	IC1IP2	IC1IP1	IC1IP0	—	INT0IP2	INT0IP1	INT0IP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **T1IP<2:0>:** Timer1 Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **OC1IP<2:0>:** Output Compare Channel 1 Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **IC1IP<2:0>:** Input Capture Channel 1 Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **INT0IP<2:0>:** External Interrupt 0 Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

TABLE 10-2: EXITING POWER-SAVING MODES

Mode	Exit Conditions								Code Execution Resumes
	Interrupts		Resets			RTCC Alarm	WDT	VDD Restore	
	All	INT0	All	POR	$\overline{MCLR}$				
Idle	Y	Y	Y	Y	Y	Y	Y	N/A	Next instruction
Sleep (all modes)	Y	Y	Y	Y	Y	Y	Y	N/A	
Deep Sleep	N	Y	N	Y	Y	Y	Y(1)	N/A	Reset vector
Retention Deep Sleep	N	Y	N	Y	Y	Y	Y(1)	N/A	Next instruction(2)
VBAT	N	N	N	N	N	N	N	Y	Reset vector

Note 1: Deep Sleep WDT.

2: $\overline{MCLR}$ assertion always results in a POR Reset (execution from the Reset vector).

REGISTER 11-42: RPOR14: PERIPHERAL PIN SELECT OUTPUT REGISTER 14

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP29R5	RP29R4	RP29R3	RP29R2	RP29R1	RP29R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP28R5	RP28R4	RP28R3	RP28R2	RP28R1	RP28R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP29R<5:0>:** RP29 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP29 (see Table 11-4 for peripheral function numbers).

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP28R<5:0>:** RP28 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP28 (see Table 11-4 for peripheral function numbers).

REGISTER 11-43: RPOR15: PERIPHERAL PIN SELECT OUTPUT REGISTER 15

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP31R5(1)	RP31R4(1)	RP31R3(1)	RP31R2(1)	RP31R1(1)	RP31R0(1)
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP30R5	RP30R4	RP30R3	RP30R2	RP30R1	RP30R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP31R<5:0>:** RP31 Output Pin Mapping bits(1)
Peripheral Output Number n is assigned to pin, RP31 (see Table 11-4 for peripheral function numbers).

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP30R<5:0>:** RP30 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP30 (see Table 11-4 for peripheral function numbers).

Note 1: These bits are unimplemented in 64-pin devices; read as '0'.

REGISTER 19-7: U1CON: USB CONTROL REGISTER (DEVICE MODE)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R-x, HSC	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	SE0	PKTDIS	—	HOSTEN	RESUME	PPBRST	USBEN
bit 7							bit 0

Legend:	U = Unimplemented bit, read as '0'		
R = Readable bit	W = Writable bit	HSC = Hardware Settable/Clearable bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-7 **Unimplemented:** Read as '0'

bit 6 **SE0:** Live Single-Ended Zero Flag bit
1 = Single-ended zero is active on the USB bus
0 = No single-ended zero is detected

bit 5 **PKTDIS:** Packet Transfer Disable bit
1 = SIE token and packet processing are disabled; automatically set when a SETUP token is received
0 = SIE token and packet processing are enabled

bit 4 **Unimplemented:** Read as '0'

bit 3 **HOSTEN:** Host Mode Enable bit
1 = USB host capability is enabled; pull-downs on D+ and D- are activated in hardware
0 = USB host capability is disabled

bit 2 **RESUME:** Resume Signaling Enable bit
1 = Resume signaling is activated
0 = Resume signaling is disabled

bit 1 **PPBRST:** Ping-Pong Buffers Reset bit
1 = Resets all Ping-Pong Buffer Pointers to the even BD banks
0 = Ping-Pong Buffer Pointers are not reset

bit 0 **USBEN:** USB Module Enable bit
1 = USB module and supporting circuitry are enabled (device attached); D+ pull-up is activated in hardware
0 = USB module and supporting circuitry are disabled (device detached)

REGISTER 19-15: U1OTGIE: USB OTG INTERRUPT ENABLE REGISTER (HOST MODE ONLY)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
IDIE	T1MSECIE	LSTATEIE	ACTVIE	SESVDIE	SESENDIE	—	VBUSVDIE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **IDIE:** ID Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 6 **T1MSECIE:** 1 Millisecond Timer Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 5 **LSTATEIE:** Line State Stable Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 4 **ACTVIE:** Bus Activity Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 3 **SESVDIE:** Session Valid Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 2 **SESENDIE:** B-Device Session End Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 1 **Unimplemented:** Read as '0'

bit 0 **VBUSVDIE:** A-Device VBUS Valid Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

23.3 Registers

23.3.1 RTCC CONTROL REGISTERS

REGISTER 23-1: RCFGCAL: RTCC CALIBRATION/CONFIGURATION REGISTER(1)

R/W-0	U-0	R/W-0	R-0, HSC	R-0, HSC	R/W-0	R/W-0	R/W-0
RTCEN(2)	—	RTCWREN	RTCSYNC	HALFSEC(3)	RTCOE	RTCPTR1	RTCPTR0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CAL7	CAL6	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0
bit 7							bit 0

Legend:	HSC = Hardware Settable/Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **RTCEN:** RTCC Enable bit(2)
1 = RTCC module is enabled
0 = RTCC module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **RTCWREN:** RTCC Value Registers Write Enable bit
1 = RTCVALH and RTCVALL registers can be written to by the user
0 = RTCVALH and RTCVALL registers are locked out from being written to by the user

bit 12 **RTCSYNC:** RTCC Value Registers Read Synchronization bit
1 = RTCVALH, RTCVALL and ALCFGRPT registers can change while reading due to a rollover ripple resulting in an invalid data read. If the register is read twice and results in the same data, the data can be assumed to be valid.
0 = RTCVALH, RTCVALL or ALCFGRPT register can be read without concern over a rollover ripple

bit 11 **HALFSEC:** Half Second Status bit(3)
1 = Second half period of a second
0 = First half period of a second

bit 10 **RTCOE:** RTCC Output Enable bit
1 = RTCC output is enabled
0 = RTCC output is disabled

bit 9-8 **RTCPTR<1:0>:** RTCC Value Register Window Pointer bits
Points to the corresponding RTCC Value registers when reading the RTCVALH and RTCVALL registers. The RTCPTR<1:0> value decrements on every read or write of RTCVALH until it reaches '00'.
RTCVAL<15:8>:
11 = Reserved
10 = MONTH
01 = WEEKDAY
00 = MINUTES
RTCVAL<7:0>:
11 = YEAR
10 = DAY
01 = HOURS
00 = SECONDS

Note 1: The RCFGCAL register is only affected by a POR.
2: A write to the RTCEN bit is only allowed when RTCWREN = 1.
3: This bit is read-only; it is cleared to '0' on a write to the lower half of the MINSEC register.

TABLE 25-1: SHARED ANALOG PINS

Analog Input Channel	Op Amp	Comparator	Comparator Reference	DAC	Band Gap	Other Analog
AN0	—	—	CVREF+	DVREF+	BGBUF1	AVREF+
AN1	OA2P1	—	CVREF-	—	—	AVREF-
AN2	OA2N2	C2INB	—	—	—	CTCMP
AN3	OA2OUT	C2INA	—	—	—	—
AN4	OA1N0	C1INB	—	—	—	—
AN5	OA1OUT	C1INA	—	—	—	—
AN6	OA1P3	—	—	—	—	—
AN9	OA1N2	—	—	—	—	—
AN10	OA2P2	—	CVREF	—	—	—
AN11	OA2N3	—	—	—	—	—
AN13	OA2P3	—	—	DAC2	—	—
AN14	OA2N4	—	—	—	—	CTPLS
AN17	OA1P1	C1IND	—	—	BGBUF2	—
AN18	OA1N4	C1INC	—	—	—	—
AN19	OA1N2	C2IND	—	—	—	—
AN20	—	C3INA	—	—	—	—
AN25	OA2N1	—	—	—	—	—
AN30	—	—	—	—	—	—
AN34	OA1P2	C3INB	—	—	—	—
AN41	—	C3IND	—	—	—	—
AN42	OA2P0	C3INC	—	—	—	—
AN43	OA2N0	—	—	—	—	—
AN44	OA2P4	—	—	—	—	—
AN47	OA1P4	—	—	—	—	—
AN48	OA1N1	—	—	—	—	—
AN49	OA1P0	C2INC	—	DAC1	—	—

Legend: Shaded cells are analog outputs.

REGISTER 26-1: ADCON1: A/D CONTROL REGISTER 1

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADON	—	ADSIDL	ADSLP	FORM3	FORM2	FORM1	FORM0
bit 15							bit 8

R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0	R/W-0
PUMPEN	ADCAL(2)	—	—	—	—	—	PWRLVL
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ADON:** A/D Module Enable bit
1 = Module is enabled
0 = Module is disabled (registers are still readable and writable)

bit 14 **Unimplemented:** Read as '0'

bit 13 **ADSIDL:** A/D Stop in Idle Control bit
1 = Halts when CPU is in Idle mode
0 = Continues to operate in CPU Idle mode

bit 12 **ADSLP:** A/D Suspend in Sleep Control bit
1 = Continues operation in Sleep mode
0 = Ignores triggers and clocks when CPU is in Sleep mode

bit 11-8 **FORM<3:0>:** Data Output Format bits
1xxx = Unimplemented, do not use
0111 = Signed Fractional (sddd dddd dddd 0000)
0110 = Fractional (dddd dddd dddd 0000)
0101 = Signed Integer (ssss sddd dddd dddd)
0100 = Integer (0000 dddd dddd dddd)
0011 = Signed Fractional (sddd dddd dddd 0000)
0010 = Fractional (dddd dddd dddd 0000)
0001 = Signed Integer (ssss sddd dddd dddd)
0000 = Integer, Raw Data (0000 dddd dddd dddd)

bit 7 **PUMPEN:** Analog Channel Switch Charge Pump Enable bit
1 = Charge pump for switches is enabled, reducing switch impedance(1)
0 = Charge pump for switches is disabled

bit 6 **ADCAL:** A/D Internal Analog Calibration bit(2)
1 = Initiates internal analog calibration
0 = No operation

bit 5-1 **Unimplemented:** Read as '0'

bit 0 **PWRLVL:** Power Level Select bit
1 = Full-Power mode; A/D clock rates from 1 MHz to 10 MHz are allowed
0 = Low-Power mode; A/D clock rates from 1 MHz to 2.5 MHz are allowed

Note 1: Use of the channel switch charge pump is recommended when AV_{DD} < 2.5V.
2: When set, ADCAL remains set for at least one T_{AD} and is then automatically cleared by hardware. Manually clearing the bit does not necessarily cancel the calibration routine. Calibration is complete when ADSTATH<1> = 1.

REGISTER 26-4: ADSTATH: A/D STATUS HIGH REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
—	—	—	—	—	PUMPST	ADREADY	ADBUSY
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

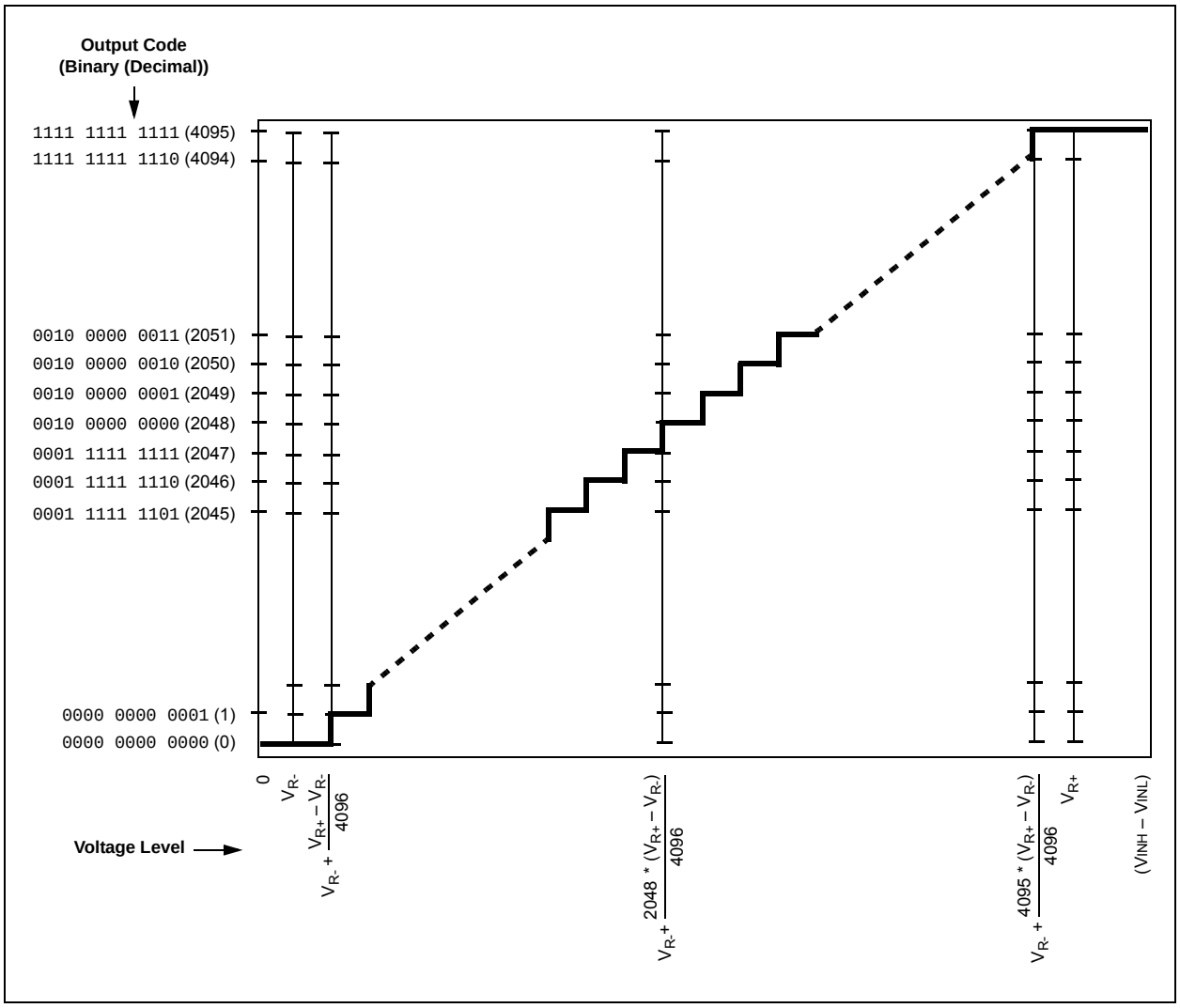
bit 15-3 **Unimplemented:** Read as ‘0’

bit 2 **PUMPST:** A/D Boost Pump Status bit
1 = The A/D boost pump is active
0 = The A/D boost pump is Idle

bit 1 **ADREADY:** A/D Analog Ready bit
1 = The analog portion of the A/D is warmed up, internally calibrated and ready
0 = The analog portion of the A/D is not ready

bit 0 **ADBUSY:** A/D Busy bit
1 = A/D conversion is in progress
0 = A/D is Idle

FIGURE 26-3: 12-BIT A/D TRANSFER FUNCTION



27.1 Important Differences Compared to Conventional A/D Converters

In principle, the Sigma-Delta A/D Converter does what most other A/Ds do: it samples an analog input voltage and generates a digital output code representing the analog voltage. There are, however, a number of differences when comparing a Sigma-Delta Converter to conventional A/D Converters, such as the Successive Approximation Register (SAR) design that is popular on many of today's microcontrollers.

The most important differences that are noticeable at the application level include:

- Variable signal bandwidth based on the OSR (Oversampling Ratio)
- Programmable input gain
- Uncorrected offset error
- Uncorrected gain error

27.1.1 RESULT QUALITY AND OVERSAMPLING

In a typical application, involving switching digital circuitry, oscillators, clocks and other noise sources common in a microcontroller-based circuit, it is often difficult to reduce the high-frequency noise floor below some arbitrary value. For A/Ds, which perform instantaneous "snapshot" based sampling (e.g., charging a Sample-and-Hold capacitor in a conventional SAR-based A/D), this noise floor ultimately restricts the maximum achievable stable result resolution.

To achieve higher effective stable resolution and to minimize the effects of high-frequency noise, the Sigma-Delta A/D Converter implements inherent oversampling in the design. This oversampling has an effect similar to low-pass filtering of the analog signal and voltage references to the A/D. Therefore, when the converter generates a result, the output code represents the average voltage of the signal or reference being measured over a specific time window, rather than an instantaneous snapshot in time (like that of the SAR-based A/D). This sampling method enables the Sigma-Delta A/D Converter to generate stable results at significantly higher resolution than is typically achievable with conventional A/D designs.

The design of this Sigma-Delta A/D Converter allows user-configurable Oversampling Ratios (OSRs), between 16 and 1024. The lowest settings provide the fastest results, but they sacrifice result code accuracy. The highest OSR settings provide the best quality and most stable results, but generate results at a much slower rate.

27.1.2 UNCORRECTED OFFSET ERROR

When uncorrected, the Sigma-Delta A/D Converter typically has more LSBs worth of offset error than conventional SAR-based A/Ds. This is partly due to the high resolution and small size of each LSB. Additionally, internal or external input circuitry, such as the internal input gain stage, can also introduce some offset error.

Fortunately, the Sigma-Delta A/D Converter implements a feature that allows it to measure its own internal offset error. This feature is controlled by the VOSCAL bit (SD1CON1<4>). Once the application firmware has measured the internal offset error, the digital output code can be saved in the firmware and subsequently subtracted from all future A/D measurements on the regular input channel(s). This procedure significantly improves the absolute accuracy of the A/D and is recommended for most applications.

27.1.3 UNCORRECTED GAIN ERROR

When uncorrected, Sigma-Delta A/D Converters typically exhibit high gain error compared to other A/D designs. To obtain high absolute accuracy from the Sigma-Delta A/D Converter, it is necessary to compensate for both offset error and gain error. Gain error can be corrected by first removing the offset error, then multiplying the resulting code with a suitable gain error correction factor.

One of the input channel settings selectable in the SD1CON3 register allows the A/D to measure its own references. When a measurement (with a gain of 1) is performed on this channel, the result code can be corrected for offset error (using the method described in **Section 27.1.2 "Uncorrected Offset Error"**) and then used to calculate the gain error correction factor. Once the gain error correction factor is known, it can be saved and stored in the firmware, so that it may be used later to correct for gain error when performing measurements on the other A/D input channels.

REGISTER 27-3: SD1CON3: S/D CONTROL REGISTER 3

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SDDIV2(1)	SDDIV1(1)	SDDIV0(1)	SDOSR2	SDOSR1	SDOSR0	SDCS1	SDCS0
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	SDCH2	SDCH1	SDCH0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 **SDDIV<2:0>:** S/D Input Clock Divider/Postscaler Ratio bits(1)
- 111 = Reserved
- 110 = 64
- 101 = 32
- 100 = 16
- 011 = 8
- 010 = 4
- 001 = 2
- 000 = 1 (No divider, clock selected by SDCS<1:0> is provided directly to A/D.)

bit 12-10 **SDOSR<2:0>:** S/D Oversampling Ratio (OSR) Selection bits
- 111 = Reserved
- 110 = 16 (fastest result, lowest quality)
- 101 = 32
- 100 = 64
- 011 = 128
- 010 = 256
- 001 = 512
- 000 = 1024 (slowest result, best quality)

bit 9-8 **SDCS<1:0>:** S/D A/D Module Clock Source Select bits
- 11 = Reserved
- 10 = Primary Oscillator (OSCI/CLKI)
- 01 = FRC (8 MHz)(2)
- 00 = System clock (FOSC/2)

bit 7-3 **Unimplemented:** Read as '0'

bit 2-0 **SDCH<2:0>:** S/D Analog Channel Input Select bits (positive input/negative input)
- 1xx = Reserved
- 011 = Measures the reference selected by SDREFP/SDREFN (used for gain error measurements)
- 010 = CH1SE/SVSS (single-ended measurement of CH1SE)
- 001 = CH1+/CH1- (Differential Channel 1)
- 000 = CH0+/CH0- (Differential Channel 0)

Note 1: To avoid overclocking or underclocking the module, set SDDIV<2:0> to obtain an A/D clock frequency (input frequency selected by SDCS<1:0> source, divided by selected SDDIVx ratio) at or between 1 MHz and 4 MHz.

2: Eight MHz FRC output is used directly, prior to the FRCDIV postscaler.

REGISTER 29-1: AMPxCON: OP AMP x CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R-0	R-x	R/W-0
AMPEN	—	AMPSIDL	AMPSLP	INTPOL1	INTPOL0	CMOUT	CMPSEL
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SPDSEL	AMPOE	NINSEL2	NINSEL1	NINSEL0	PINSEL2	PINSEL1	PINSEL0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **AMPEN:** Op Amp Control Module Enable bit
1 = Module is enabled
0 = Module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **AMPSIDL:** Op Amp Peripheral Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12 **AMPSLP:** Op Amp Peripheral Enabled in Sleep Mode bit
1 = Continues module operation when device enters Sleep mode
0 = Discontinues module operation in Sleep mode

bit 11-10 **INTPOL<1:0>:** Interrupt Mode Select bits
When CMPSEL = 1:
11 = Interrupt occurs on any change
10 = Interrupt occurs on negative edge
01 = Interrupt occurs on positive edge
00 = Interrupts are disabled
When CMPSEL = 0:
Op amp interrupts are not generated.

bit 9 **CMOUT:** Comparator Mode Output State bit
When CMPSEL = 1:
1 = Non-inverting input is greater than the inverting input
0 = Non-inverting input is less than the inverting input
When CMPSEL = 0:
Op Amp mode (no digital state information is generated).

bit 8 **CMPSEL:** Op Amp Mode Select bit
1 = Configured as a comparator
0 = Configured as an op amp

bit 7 **SPDSEL:** Op Amp/Comparator Power/Speed Select bit
1 = Higher power and bandwidth (faster response time)
0 = Lower power and bandwidth (slower response time)

bit 6 **AMPOE:** Amplifier Output Enable bit
1 = Amplifier or comparator output is sent to OAxOUT pin
0 = Amplifier or comparator output is not sent to OAxOUT (pin is controlled by TRISx and LATx bits)

REGISTER 34-5: DEVID: DEVICE ID REGISTER

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 23							bit 16

R	R	R	R	R	R	R	R
FAMID7	FAMID6	FAMID5	FAMID4	FAMID3	FAMID2	FAMID1	FAMID0
bit 15							bit 8

R	R	R	R	R	R	R	R
DEV7	DEV6	DEV5	DEV4	DEV3	DEV2	DEV1	DEV0
bit 7							bit 0

Legend: R = Readable bit	U = Unimplemented bit

bit 23-16 **Unimplemented:** Read as '1'

bit 15-8 **FAMID<7:0>:** Device Family Identifier bits

0100 1000 = PIC24FJ128GC010 family

bit 7-0 **DEV<7:0>:** Individual Device Identifier bits

1000 1000 = PIC24FJ64GC006
1000 1001 = PIC24FJ128GC006
1000 0100 = PIC24FJ64GC010
1000 0101 = PIC24FJ128GC010

REGISTER 34-6: DEVREV: DEVICE REVISION REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 23							bit 16

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R	R	R	R
—	—	—	—	REV3	REV2	REV1	REV0
bit 7							bit 0

Legend: R = Readable bit	U = Unimplemented bit

bit 23-4 **Unimplemented:** Read as '0'

bit 3-0 **REV<3:0>:** Device Revision Identifier bits

TABLE 37-11: INTERNAL VOLTAGE REGULATOR SPECIFICATIONS

Operating Conditions: -40°C < TA < +85°C (unless otherwise stated)							
Param No.	**Symbol**	**Characteristics**	**Min**	**Typ**	**Max**	**Units**	**Comments**
DVR10	VBG	Internal Band Gap Reference	—	1.2	—	V	
DVR11	TBG	Band Gap Reference Start-up Time	—	1	—	ms	
DVR20	VRGOUT	Regulator Output Voltage	—	1.8	—	V	VDD > 2.0V
DVR21	CEFC	External Filter Capacitor Value	4.7	10	—	µF	Series Resistance < 3Ω recommended; < 5Ω required
DVR25	TVREG	Start-up Time	—	10	—	µs	PMSLP = 1 with any POR or BOR
DVR30	VLVR	Low-Voltage Regulator Output Voltage	—	1.2	—	V	RETEN = 1, $\overline{\text{LPCFG}}$ = 0

TABLE 37-12: BAND GAP REFERENCE (BGBUFn) SPECIFICATIONS

Operating Conditions: -40°C < TA < +85°C, 2.0V < (A)VDD < 3.6V(1)							
Param No.	**Sym**	**Characteristics**	**Min**	**Typ**	**Max**	**Units**	**Comments**
DBG01		Recommended Output Capacitance for Optimal Transient Response	—	—	22	µF	BGBUF1 or BGBUF2
DBG02		Output Voltage	1.140	1.200	1.260	V	BUFREF<1:0> = 00, 2.0V < AVDD < 3.6V
DBG03			1.945	2.048	2.151	V	BUFREF<1:0> = 01(2)
DBG04			2.432	2.560	2.688	V	BUFREF<1:0> = 10(2)
DBG05			2.918	3.072	3.226	V	BUFREF<1:0> = 11(2)
DBG07		DC Output Resistance	20	—	—	Ω	BUFREF<1:0> = 00, 2.0V < AVDD ≤ 2.5V
DBG08			20	—	—	Ω	BUFREF<1:0> = 00, 2.5V < AVDD < 3.6V
DBG09			20	—	—	Ω	BUFREF<1:0> = 01, 10 or 11(2)
DBG10		Maximum Continuous DC Output Current Rating	—	—	1	mA	This value is not tested in production(3)
DBG11		Module Start-up Time from Disabled State	—	5	—	ms	Time from BUFEN and BUFOE = 1 to output stable, CLOAD = 20 µF
DBG12		Module Start-up Time from Standby Mode	—	100	—	µs	Time from BUFSTBY = 0 to output stable
DBG14		AVDD Active Current	—	100	—	µA	Module enabled, BUFOE = 1

Note 1: No DC loading on module unless otherwise stated.

2: For BUFREF<1:0> ≠ 00, (Reference Output Max + 100 mV) < AVDD < 3.6V.

3: To minimize voltage error, the DC loading on the BGBUFn output pins should be <100 µA.

FIGURE 38-47: 10-BIT DAC OFFSET vs. TEMPERATURE

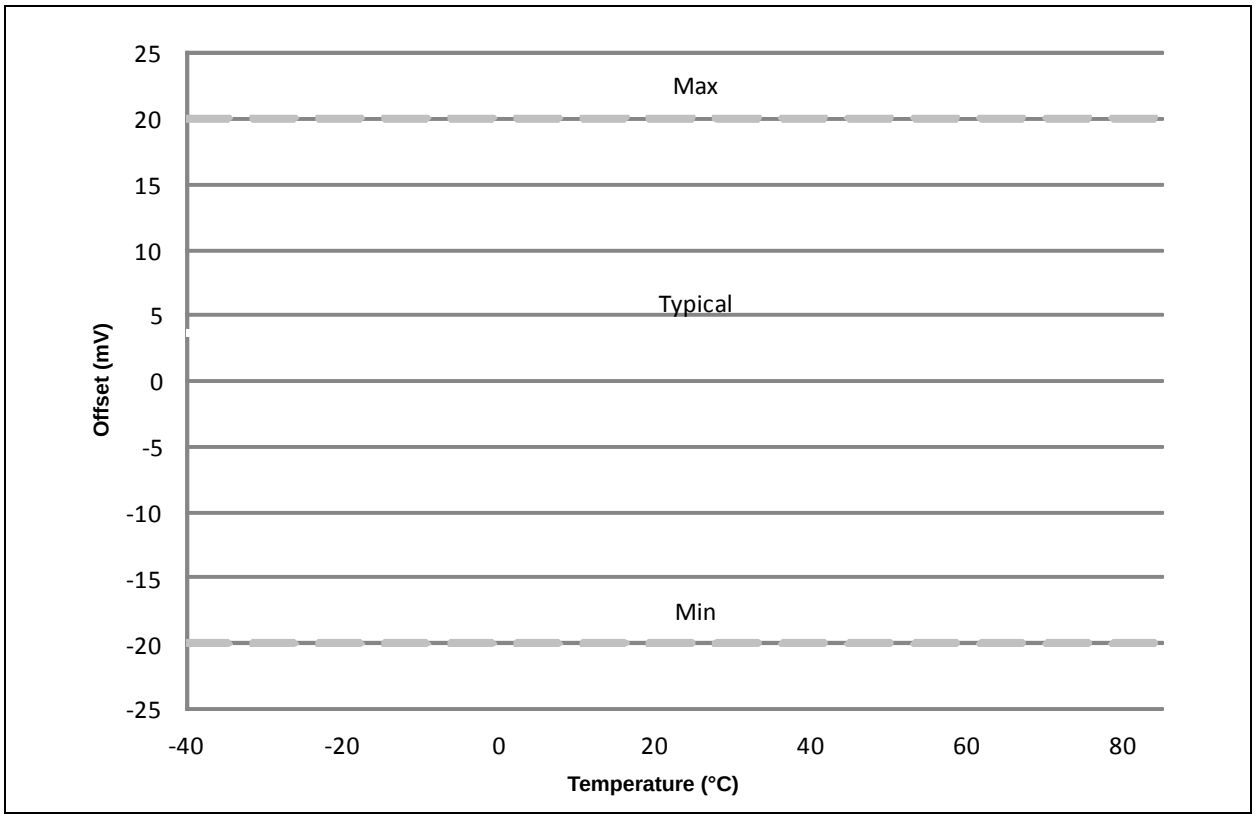


FIGURE 38-48: 10-BIT DAC GAIN vs. TEMPERATURE