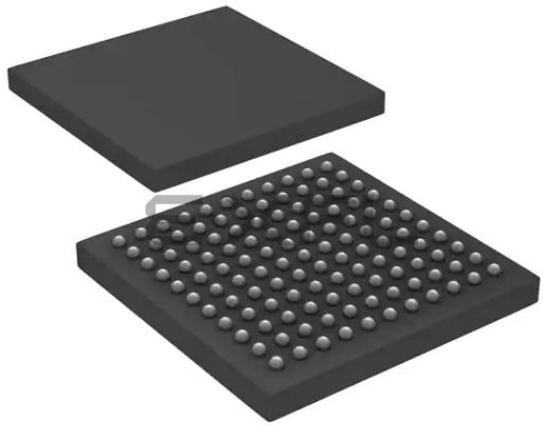
Microchip Technology - PIC24FJ64GC010T-I/BG Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, LCD, LVD, POR, PWM, WDT
Number of I/O	85
Program Memory Size	64KB (22K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 50x12b, 2x16b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	121-TFBGA
Supplier Device Package	121-TFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj64gc010t-i-bg

TABLE 1-2: DEVICE FEATURES FOR THE PIC24FJ128GC010 FAMILY: 100/121-PIN DEVICES

Features	PIC24FJ64GC010	PIC24FJ128GC010
Operating Frequency	DC – 32 MHz	
Program Memory (bytes)	64K	128K
Program Memory (instructions)	22,016	44,032
Data Memory (bytes)	8K	
Interrupt Sources (soft vectors/ NMI traps)	66 (62/4)	
I/O Ports	Ports A, B, C, D, E, F, G	
Total I/O Pins	85	
Remappable Pins	44 (32 I/Os, 12 input only)	
Timers: Total Number (16-bit)	5(1)	
32-Bit (from paired 16-bit timers)	2	
Input Capture w/Timer Channels	9(1)	
Output Compare/PWM Channels	9(1)	
Input Change Notification Interrupt	82	
Serial Communications: UART	4(1)	
SPI (3-wire/4-wire)	2(1)	
I^2C	2	
Digital Signal Modulator	Yes	
Parallel Communications (EPMP/PSP)	Yes	
JTAG Boundary Scan	Yes	
12-Bit Pipeline Analog-to-Digital Converter (A/D) (input channels)	50	
Sigma-Delta Analog-to-Digital Converter (A/D) (differential channels)	2	
Digital-to-Analog Converter (DAC)	2	
Operational Amplifiers	2	
Analog Comparators	3	
CTMU Interface	Yes	
LCD Controller (available pixels)	472 (59 SEG x 8 COM)	
Resets (and delays)	Core POR, VDD POR, VBAT POR, BOR, RESET Instruction, MCLR, WDT, Illegal Opcode, REPEAT Instruction, Hardware Traps, Configuration Word Mismatch (OST, PLL Lock)	
Instruction Set	76 Base Instructions, Multiple Addressing Mode Variations	
Packages	100-Pin TQFP and 121-Pin BGA	

Note 1: Peripherals are accessible through remappable pins.

TABLE 1-3: PIC24FJ128GC010 FAMILY PINOUT DESCRIPTION

Pin Function	Pin Number/Grid Locator			I/O	Input Buffer	Description
	64-Pin TQFP/QFN	100-Pin TQFP	121-Pin BGA			
AN0	16	25	K2	I	ANA	12-Bit Pipeline A/D Converter Inputs.
AN1	15	24	K1	I	ANA	
AN2	14	23	J2	I	ANA	
AN3	13	22	J1	I	ANA	
AN4	12	21	H2	I	ANA	
AN5	11	20	H1	I	ANA	
AN6	17	26	L1	I	ANA	
AN7	18	27	J3	I	ANA	
AN8	—	6	D1	I	ANA	
AN9	—	8	E2	I	ANA	
AN10	32	50	L11	I	ANA	
AN11	31	49	L10	I	ANA	
AN12	27	41	J7	I	ANA	
AN13	28	42	L7	I	ANA	
AN14	29	43	K7	I	ANA	
AN15	30	44	L8	I	ANA	
AN16	—	9	E1	I	ANA	
AN17	4	10	E3	I	ANA	
AN18	5	11	F4	I	ANA	
AN19	6	12	F2	I	ANA	
AN20	55	84	C7	I	ANA	
AN21	—	19	G2	I	ANA	
AN22	—	92	B5	I	ANA	
AN23	—	91	C5	I	ANA	
AN24	43	69	E10	I	ANA	
AN25	50	77	A10	I	ANA	
AN26	—	38	J6	I	ANA	
AN27	—	39	L6	I	ANA	
AN28	—	47	L9	I	ANA	
AN29	—	48	K9	I	ANA	
AN30	33	51	K10	I	ANA	
AN31	—	52	K11	I	ANA	
AN32	—	53	J10	I	ANA	
AN33	—	1	B2	I	ANA	
AN34	54	83	D7	I	ANA	
AN35	49	76	A11	I	ANA	
AN36	—	60	G11	I	ANA	
AN37	—	61	G9	I	ANA	
AN38	—	66	E11	I	ANA	
AN39	—	67	E8	I	ANA	
AN40	42	68	E9	I	ANA	

Legend: TTL = TTL input buffer
ANA = Analog level input/output
ST = Schmitt Trigger input buffer
I^2C = I^2C/SMBus input buffer

4.1.1 PROGRAM MEMORY ORGANIZATION

The program memory space is organized in word-addressable blocks. Although it is treated as 24 bits wide, it is more appropriate to think of each address of the program memory as a lower and upper word, with the upper byte of the upper word being unimplemented. The lower word always has an even address, while the upper word has an odd address (Figure 4-2).

Program memory addresses are always word-aligned on the lower word and addresses are incremented or decremented by two during code execution. This arrangement also provides compatibility with data memory space addressing and makes it possible to access data in the program memory space.

4.1.2 HARD MEMORY VECTORS

All PIC24F devices reserve the addresses between 000000h and 000200h for hard-coded program execution vectors. A hardware Reset vector is provided to redirect code execution from the default value of the PC on device Reset to the actual start of code. A GOTO instruction is programmed by the user at 000000h with the actual address for the start of code at 000002h.

PIC24F devices also have two Interrupt Vector Tables (IVTs), located from 000004h to 0000FFh and 000100h to 0001FFh. These vector tables allow each of the many device interrupt sources to be handled by separate ISRs. A more detailed discussion of the Interrupt Vector Tables is provided in **Section 8.1 "Interrupt Vector Table"**.

4.1.3 FLASH CONFIGURATION WORDS

In PIC24FJ128GC010 family devices, the top four words of on-chip program memory are reserved for configuration information. On device Reset, the configuration information is copied into the appropriate Configuration register. The addresses of the Flash Configuration Word for devices in the PIC24FJ128GC010 family are shown in Table 4-1. Their location in the memory map is shown with the other memory vectors in Figure 4-1.

The Configuration Words in program memory are a compact format. The actual Configuration bits are mapped in several different registers in the configuration memory space. Their order in the Flash Configuration Words does not reflect a corresponding arrangement in the configuration space. Additional details on the device Configuration Words are provided in **Section 34.0 "Special Features"**.

TABLE 4-1: FLASH CONFIGURATION WORDS FOR PIC24FJ128GC0 FAMILY DEVICES

Device	Program Memory (Words)	Configuration Word Addresses
PIC24FJ64GC0XX	22,016	00ABF8h:00ABFEh
PIC24FJ128GC0XX	44,032	0157F8h:0157FEh

FIGURE 4-2: PROGRAM MEMORY ORGANIZATION

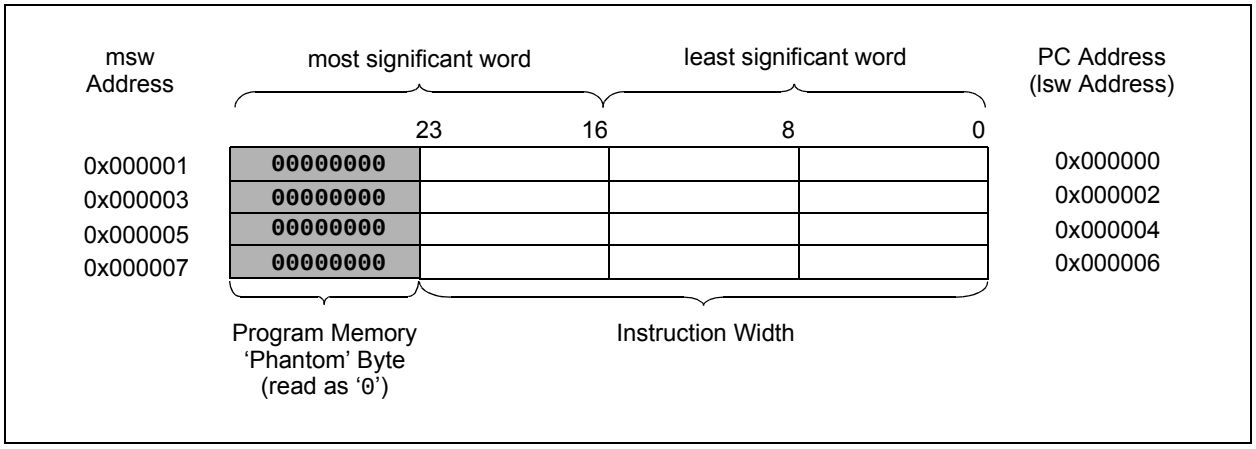

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TABLE 4-25: 12-BIT PIPELINE A/D CONVERTER REGISTER MAP (CONTINUED)

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
ADRES0	0340	A/D Result Register 0																0000
ADRES1	0342	A/D Result Register 1																0000
ADRES2	0344	A/D Result Register 2																0000
ADRES3	0346	A/D Result Register 3																0000
ADRES4	0348	A/D Result Register 4																0000
ADRES5	034A	A/D Result Register 5																0000
ADRES6	034C	A/D Result Register 6																0000
ADRES7	034E	A/D Result Register 7																0000
ADRES8	0350	A/D Result Register 8																0000
ADRES9	0352	A/D Result Register 9																0000
ADRES10	0354	A/D Result Register 10																0000
ADRES11	0356	A/D Result Register 11																0000
ADRES12	0358	A/D Result Register 12																0000
ADRES13	035A	A/D Result Register 13																0000
ADRES14	035C	A/D Result Register 14																0000
ADRES15	035E	A/D Result Register 15																0000
ADRES16	0360	A/D Result Register 16																0000
ADRES17	0362	A/D Result Register 17																0000
ADRES18	0364	A/D Result Register 18																0000
ADRES19	0366	A/D Result Register 19																0000
ADRES20	0368	A/D Result Register 20																0000
ADRES21	036A	A/D Result Register 21																0000
ADRES22	036C	A/D Result Register 22																0000
ADRES23	036E	A/D Result Register 23																0000
ADRES24	0370	A/D Result Register 24																0000
ADRES25	0372	A/D Result Register 25																0000
ADRES26	0374	A/D Result Register 26																0000
ADRES27	0376	A/D Result Register 27																0000
ADRES28	0378	A/D Result Register 28																0000
ADRES29	037A	A/D Result Register 29																0000
ADRES30	037C	A/D Result Register 30																0000
ADRES31	037E	A/D Result Register 31																0000

Legend: — = unimplemented, read as '0'; r = reserved, do not modify. Reset values are shown in hexadecimal.

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TABLE 4-32: COMPARATORS REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CMSTAT	0630	CMIDL	—	—	—	—	C3EVT	C2EVT	C1EVT	—	—	—	—	—	C3OUT	C2OUT	C1OUT	0000
CVRCON	0632	—	—	—	—	—	CVREFP	CVREFM1	CVREFM0	CVREN	CVROE	CVRSS	CVR4	CVR3	CVR2	CVR1	CVR0	0000
CM1CON	0634	CON	COE	CPOL	—	—	—	CEVT	COUT	EVPOL1	EVPOL0	—	CREF	—	—	CCH1	CCH0	0000
CM2CON	0636	CON	COE	CPOL	—	—	—	CEVT	COUT	EVPOL1	EVPOL0	—	CREF	—	—	CCH1	CCH0	0000
CM3CON	0638	CON	COE	CPOL	—	—	—	CEVT	COUT	EVPOL1	EVPOL0	—	CREF	—	—	CCH1	CCH0	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-33: CRC REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CRCCON1	0640	CRCEN	—	CSIDL	VWORD4	VWORD3	VWORD2	VWORD1	VWORD0	CRCFUL	CRCMPT	CRCISEL	CRCGO	LENDIAN	—	—	—	0040
CRCCON2	0642	—	—	—	DWIDTH4	DWIDTH3	DWIDTH2	DWIDTH1	DWIDTH0	—	—	—	PLEN4	PLEN3	PLEN2	PLEN1	PLEN0	0000
CRCXORL	0644	X<15:1>															—	0000
CRCXORH	0646	X<31:16>																0000
CRCDATL	0648	CRC Data Input Register Low																0000
CRCDATH	064A	CRC Data Input Register High																0000
CRCWDATL	064C	CRC Result Register Low																0000
CRCWDATH	064E	CRC Result Register High																0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-34: BAND GAP BUFFER INTERFACE REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
BUFCON0	0670	BUFEN	—	BUFSIDL	BUFSLP	—	—	—	—	—	BUFSTBY	—	—	—	—	BUFREF1	BUFREF0	0000
BUFCON1	0672	BUFEN	—	BUFSIDL	BUFSLP	—	—	—	—	BUFOE	BUFSTBY	—	—	—	—	BUFREF1	BUFREF0	0000
BUFCON2	0674	BUFEN	—	BUFSIDL	BUFSLP	—	—	—	—	BUFOE	BUFSTBY	—	—	—	—	BUFREF1	BUFREF0	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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REGISTER 8-15: IEC2: INTERRUPT ENABLE CONTROL REGISTER 2 (CONTINUED)

bit 1 **SPI2IE:** SPI2 Event Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 0 **SPF2IE:** SPI2 Fault Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

REGISTER 8-16: IEC3: INTERRUPT ENABLE CONTROL REGISTER 3

U-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
—	RTCIE	DMA5IE	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	U-0
—	INT4IE(1)	INT3IE(1)	—	—	MI2C2IE	SI2C2IE	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14 **RTCIE:** Real-Time Clock and Calendar Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 13 **DMA5IE:** DMA Channel 5 Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 12-7 **Unimplemented:** Read as '0'

bit 6 **INT4IE:** External Interrupt 4 Enable bit(1)
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 5 **INT3IE:** External Interrupt 3 Enable bit(1)
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 4-3 **Unimplemented:** Read as '0'

bit 2 **MI2C2IE:** Master I2C2 Event Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 1 **SI2C2IE:** Slave I2C2 Event Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 0 **Unimplemented:** Read as '0'

Note 1: If an external interrupt is enabled, the interrupt input must also be configured to an available RPn or RPIn pin. See **Section 11.4 "Peripheral Pin Select (PPS)"** for more information.

REGISTER 11-7: ANSG: PORTG ANALOG FUNCTION SELECTION REGISTER

R/W-1	U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-1
ANSG15(1)	—	—	—	—	—	ANSG<9:8>	
bit 15							bit 8

R/W-1	R/W-1	U-0	U-0	U-0	U-0	U-0	U-0
ANSG<7:6>		—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ANSG15:** Analog Function Selection bit(1)
1 = Pin is configured in Analog mode; I/O port read is disabled
0 = Pin is configured in Digital mode; I/O port read is enabled

bit 14-10 **Unimplemented:** Read as '0'

bit 9-6 **ANSG<9:6>:** Analog Function Selection bits
1 = Pin is configured in Analog mode; I/O port read is disabled
0 = Pin is configured in Digital mode; I/O port read is enabled

bit 5-0 **Unimplemented:** Read as '0'

Note 1: This bit is not available in 64-pin devices.

REGISTER 11-8: ANCFG: ANALOG CONFIGURATION REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-0	U-0	U-0
—	—	—	—	—	VBG2EN	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-3 **Unimplemented:** Read as '0'

bit 2 **VBG2EN:** VBG/2 Enable bit
1 = Band gap voltage reference VBG/2 is enabled
0 = Band gap voltage reference VBG/2 is disabled

bit 1-0 **Unimplemented:** Read as '0'

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11.3 Input Change Notification (ICN)

The Input Change Notification function of the I/O ports allows the PIC24FJ128GC010 family of devices to generate interrupt requests to the processor in response to a Change-of-State (COS) on selected input pins. This feature is capable of detecting input Change-of-States, even in Sleep mode, when the clocks are disabled. Depending on the device pin count, there are up to 82 external inputs that may be selected (enabled) for generating an interrupt request on a Change-of-State.

Registers, CNEN1 through CNEN6, contain the interrupt enable control bits for each of the Change Notification (CN) input pins. Setting any of these bits enables a CN interrupt for the corresponding pins.

Each CN pin has both a weak pull-up and a weak pull-down connected to it. The pull-ups act as a current source that is connected to the pin, while the pull-downs act as a current sink that is connected to the pin. These eliminate the need for external resistors when push button or keypad devices are connected. The pull-ups and pull-downs are separately enabled using the CNPU1 through CNPU6 registers (for pull-ups) and the CNPD1 through CNPD6 registers (for pull-downs). Each CN pin has individual control bits for its pull-up and pull-down. Setting a control bit enables the weak pull-up or pull-down for the corresponding pin.

When the internal pull-up is selected, the pin pulls up to V_{DD} – 1.1V (typical). When the internal pull-down is selected, the pin pulls down to V_{SS}.

Note:	Pull-ups on Change Notification pins should always be disabled whenever the port pin is configured as a digital output.

EXAMPLE 11-1: PORT WRITE/READ IN ASSEMBLY

```
MOV   0xFF00, W0   ; Configure PORTB<15:8> as inputs
MOV   W0, TRISB    ; and PORTB<7:0> as outputs
NOP                ; Delay 1 cycle
BTSS  PORTB, #13   ; Next Instruction
```

EXAMPLE 11-2: PORT WRITE/READ IN 'C'

```
TRISB = 0xFF00;              // Configure PORTB<15:8> as inputs and PORTB<7:0> as outputs
NOP();                       // Delay 1 cycle
If (PORTBbits.RB13){ };      // Next Instruction
```

11.4.3.2 Output Mapping

In contrast to inputs, the outputs of the Peripheral Pin Select options are mapped on the basis of the pin. In this case, a control register associated with a particular pin dictates the peripheral output to be mapped. The RPORx registers are used to control output mapping. Each register contains two 6-bit fields, with each field being associated with one RPn pin (see Register 11-28 through Register 11-43). The value of the bit field corresponds to one of the peripherals and that peripheral's output is mapped to the pin (see Table 11-4).

Because of the mapping technique, the list of peripherals for output mapping also includes a null value of '000000'. This permits any given pin to remain disconnected from the output of any of the pin-selectable peripherals.

TABLE 11-4: SELECTABLE OUTPUT SOURCES (MAPS FUNCTION TO OUTPUT)

Output Function Number(1)	Function	Output Name
0	NULL(2)	Null
1	C1OUT	Comparator 1 Output
2	C2OUT	Comparator 2 Output
3	U1TX	UART1 Transmit
4	$\overline{\text{U1RTS}}$(3)	UART1 Request-to-Send
5	U2TX	UART2 Transmit
6	$\overline{\text{U2RTS}}$(3)	UART2 Request-to-Send
7	SDO1	SPI1 Data Output
8	SCK1OUT	SPI1 Clock Output
9	SS1OUT	SPI1 Slave Select Output
10	SDO2	SPI2 Data Output
11	SCK2OUT	SPI2 Clock Output
12	SS2OUT	SPI2 Slave Select Output
18	OC1	Output Compare 1
19	OC2	Output Compare 2
20	OC3	Output Compare 3
21	OC4	Output Compare 4
22	OC5	Output Compare 5
23	OC6	Output Compare 6
24	OC7	Output Compare 7
25	OC8	Output Compare 8
28	U3TX	UART3 Transmit
29	$\overline{\text{U3RTS}}$(3)	UART3 Request-to-Send
30	U4TX	UART4 Transmit
31	$\overline{\text{U4RTS}}$(3)	UART4 Request-to-Send
35	OC9	Output Compare 9
36	C3OUT	Comparator 3 Output
37	MDOUT	DSM Modulator Output
38-63	(unused)	NC

Note 1: Setting the RPORx register with the listed value assigns that output function to the associated RPn pin.

2: The NULL function is assigned to all RPn outputs at device Reset and disables the RPn output function.

3: IrDA® BCLKx functionality uses this output.

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19.1.2 HOST AND OTG MODES

19.1.2.1 D+ and D- Pull-Down Resistors

PIC24FJ128GC010 family devices have a built-in 15 kΩ pull-down resistor on the D+ and D- lines. These are used in tandem to signal to the bus that the microcontroller is operating in Host mode. They are engaged by setting the HOSTEN bit (U1CON<3>). If the OTGEN bit (U1OTGCON<2>) is set, then these pull-downs are enabled by setting the DPPULDWN and DMPULDWN bits (U1OTGCON<5:4>).

19.1.2.2 Power Configurations

In Host mode, as well as Host mode in On-The-Go operation, the *"USB 2.0 OTG Specification"* requires that the host application should supply power on VBUS. Since the microcontroller is running below VBUS, and is not able to source sufficient current, a separate power supply must be provided.

When the application is always operating in Host mode, a simple circuit can be used to supply VBUS and regulate current on the bus (Figure 19-5). For OTG operation, it is necessary to be able to turn VBUS on or off as needed, as the microcontroller switches between Device and Host modes. A typical example using an external charge pump is shown in Figure 19-6.

FIGURE 19-5: USB OTG HOST INTERFACE EXAMPLE

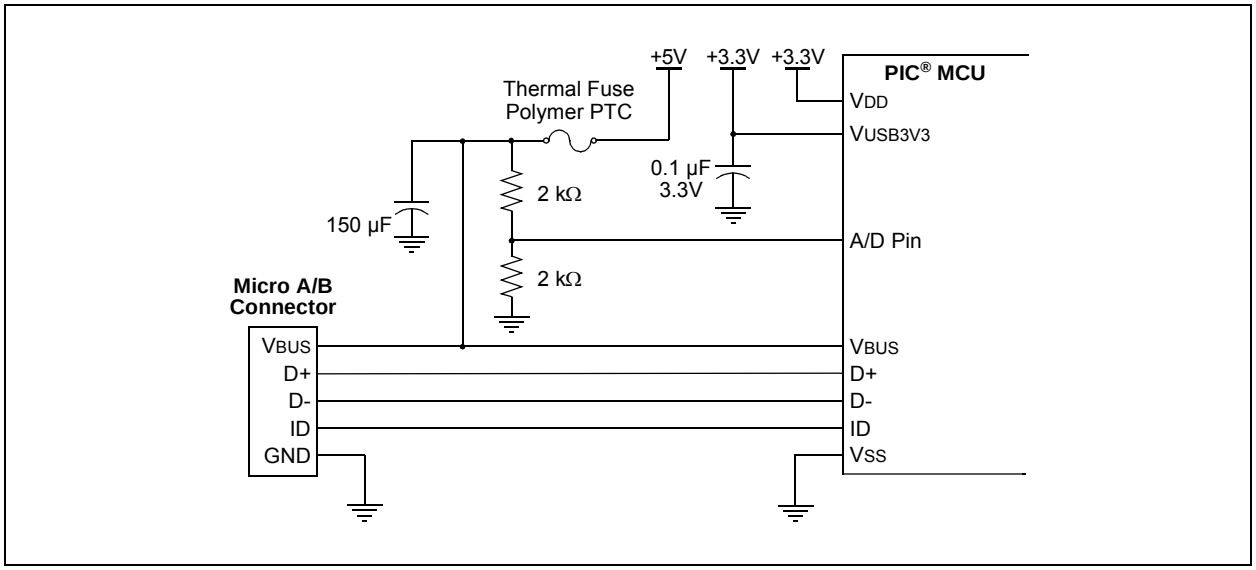
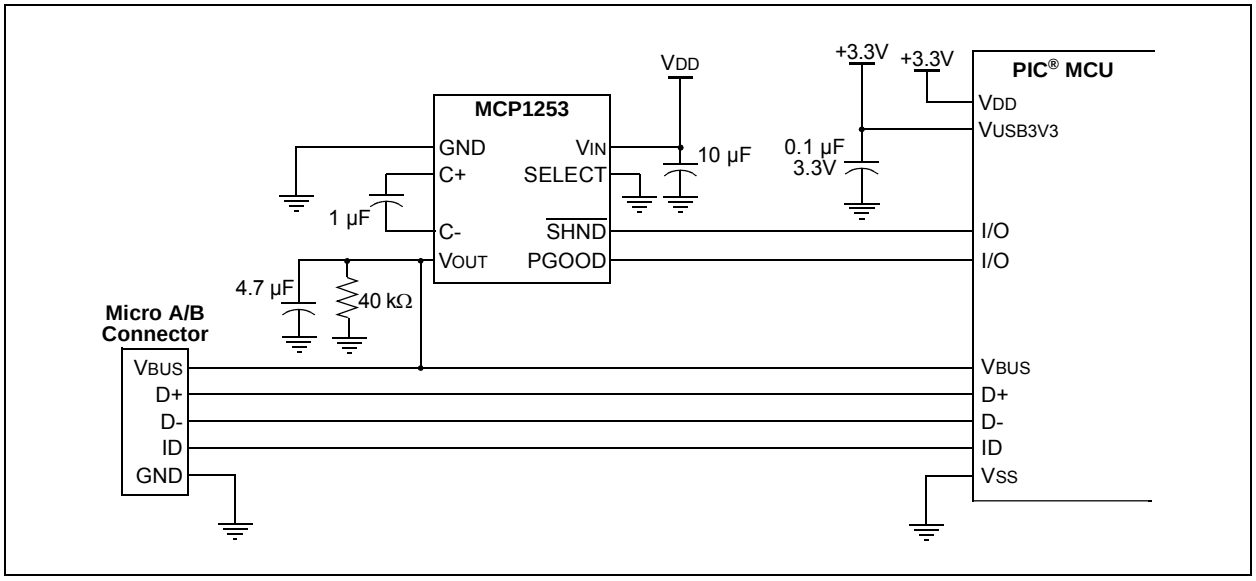


FIGURE 19-6: USB OTG INTERFACE EXAMPLE



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19.7.3 USB ENDPOINT MANAGEMENT REGISTERS

REGISTER 19-21: U1EPn: USB ENDPOINT n CONTROL REGISTERS (n = 0 TO 15)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
LSPD(1)	RETRYDIS(1)	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **LSPD:** Low-Speed Direct Connection Enable bit (U1EP0 only)(1)
- 1 = Direct connection to a low-speed device is enabled
- 0 = Direct connection to a low-speed device is disabled

bit 6 **RETRYDIS:** Retry Disable bit (U1EP0 only)(1)
- 1 = Retry NAK transactions are disabled
- 0 = Retry NAK transactions are enabled; retry is done in hardware

bit 5 **Unimplemented:** Read as '0'

bit 4 **EPCONDIS:** Bidirectional Endpoint Control bit

If EPTXEN and EPRXEN = 1:
- 1 = Disables Endpoint n from control transfers; only TX and RX transfers are allowed
- 0 = Enables Endpoint n for control (SETUP) transfers; TX and RX transfers are also allowed

For All Other Combinations of EPTXEN and EPRXEN:
This bit is ignored.

bit 3 **EPRXEN:** Endpoint Receive Enable bit
- 1 = Endpoint n receive is enabled
- 0 = Endpoint n receive is disabled

bit 2 **EPTXEN:** Endpoint Transmit Enable bit
- 1 = Endpoint n transmit is enabled
- 0 = Endpoint n transmit is disabled

bit 1 **EPSTALL:** Endpoint STALL Status bit
- 1 = Endpoint n was stalled
- 0 = Endpoint n was not stalled

bit 0 **EPHSHK:** Endpoint Handshake Enable bit
- 1 = Endpoint handshake is enabled
- 0 = Endpoint handshake is disabled (typically used for isochronous endpoints)

Note 1: These bits are available only for U1EP0 and only in Host mode. For all other U1EPn registers, these bits are always unimplemented and read as '0'.

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20.0 DATA SIGNAL MODULATOR

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"Data Signal Modulator (DSM)"** (DS39744) which is available from the Microchip web site (www.microchip.com). The information in this data sheet supersedes the information in the FRM.

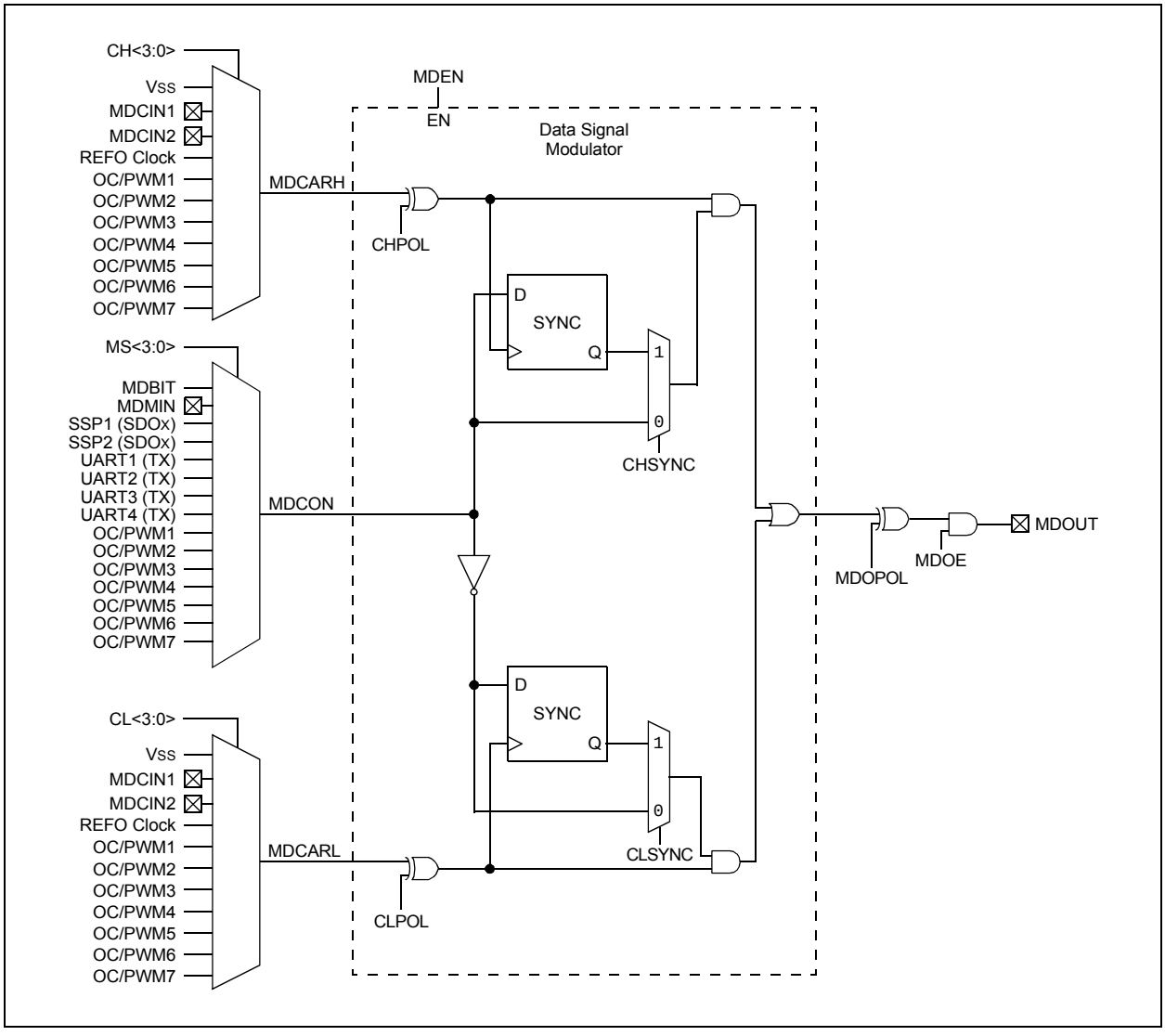
The Data Signal Modulator (DSM) allows the user to mix a digital data stream (the "modulator signal") with a carrier signal to produce a modulated output. Both the carrier and the modulator signals are supplied to the DSM module, either internally from the output of a peripheral, or externally through an input pin.

The modulated output signal is generated by performing a logical AND operation of both the carrier and modulator signals and then it is provided to the MDOUT pin. Using this method, the DSM can generate the following types of key modulation schemes:

- Frequency Shift Keying (FSK)
- Phase-Shift Keying (PSK)
- On-Off Keying (OOK)

Figure 20-1 shows a simplified block diagram of the Data Signal Modulator peripheral.

FIGURE 20-1: SIMPLIFIED BLOCK DIAGRAM OF THE DATA SIGNAL MODULATOR



NOTES:

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23.0 REAL-TIME CLOCK AND CALENDAR (RTCC)

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the Real-Time Clock and Calendar, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"RTCC with External Power Control"** (DS39745) which is available from the Microchip web site (www.microchip.com). The information in this data sheet supersedes the information in the FRM.

The RTCC provides the user with a Real-Time Clock and Calendar (RTCC) function that can be calibrated.

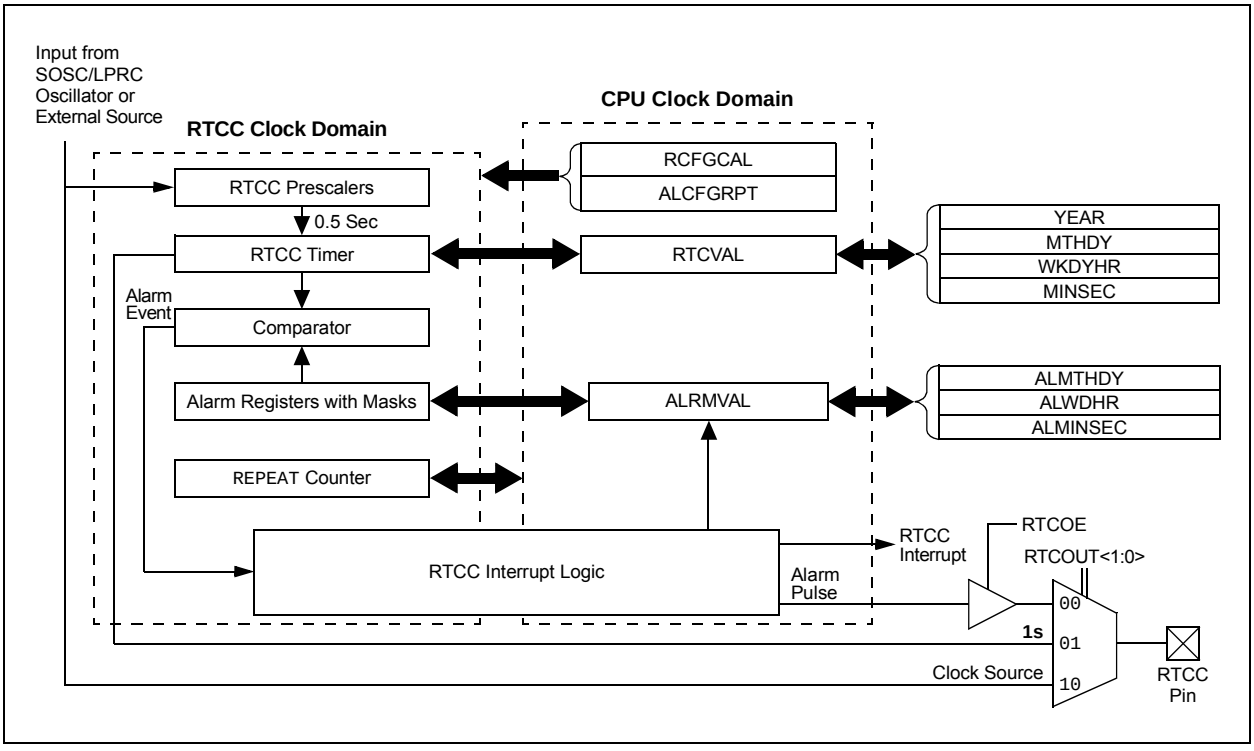
Key features of the RTCC module are:

- Operates in Deep Sleep mode
- Selectable Clock Source
- Provides Hours, Minutes and Seconds Using 24-Hour Format
- Visibility of One Half Second Period
- Provides Calendar – Weekday, Date, Month and Year
- Alarm-Configurable for Half a Second, One Second, Ten Seconds, One Minute, Ten Minutes, One Hour, One Day, One Week, One Month or One Year
- Alarm Repeat with Decrementing Counter
- Alarm with Indefinite Repeat Chime
- Year 2000 to 2099 Leap Year Correction
- BCD Format for Smaller Software Overhead
- Optimized for Long-Term Battery Operation
- User Calibration of the 32.768 kHz Clock Crystal/32K INTRC Frequency with Periodic Auto-Adjust
- Optimized for Long-Term Battery Operation
- Fractional Second Synchronization
- Calibration to within ±2.64 Seconds Error per Month
- Calibrates up to 260 ppm of Crystal Error
- Ability to Periodically Wake-up External Devices without CPU Intervention (external power control)
- Power Control Output for External Circuit Control
- Calibration takes Effect Every 15 Seconds
- Runs from Any One of the Following:
  - External Real-Time Clock (RTC) of 32.768 kHz
  - Internal 31.25 kHz LPRC clock
  - 50 Hz or 60 Hz external input

23.1 RTCC Source Clock

The user can select between the SOSC crystal oscillator, LPRC internal oscillator or an external 50 Hz/60 Hz power line input as the clock reference for the RTCC module. This gives the user an option to trade off system cost, accuracy and power consumption, based on the overall system needs.

FIGURE 23-1: RTCC BLOCK DIAGRAM



REGISTER 23-3: ALCFGRPT: ALARM CONFIGURATION REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ALRMEN	CHIME	AMASK3	AMASK2	AMASK1	AMASK0	ALRMPTR1	ALRMPTR0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ARPT7	ARPT6	ARPT5	ARPT4	ARPT3	ARPT2	ARPT1	ARPT0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ALRMEN:** Alarm Enable bit

1 = Alarm is enabled (cleared automatically after an alarm event whenever ARPT<7:0> = 00h and CHIME = 0)
0 = Alarm is disabled

bit 14 **CHIME:** Chime Enable bit

1 = Chime is enabled; ARPT<7:0> bits are allowed to roll over from 00h to FFh
0 = Chime is disabled; ARPT<7:0> bits stop once they reach 00h

bit 13-10 **AMASK<3:0>:** Alarm Mask Configuration bits

0000 = Every half second
0001 = Every second
0010 = Every 10 seconds
0011 = Every minute
0100 = Every 10 minutes
0101 = Every hour
0110 = Once a day
0111 = Once a week
1000 = Once a month
1001 = Once a year (except when configured for February 29th, once every 4 years)
101x = Reserved – do not use
11xx = Reserved – do not use

bit 9-8 **ALRMPTR<1:0>:** Alarm Value Register Window Pointer bits

Points to the corresponding Alarm Value registers when reading the ALRMVALH and ALRMVALL registers. The ALRMPTR<1:0> value decrements on every read or write of ALRMVALH until it reaches '00'.

ALRMVAL<15:8>:
00 = ALRMMIN
01 = ALRMWD
10 = ALRMMNTH
11 = Unimplemented

ALRMVAL<7:0>:
00 = ALRMSEC
01 = ALRMHR
10 = ALRMDAY
11 = Unimplemented

bit 7-0 **ARPT<7:0>:** Alarm Repeat Counter Value bits

11111111 = Alarm will repeat 255 more times
•
•
•
00000000 = Alarm will not repeat

The counter decrements on any alarm event; it is prevented from rolling over from 00h to FFh unless CHIME = 1.

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REGISTER 26-2: ADCON2: A/D CONTROL REGISTER 2

R/W-0	R/W-0	U-0	R/W-0	U-0	R/W-0	r-1	r-1
PVCFG1	PVCFG0	—	NVCFG0	—	BUFORG	—	—
bit 15							bit 8

r-0	r-0	U-0	U-0	U-0	U-0	R/W-0	r-0
—	—	—	—	—	—	RFPUMP	—
bit 7							bit 0

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **PVCFG<1:0>:** Converter Voltage Reference Configuration for ADREF+ bits
10 = BGBUF1 Internal Reference(1)
01 = External VREF+
00 = AVDD

bit 13 **Unimplemented:** Read as '0'

bit 12 **NVCFG0:** Converter Voltage Reference Configuration for ADREF- bit
1 = External VREF-
0 = AVSS

bit 11 **Unimplemented:** Read as '0'

bit 10 **BUFORG:** ADRES Result Buffer Organization Control bit
1 = Result buffer is organized as an indexed buffer; ADTBLn conversion result is stored in ADRESn (where n is the same number between 0-31)
0 = Result buffer is organized as a 32 result deep FIFO-like buffer; results get stored in the sequential order that they are generated

bit 9-8 **Reserved:** Always write '11' to these bits for normal A/D operation

bit 7-6 **Reserved:** Always write '00' to these bits for normal A/D operation

bit 5-2 **Unimplemented:** Read as '0'

bit 1 **RFPUMP:** Internal Reference Bias Control bit
1 = Internal bias is optimized for operation with small reference voltage (e.g., < (0.65 * AVDD))
0 = Normal operating mode

bit 0 **Reserved:** Always write '0' to this bit for normal A/D operation

Note 1: In order to use the BGBUF1 internal reference for the A/D, firmware must also configure and enable the buffer through the BUFCON1 register.

REGISTER 27-2: SD1CON2: S/D CONTROL REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
CHOP1	CHOP0	SDINT1	SDINT0	—	—	SDWM1	SDWM0
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	U-0	U-0	HS/C-0
—	—	—	RNDRES1	RNDRES0	—	—	SDRDY
bit 7							bit 0

Legend:	C = Clearable bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **CHOP<1:0>:** Chopping Enable bits
11 = Chopping is enabled (recommended setting, improves result quality)
10 = Reserved
01 = Reserved
00 = Chopping is disabled

bit 13-12 **SDINT<1:0>:** S/D Interrupt Event Generation Select bits
11 = Interrupt on every sample clock
10 = Interrupt on every fifth sample clock
01 = Interrupt when New Result < Old Result
00 = Interrupt when New Result > Old Result

bit 11-10 **Unimplemented:** Read as '0'

bit 9-8 **SDWM<1:0>:** S/D Output Result Register Write bits
11 = Reserved; do not use
10 = SD1RESH/SD1RESL are never updated (used for threshold compare operations)
01 = SD1RESH/SD1RESL are updated on every interrupt
00 = SD1RESH/SD1RESL are updated on every interrupt when SDRDY = 0

bit 7-5 **Unimplemented:** Read as '0'

bit 4-3 **RNDRES<1:0>:** Round Data Control bits
11 = Round result to 8 bits
10 = Round result to 16 bits
01 = Round result to 24 bits
00 = No rounding

bit 2-1 **Unimplemented:** Read as '0'

bit 0 **SDRDY:** S/D Filter Data Ready bit (set by hardware)
1 = Sync filter delay is satisfied (clear this bit in software)
0 = Sync filter delay is not satisfied yet

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TABLE 37-7: DC CHARACTERISTICS: ∆ CURRENT (BOR, WDT, DSBOR, DSWDT, LCD)

DC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial			
Parameter No.	**Typical(1)**	**Max**	**Units**	**Operating Temperature**	**VDD**	**Conditions**
Incremental Current Brown-out Reset (∆BOR)(2)						
DC25	3.1	5.0	µA	-40°C to +85°C	2.0V	∆BOR(2)
	4.3	6.0	µA	-40°C to +85°C	3.3V	
Incremental Current Watchdog Timer (∆WDT)(2)						
DC71	0.8	1.5	µA	-40°C to +85°C	2.0V	∆WDT (with LPRC selected)(2)
	0.8	1.5	µA	-40°C to +85°C	3.3V	
Incremental Current HLVD (∆HLVD)(2)						
DC75	4.2	15	µA	-40°C to +85°C	2.0V	∆HLVD(2)
	4.2	15	µA	-40°C to +85°C	3.3V	
Incremental Current Real-Time Clock and Calendar (∆RTCC)(2)						
DC77	0.30	1.0	µA	-40°C to +85°C	2.0V	∆RTCC (with SOSC)(2)
	0.35	1.0	µA	-40°C to +85°C	3.3V	
DC77a	0.30	1.0	µA	-40°C to +85°C	2.0V	∆RTCC (with LPRC)(2)
	0.35	1.0	µA	-40°C to +85°C	3.3V	
Incremental Current Deep Sleep BOR (∆DSBOR)(2)						
DC81	0.11	0.40	µA	-40°C to +85°C	2.0V	∆Deep Sleep BOR(2)
	0.12	0.40	µA	-40°C to +85°C	3.3V	
Incremental Current Deep Sleep Watchdog Timer Reset (∆DSWDT)(2)						
DC80	0.24	0.40	µA	-40°C to +85°C	2.0V	∆Deep Sleep WDT(2)
	0.24	0.40	µA	-40°C to +85°C	3.3V	
Incremental Current LCD (∆LCD)(2)						
DC82	0.8	3.0	µA	-40°C to +85°C	3.3V	∆LCD external/internal;(2,3) 1/8 MUX, 1/3 Bias
DC90	20	—	µA	-40°C to +85°C	2.0V	∆LCD charge pump;(2,4) 1/8 MUX, 1/3 Bias
	24	—	µA	-40°C to +85°C	3.3V	
VBAT A/D Monitor(5)						
DC91	1.5	—	µA	-40°C to +85°C	3.3V	VBAT = 2V
	4.0	—	µA	-40°C to +85°C	3.3V	VBAT = 3.3V

Note 1: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: Incremental current while the module is enabled and running.

3: LCD is enabled and running, no glass is connected; the resistor ladder current is not included.

4: LCD is enabled and running, no glass is connected.

5: The A/D channel is connected to the VBAT pin internally; this is the current during A/D VBAT operation.

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FIGURE 38-41: 12-BIT PIPELINE A/D INL vs. TEMPERATURE

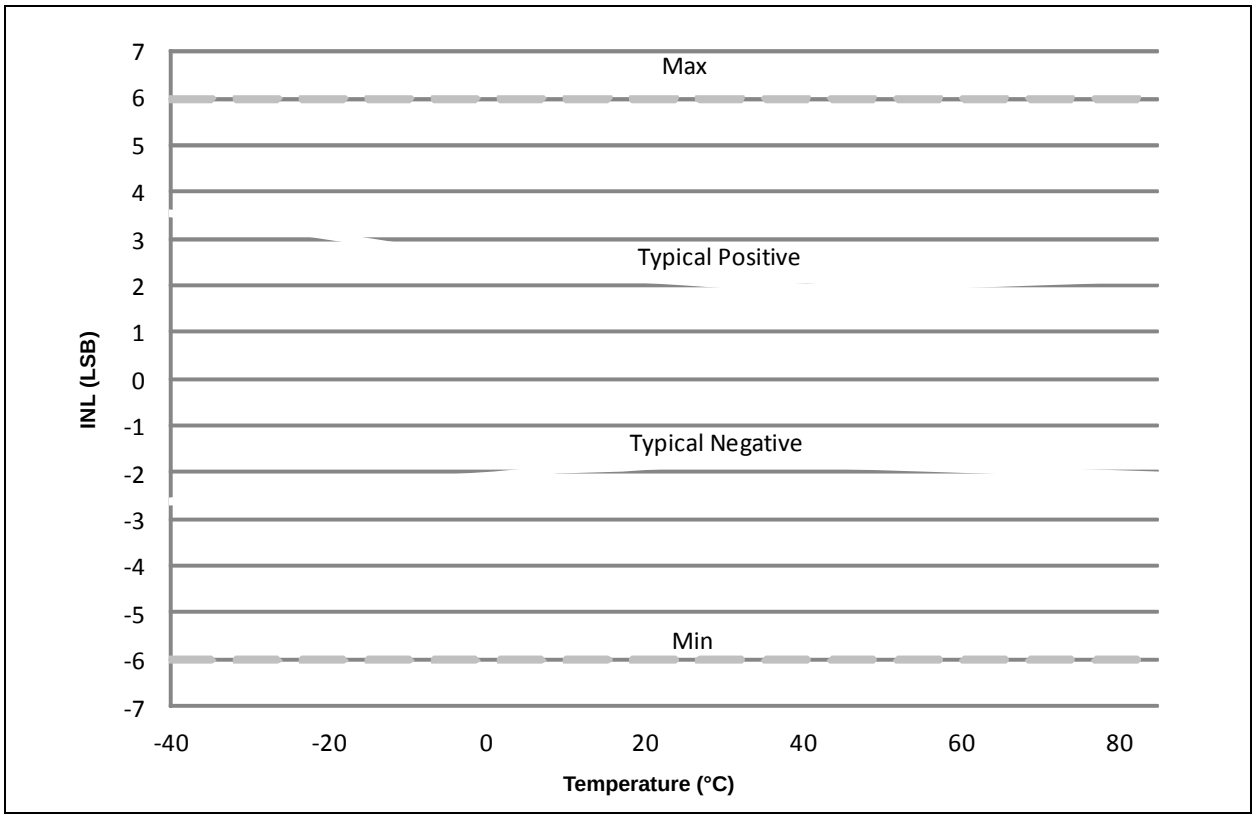
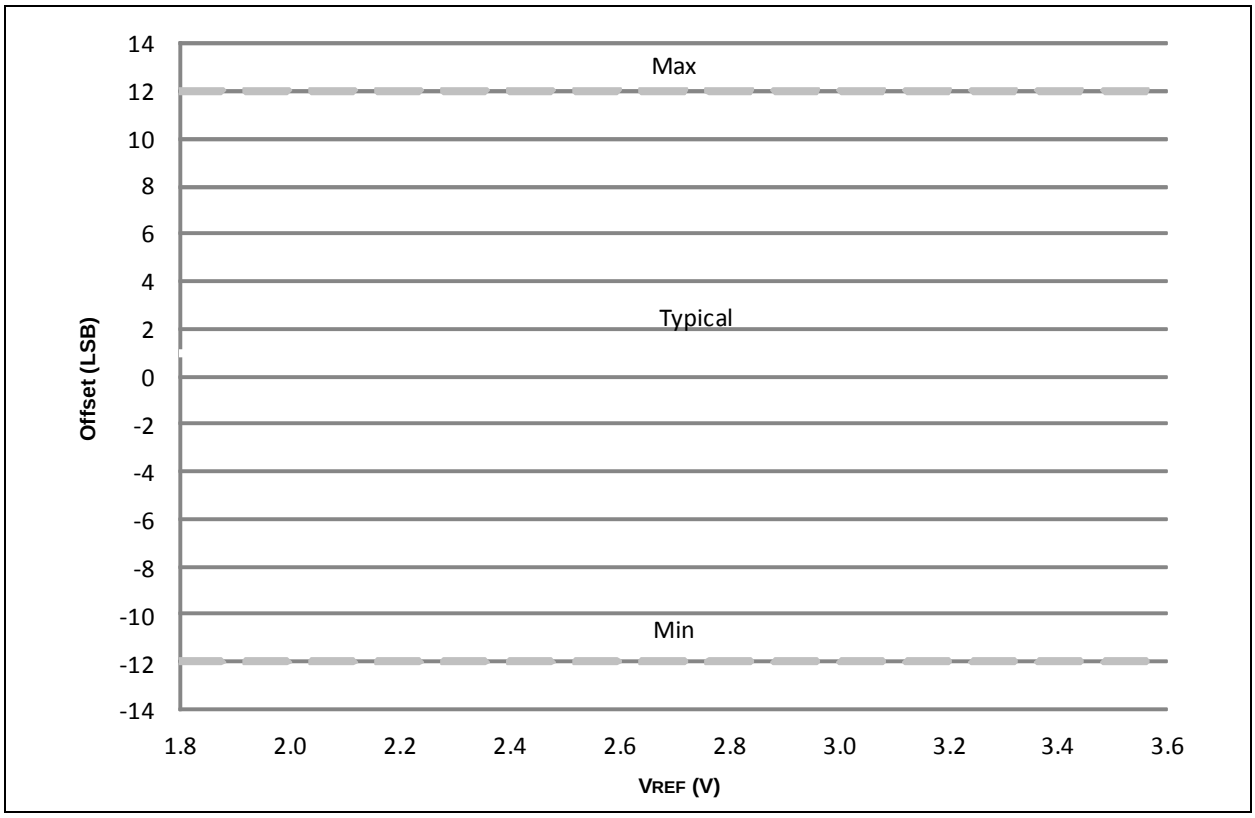


FIGURE 38-42: 12-BIT PIPELINE A/D OFFSET vs. VREF



APPENDIX A: REVISION HISTORY

Revision A (July 2012)

Original data sheet for the PIC24FJ128GC010 family of devices.

Revision B (May 2013)

Changes descriptive title on Page 1 to “16-Bit Flash Microcontrollers with 12-Bit Pipeline A/D, Sigma-Delta A/D, USB On-The-Go and XLP Technology”.

Adds CoreMark® rating to the **“High-Performance CPU”** section on Page 2.

Removes all references to JTAG device programming throughout the document.

Corrects the default Doze mode ratio as 1:8 (previously described as 1:1) throughout the document.

Corrects the default FRC postscaler setting to 1:2.

Corrects references in **Section 10.4.6 “Deep Sleep WDT”** regarding the Configuration register for the DSWDTOSC and DSWDPS<4:0> bits.

Changes the description of the behavior of the UERRIF bit in the U1IR register, from “Read-Only” to “Read, Write 1 to Clear”, in both contexts of the register.

Corrects the low end of the operating range of the voltage regulator, described in **Section 34.2 “On-Chip Voltage Regulator”**, to 2.0V.

Updates **Section 37.0 “Electrical Characteristics”**:

- Adds maximum specifications to most DC Specifications
- Adds systematic parameter numbers to existing DC and AC Specifications that were previously not numbered
- Moves DC Specification for USB module from Table 37-4 to a new Table 37-15; all subsequent tables are renumbered accordingly
- Updates most typical and maximum specifications in the following tables:
  - Table 37-12 (Band Gap Reference (BGBUFn) Specifications)
  - Table 37-19 (Operational Amplifier Specifications)
  - Table 37-28 (12-bit Pipeline A/D Module Specifications)
  - Table 37-30 (10-Bit DAC Specifications)
  - Table 37-31 (16-Bit Sigma-Delta A/D Converter Specifications)

Other minor typographic changes and updates throughout.

Revision C (October 2014)

Adds PWRLCLK pin function description to **Section 1.0 “Device Overview”**.

Updates suitable capacitor requirements in **Section 2.2 “Power Supply Pins”**.

Updates Figure 9-1 (PIC24FJ128GC010 Family Clock Diagram.

Updates the code in Example 10-2 (Deep Sleep Sequence) and adds code in Example 10-3 (Entering and Exiting Doze Mode).

Adds Register 11-8 (ANCFG: Analog Configuration).

Adds **Section 32.4 “Measuring Die Temperature”**.

Updates values in DI30 and DI30a in Table 37-9.

Adds DCT22, DCT23 and DCT24 rows to Table 37-14.

Adds **Section 38.0 “DC and AC Device Characteristics Graphs”**.

Updates some of the diagrams in **Section 39.0 “Packaging Information”**.

Other minor typographic changes and updates throughout the document.

Revision D (December 2016)

Updates Pin 12 and 14 in Table 1.

Adds CH1SE to Table 1-3 (PIC24FJ128GC010 Family Pinout Description).

Updates Table 9-1 (PIC24FJ128GC010 Family Clock Diagram).

Removes original Note 2 reference from Table 10-2 (Exiting Power-Saving Modes).

Removes original Note 1 reference and updates the description for RFPUMP in Register 26-2 (ADCON2: A/D Control Register 2).

Removes additional Minimum and Maximum data from Table 37-28 (12-Bit Pipeline A/D Module Specifications).