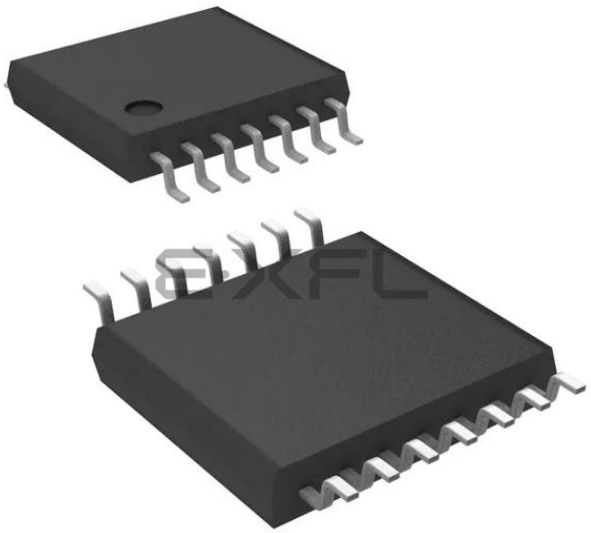

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	11
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	14-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	14-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l011d3p6

2.1 Device overview

Table 2. Ultra-low-power STM32L011x3/x4 device features and peripheral counts

Peripheral		STM32 L011D3	STM32 L011F3	STM32 L011E3	STM32 L011G3	STM32 L011K3	STM32 L011D4	STM32 L011F4	STM32 L011E4	STM32 L011G4	STM32 L011K4
Flash (Kbytes)		8					16				
Data EEPROM (bytes)		512									
RAM (Kbytes)		2									
Timers	General-purpose	2									
	LPTIM	1									
RTC/SYSTICK/IWDG/ WWDG		1/1/1/1									
Communi-cation interfaces	SPI	1									
	I^2C	1									
	USART	1									
	LPUART	1									
GPIOs		11	16	21	24	26/28(1)	11	16	21	24	26/28(1)
Clocks: HSE(2)/LSE/HSI/MSI/LSI		1/1/1/1/1									
12b synchronized ADC Number of channels		1 4	1 7/9(3)	1 10			1 4	1 7/9(3)	1 10		
Comparators		2									
Max. CPU frequency		32 MHz									
Operating voltage		1.8 V to 3.6 V (down to 1.65 V at power-down) with BOR option 1.65 V to 3.6 V without BOR option									
Operating temperatures		Ambient temperature: –40 to +125 °C Junction temperature: –40 to +130 °C									
Packages		TSSOP 14	TSSOP/ UFQFPN 20	WLCSP 25	UFQFPN 28	LQFP/ UFQFPN 32	TSSOP 14	TSSOP/ UFQFPN 20	WLCSP 25	UFQFPN 28	LQFP/, UFQFPN 32

1. The devices feature 26 and 28 GPIOs on LQFP32 and UFQFPN32, respectively.
2. HSE available only as external clock input (HSE bypass).
3. The devices feature 7 and 9 ADC channels on UFQFPN20 and TSSOP20, respectively.

Figure 1. STM32L011x3/4 block diagram

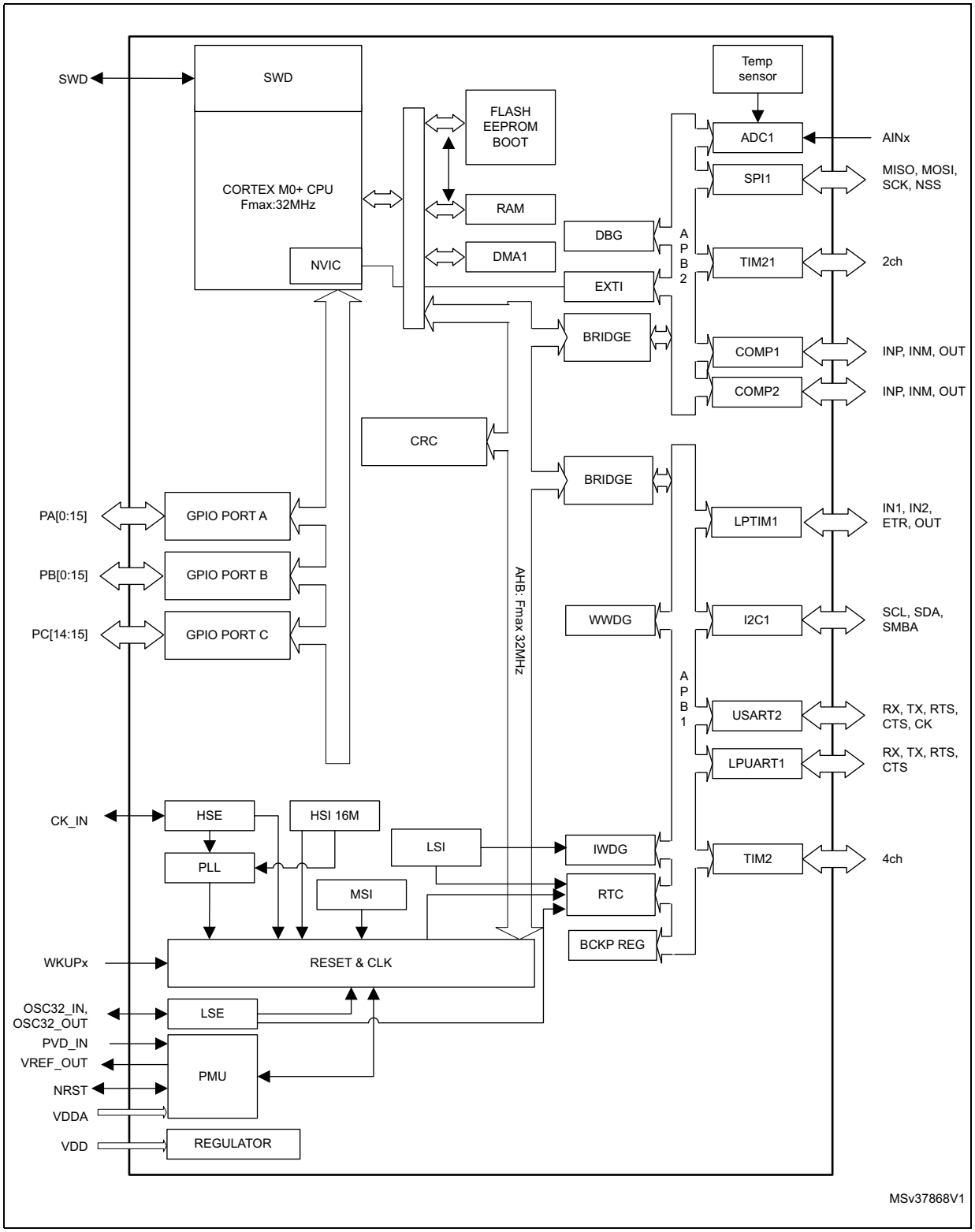


Table 5. Functionalities depending on the working mode (from Run/active down to standby) (continued)[1][2]

IPs	Run/Active	Sleep	Low-power run	Low-power sleep	Stop		Standby	
						Wakeup capability		Wakeup capability
Programmable Voltage Detector (PVD)	O	O	O	O	O	O	-	-
Power-on/down reset (POR/PDR)	Y	Y	Y	Y	Y	Y	Y	Y
High Speed Internal (HSI)	O	O	-	-	[3]	-	-	-
High Speed External (HSE)	O	O	O	O	-	-	-	-
Low Speed Internal (LSI)	O	O	O	O	O	-	O	-
Low Speed External (LSE)	O	O	O	O	O	-	O	-
Multi-Speed Internal (MSI)	O	O	Y	Y	-	-	-	-
Inter-Connect Controller	Y	Y	Y	Y	Y	-	-	-
RTC	O	O	O	O	O	O	O	-
RTC Tamper	O	O	O	O	O	O	O	O
Auto WakeUp (AWU)	O	O	O	O	O	-	O	O
USART	O	O	O	O	O[4]	O	-	-
LPUART	O	O	O	O	O[4]	O	-	-
SPI	O	O	O	O	-		-	-
I2C	O	O	O	O	O[5]	O	-	-
ADC	O	O	-	-	-	-	-	-
Temperature sensor	O	O	O	O	O	-	-	-
Comparators	O	O	O	O	O	O	-	-
16-bit timers	O	O	O	O	-	-	-	-
LPTIM	O	O	O	O	O	O	-	-
IWDG	O	O	O	O	O	O	O	O
WWDG	O	O	O	O	-	-	-	-
SysTick Timer	O	O	O	O	-	-	-	-
GPIOs	O	O	O	O	O	O	-	2 pins

(rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 38 GPIOs can be connected to the 16 configurable interrupt/event lines. The 10 other lines are connected to PVD, RTC, USART, I2C, LPUART, LPTIM or comparator events.

3.8 Memories

The STM32L011x3/4 devices have the following features:

- 2 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states. With the enhanced bus matrix, operating the RAM does not lead to any performance penalty during accesses to the system bus (AHB and APB buses).
- The non-volatile memory is divided into three arrays:
  - 8 or 16 Kbytes of embedded Flash program memory
  - 512 bytes of data EEPROM
  - Information block containing 32 user and factory options bytes plus 4 Kbytes of system memory

The user options bytes are used to write-protect or read-out protect the memory (with 4 Kbyte granularity) and/or readout-protect the whole memory with the following options:

- **Level 0**: no protection
- **Level 1**: memory readout protected.

  The Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
- **Level 2**: chip readout protected, debug features (Cortex-M0+ serial wire) and boot in RAM selection disabled (debugline fuse)

The whole non-volatile memory embeds the error correction code (ECC) feature.

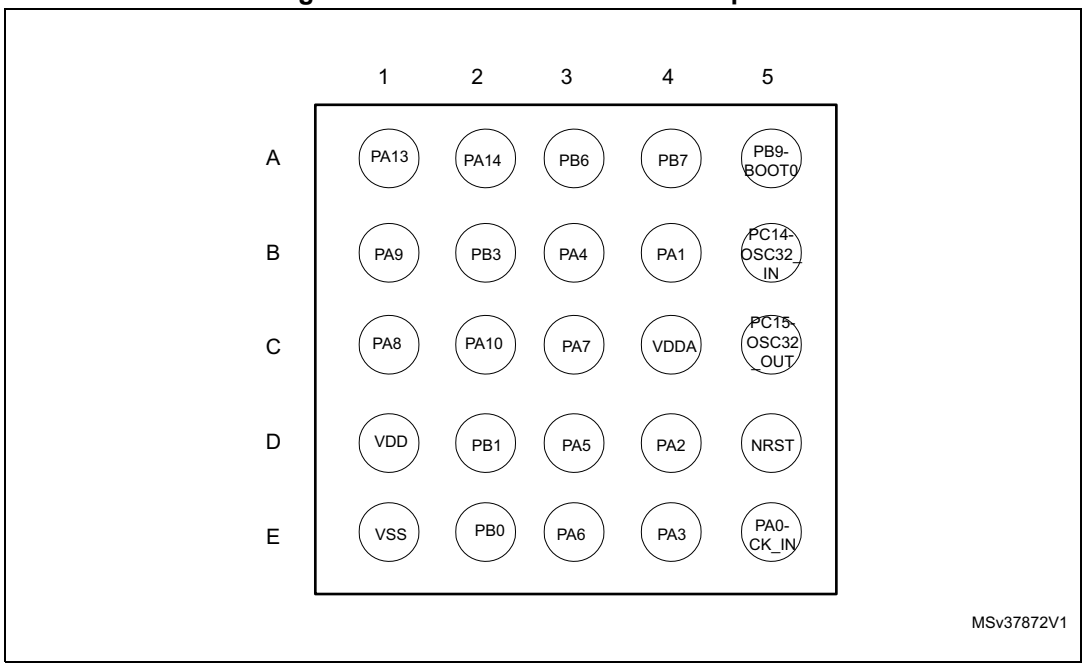
3.9 Direct memory access (DMA)

The flexible 5-channel, general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

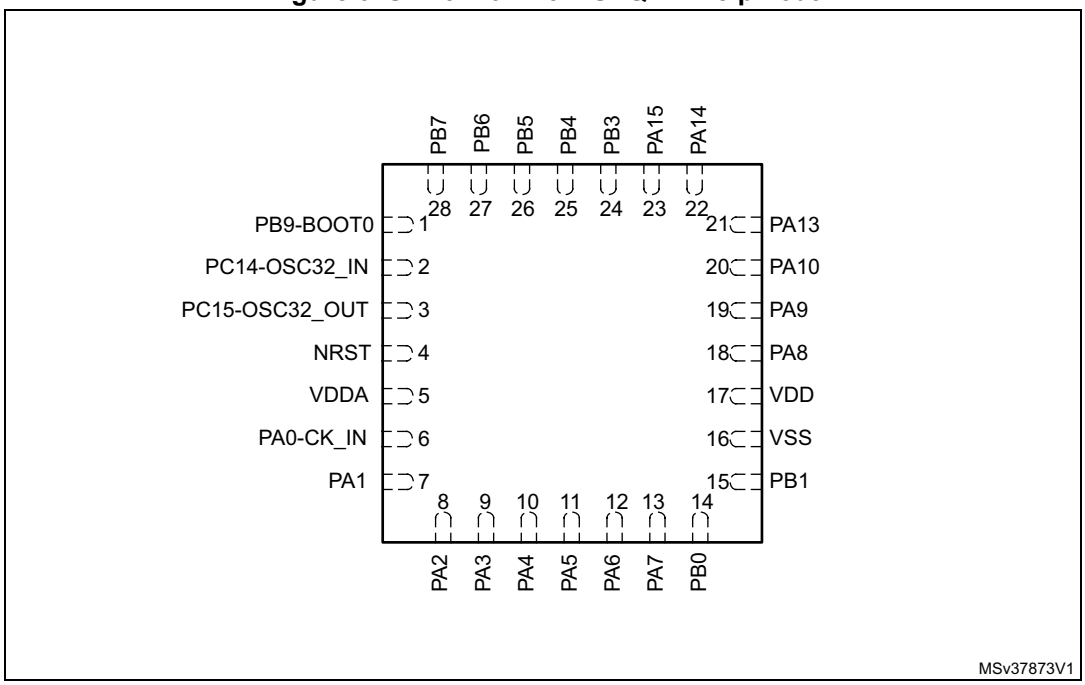
The DMA can be used with the main peripherals: SPI, I^2C, USART, LPUART, general-purpose timers, and ADC.

Figure 5. STM32L011x3/4 WLCSP25 pinout



1. The above figure shows the package top view.

Figure 6. STM32L011x3/4 UFQFPN28 pinout



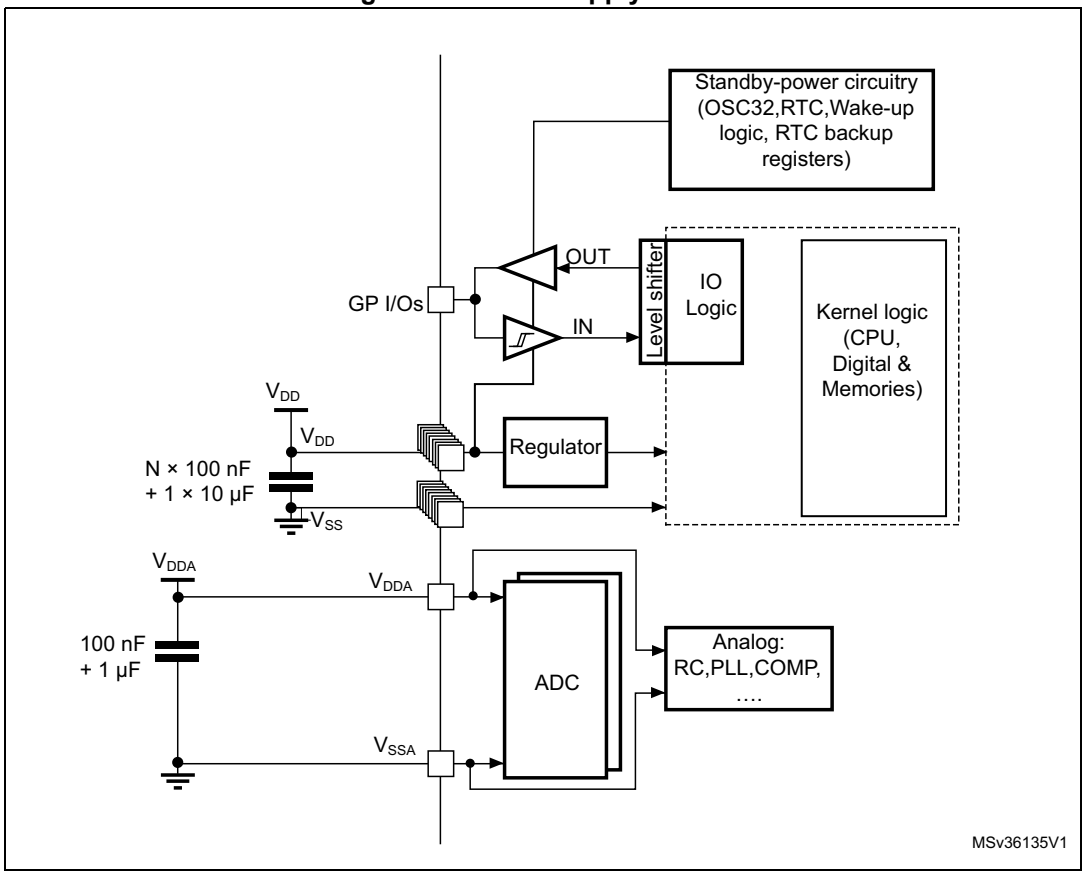
1. The above figure shows the package top view.

Table 13. Pin definitions

Pin number							Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
TSSOP14	UFQFPN20	TSSOP20	UFQFPN28	LQFP32	UFQFPN32[1]	WLCSP25					Alternate functions	Additional functions
2	1	2	2	2	2	B5	PC14-OSC32_IN	I/O	FT	-	-	OSC32_IN
3	2	3	3	3	3	C5	PC15-OSC32_OUT	I/O	TC	-	-	OSC32_OUT
4	3	4	4	4	4	D5	NRST	I/O	RST	(2)	-	-
10	4	5	5	5	5	C4	VDDA	S	-	(3)(4)	-	-
5	5	6	6	6	6	E5	PA0-CK_IN	I/O	TTa	-	USART2_RX, LPTIM1_IN1, TIM2_CH1, USART2_CTS, TIM2_ETR, LPUART1_RX, COMP1_OUT	COMP1_INM, ADC_IN0, RTC_TAMP2/WKUP1/CK_IN
6	6	7	7	7	7	B4	PA1	I/O	FT	-	EVENTOUT, LPTIM1_IN2, TIM2_CH2, I2C1_SMBA, USART2_RTS, TIM21_ETR, LPUART1_TX	COMP1_INP, ADC_IN1
-	-	8	8	8	8	D4	PA2	I/O	TTa	-	TIM21_CH1, TIM2_CH3, USART2_TX, LPUART1_TX, COMP2_OUT	COMP2_INM, ADC_IN2, RTC_TAMP3/RTC_TS/RTC_OUT/WKUP3
-	-	9	9	9	9	E4	PA3	I/O	FT	-	TIM21_CH2, TIM2_CH4, USART2_RX, LPUART1_RX	COMP2_INP, ADC_IN3
7	7	10	10	10	10	B3	PA4	I/O	TTa	-	SPI1_NSS, LPTIM1_IN1, LPTIM1_ETR, I2C1_SCL, USART2_CK, TIM2_ETR, LPUART1_TX, COMP2_OUT	COMP1_INM, COMP2_INM, ADC_IN4

6.1.6 Power supply scheme

Figure 13. Power supply scheme



1. On TSSOP14 package, V_{DDA} is internally connected to V_{DD}.
2. V_{SSA} is internally connected to V_{SS} on all packages.

6.1.7 Current consumption measurement

Figure 14. Current consumption measurement scheme

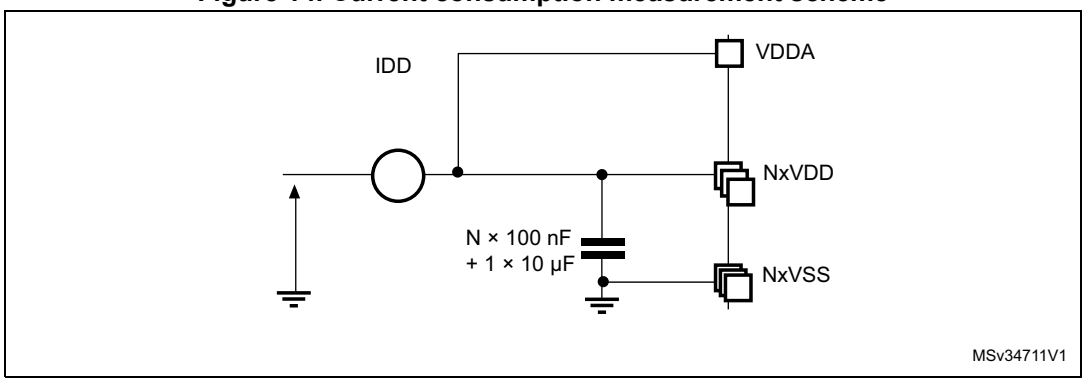


Table 27. Current consumption in Low-power Run mode

Symbol	Parameter	Conditions			Typ	Max(1)	Unit
I_{DD} (LP Run)	Supply current in Low-power run mode	All peripherals OFF, code executed from RAM, Flash switched OFF, V_{DD} from 1.65 V to 3.6 V	MSI clock, 65 kHz f_{HCLK} = 32 kHz	T_A = -40 °C to 25 °C	5.7	8.1	µA
				T_A = 85 °C	6.5	9	
				T_A = 105 °C	8	13	
				T_A = 125 °C	11.5	22	
			MSI clock, 65 kHz f_{HCLK} = 65 kHz	T_A =-40 °C to 25 °C	8.7	11	
				T_A = 85 °C	9.5	12	
				T_A = 105 °C	11	15	
				T_A = 125 °C	15	24	
			MSI clock, 131 kHz f_{HCLK} = 131 kHz	T_A = -40 °C to 25 °C	17	19	
				T_A = 55 °C	17	19.5	
				T_A = 85 °C	17.5	20	
				T_A = 105 °C	19	22	
				T_A = 125 °C	22.5	31	
		All peripherals OFF, code executed from Flash, V_{DD} from 1.65 V to 3.6 V	MSI clock, 65 kHz f_{HCLK} = 32 kHz	T_A = -40 °C to 25 °C	18	22	
				T_A = 85 °C	20	24	
				T_A = 105 °C	22	27	
				T_A = 125 °C	26.5	37	
			MSI clock, 65 kHz f_{HCLK} = 65 kHz	T_A = -40 °C to 25 °C	22	25	
				T_A = 85 °C	24	27	
				T_A = 105 °C	26	30	
				T_A = 125 °C	30.5	39	
			MSI clock, 131 kHz f_{HCLK} = 131 kHz	T_A = -40 °C to 25 °C	32	34	
				T_A = 55 °C	32.5	35	
				T_A = 85 °C	34	37	
				T_A = 105 °C	36	39	
				T_A = 125 °C	40	47	

1. Guaranteed by characterization results at 125 °C, not tested in production, unless otherwise specified.

Table 32. Peripheral current consumption in run or Sleep mode(1)

Peripheral		Typical consumption, V_{DD} = 3.0 V, T_A = 25 °C				Unit
		Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	Low-power sleep and run	
APB1	WWDG	2.5	2	1.6	2	µA/MHz (f_{HCLK})
	LPUART1	8.3	7.2	5.4	7.2	
	I2C1	11	8.2	6.8	8.9	
	LPTIM1	14	11	8.7	11	
	TIM2	10.5	8.5	6.4	8.5	
	USART2	8.5	6.8	5.4	7.1	
APB2	ADC1(2)	5.0	3.9	3.3	4	µA/MHz (f_{HCLK})
	SPI1	4.5	3.5	2.9	3.6	
	TIM21	6.8	6.1	4.5	5.6	
	DBGMCU	1.7	1.7	1.1	1.4	
	SYSCFG/ COMP	2.5	2.4	1.6	2.3	
Cortex-M0+ core I/O port	GPIOA	7.6	6.3	4.9	6.5	µA/MHz (f_{HCLK})
	GPIOB	5.1	4.1	3.2	4	
	GPIOC	1.1	0.7	0.6	0.8	
AHB	CRC	1.5	1.1	1	1.2	µA/MHz (f_{HCLK})
	FLASH(3)	10	8.5	7	8.5	
	DMA1	5.3	4.2	3.5	4.8	
All enabled		96	80	62	88	
PWR		2.1	1.9	1.4	1.8	µA/MHz (f_{HCLK})

1. Data based on differential I_{DD} measurement between all peripherals OFF an one peripheral with clock enabled, in the following conditions: f_{HCLK} = 32 MHz (range 1), f_{HCLK} = 16 MHz (range 2), f_{HCLK} = 4 MHz (range 3), f_{HCLK} = 64kHz (Low-power run/sleep), $f_{APB1} = f_{HCLK}$, $f_{APB2} = f_{HCLK}$, default prescaler value for each peripheral. The CPU is in Sleep mode in both cases. No I/O pins toggling. Not tested in production.
2. HSI oscillator is OFF for this measure.
3. These values correspond to the Flash memory dynamic current consumption. The Flash memory static consumption (Flash memory ON) equals 12 µA and does not depend on the frequency.
The Flash memory consumption is already taken into account in all the supply current consumption tables (Flash memory ON cases).

Table 33. Peripheral current consumption in Stop and Standby mode

Symbol	Peripheral	Typical consumption, T_A = 25 °C		Unit
		V_{DD}=1.8 V	V_{DD}=3.0 V	
$I_{DD(PVD / BOR)}$	-	0.6	1	µA
I_{REFINT}	-	1.25	1.3	
-	LSE Low drive	0.11	0.16	
-	LPTIM1, Input 100 Hz	0.01	0.02	
-	LPTIM1, Input 1 MHz	8	9	
-	LPUART1	0.025	0.027	
-	RTC	0.1	0.19	

6.3.5 Wakeup time from low-power mode

The wakeup times given in the following table are measured with the MSI or HSI16 RC oscillator. The clock source used to wake up the device depends on the current operating mode:

- Sleep mode: the clock source is the clock that was set before entering Sleep mode
- Stop mode: the clock source is either the MSI oscillator in the range configured before entering Stop mode, the HSI16 or HSI16/4.
- Standby mode: the clock source is the MSI oscillator running at 2.1 MHz

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 18*.

Table 34. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WUSLEEP}$	Wakeup from Sleep mode	f_{HCLK} = 32 MHz	7	8	CPU cycles
$t_{WUSLEEP\_LP}$	Wakeup from Low-power sleep mode, f_{HCLK} = 262 kHz	f_{HCLK} = 262 kHz Flash enabled	7	8	
		f_{HCLK} = 262 kHz Flash switched OFF	9	10	

6.3.6 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the input pin is a standard GPIO.The external clock signal has to respect the I/O characteristics in *Section 6.3.12*. However, the recommended clock input waveform is shown in *Figure 20*.

Table 35. High-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	CSS is ON or PLL is used	1	8	32	MHz
		CSS is OFF, PLL not used	0	8	32	MHz
V_{HSEH}	CK_IN input pin high level voltage	-	$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	CK_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSE)}$ $t_{w(HSE)}$	CK_IN high or low time		12	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	CK_IN rise or fall time		-	-	20	
$C_{in(HSE)}$	CK_IN input capacitance		-	2.6	-	pF
$DuCy_{(HSE)}$	Duty cycle		45	-	55	%
I_L	CK_IN Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	µA

1. Guaranteed by design, not tested in production.

Figure 20. High-speed external clock source AC timing diagram

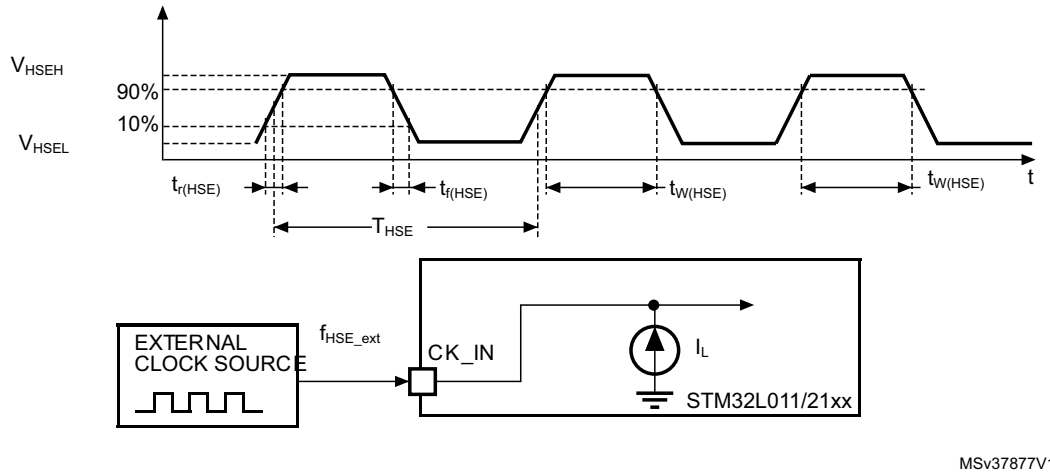


Table 40. MSI oscillator characteristics (continued)

Symbol	Parameter	Condition	Typ	Max	Unit
$t_{SU(MSI)}$	MSI oscillator startup time	MSI range 0	30	-	µs
		MSI range 1	20	-	
		MSI range 2	15	-	
		MSI range 3	10	-	
		MSI range 4	6	-	
		MSI range 5	5	-	
		MSI range 6, Voltage range 1 and 2	3.5	-	
		MSI range 6, Voltage range 3	5	-	
$t_{STAB(MSI)}$(2)	MSI oscillator stabilization time	MSI range 0	-	40	µs
		MSI range 1	-	20	
		MSI range 2	-	10	
		MSI range 3	-	4	
		MSI range 4	-	2.5	
		MSI range 5	-	2	
		MSI range 6, Voltage range 1 and 2	-	2	
		MSI range 3, Voltage range 3	-	3	
$f_{OVER(MSI)}$	MSI oscillator frequency overshoot	Any range to range 5	-	4	MHz
		Any range to range 6	-	6	

1. This is a deviation for an individual part, once the initial frequency has been measured.
2. Guaranteed by characterization results, not tested in production.

6.3.8 PLL characteristics

The parameters given in *Table 41* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 18*.

Table 41. PLL characteristics

Symbol	Parameter	Value			Unit
		Min	Typ	Max(1)	
f_{PLL_IN}	PLL input clock(2)	2	-	24	MHz
	PLL input clock duty cycle	45	-	55	%

Table 48. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +125 °C conforming to JESD78A	II level A

6.3.12 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range), or other functional failure (for example reset occurrence oscillator frequency deviation).

The test results are given in the *Table 49*.

Table 49. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on BOOT0	-0	NA	mA
	Injected current on all FT pins	-5 (1)	NA	
	Injected current on any other pin	-5 (1)	+5	

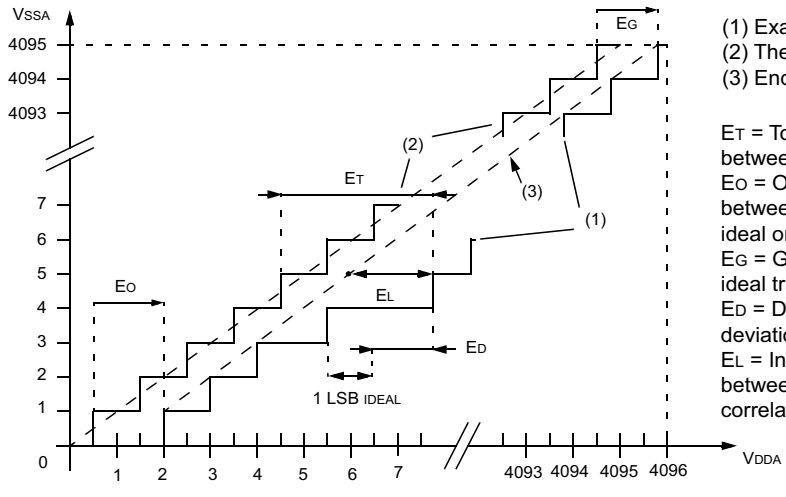
1. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

Table 56. ADC accuracy(1)(2)(3)(4)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ET	Total unadjusted error	1.65 V < V_{DDA} < 3.6 V, range 1/2/3, TSSOP14 package	-	3	5	LSB
EO	Offset error		-	2	2.5	
EG	Gain error		-	2	2.5	
EL	Integral linearity error		-	1.5	2.5	
ED	Differential linearity error		-	1	1.7	
ENOB	Effective number of bits		9.5	10.5	-	bits
	Effective number of bits (16-bit mode oversampling with ratio =256)(5)		10.7	11.6	-	
SINAD	Signal-to-noise distortion		59	65	-	dB
SNR	Signal-to-noise ratio		59	65	-	
	Signal-to-noise ratio (16-bit mode oversampling with ratio =256)(5)		66	73	-	
THD	Total harmonic distortion		-	-75	-63	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.
   Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.12* does not affect the ADC accuracy.
3. Better performance may be achieved in restricted V_{DDA}, frequency and temperature ranges.
4. In TSSOP14 package, where V_{DDA} pin is shared with V_{DD} pin, I/O toggling should be minimized to reach the values given in the above table. I/O toggling with loaded I/O pins can generate ripple on V_{DD}/V_{DDA} and degrade the ADC accuracy.
5. This number is obtained by the test board without additional noise, resulting in non-optimized value for oversampling mode.

Figure 28. ADC accuracy characteristics



(1) Example of an actual transfer curve
(2) The ideal transfer curve
(3) End point correlation line

E_T = Total Unajusted Error: maximum deviation between the actual and ideal transfer curves.
E_O = Offset Error: maximum deviation between the first actual transition and the first ideal one.
E_G = Gain Error: deviation between the last ideal transition and the last actual one.
E_D = Differential Linearity Error: maximum deviation between actual steps and the ideal ones.
E_L = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

MS19880V2

6.3.17 Comparators

Table 59. Comparator 1 characteristics

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
V_{DDA}	Analog supply voltage	-	1.65		3.6	V
R_{400K}	R_{400K} value	-	-	400	-	kΩ
R_{10K}	R_{10K} value	-	-	10	-	
V_{IN}	Comparator 1 input voltage range	-	0.6	-	V_{DDA}	V
t_{START}	Comparator startup time	-	-	7	10	µs
td	Propagation delay(2)	-	-	3	10	
V_{offset}	Comparator offset(3)	-	-	±3	±10	mV
$d_{Voffset}/dt$	Comparator offset variation in worst voltage stress conditions(3)	V_{DDA} = 3.6 V V_{IN+} = 0 V V_{IN-} = V_{REFINT} T_A = 25 °C	0	1.5	10	mV/1000 h
I_{COMP1}	Current consumption(4)	-	-	160	260	nA

1. Guaranteed by characterization, not tested in production.
2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.
3. In TSSOP14 package, where V_{DDA} pin is shared with V_{DD} pin, I/O toggling should be minimized to reach the values given in the above table. I/O toggling with loaded I/O pins can generate ripple on V_{DD}/V_{DDA} and degrade the comparator performance.
4. Comparator consumption only. Internal reference voltage not included.

Table 60. Comparator 2 characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
V_{DDA}	Analog supply voltage	-	1.65	-	3.6	V
V_{IN}	Comparator 2 input voltage range	-	0	-	V_{DDA}	V
t_{START}	Comparator startup time	Fast mode	-	15	20	µs
		Slow mode	-	20	25	
$t_{d\ slow}$	Propagation delay(2) in slow mode	1.65 V ≤ V_{DDA} ≤ 2.7 V	-	1.8	3.5	
		2.7 V ≤ V_{DDA} ≤ 3.6 V	-	2.5	6	
$t_{d\ fast}$	Propagation delay(2) in fast mode	1.65 V ≤ V_{DDA} ≤ 2.7 V	-	0.8	2	
		2.7 V ≤ V_{DDA} ≤ 3.6 V	-	1.2	4	
V_{offset}	Comparator offset error(3)		-	±4	±20	mV
dThreshold/dt	Threshold voltage temperature coefficient	V_{DDA} = 3.3V T_A = 0 to 50 °C V- = V_{REFINT}, 3/4 V_{REFINT}, 1/2 V_{REFINT}, 1/4 V_{REFINT}.	-	15	30	ppm /°C

6.3.19 Communications interfaces

I²C interface characteristics

The I²C interface meets the timings requirements of the I²C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm) : with a bit rate up to 100 kbit/s
- Fast-mode (Fm) : with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+) : with a bit rate up to 1 Mbit/s.

The I²C timing requirements are guaranteed by design when the I²C peripheral is properly configured (refer to the reference manual for details) and when the I2CCLK frequency is greater than the minimum given in *Table 63*. The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not "true" open-drain. When configured as open-drain, the PMOS connected between the I/O pin and VDDIOx is disabled, but is still present. Only FTf I/O pins support Fm+ low level output current maximum requirement (refer to *Section 6.3.13: I/O port characteristics* for the I2C I/Os characteristics).

All I²C SDA and SCL I/Os embed an analog filter (see *Table 62* for the analog filter characteristics).

Table 62. I2C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	50(2)	100(3)	ns

1. Guaranteed by design, not tested in production.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered

Table 63. I2C frequency in all I2C modes

Symbol	Parameter	Condition		Min	Unit
f_{I2CCLK}	I2C clock frequency	Standard-mode		2	MHz
		Fast-mode		8	
		Fast-mode Plus	Analog filter ON, DNF = 0	18	
			Analog filter OFF, DNF = 1	16	

SPI characteristics

Unless otherwise specified, the parameters given in the following tables are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 18*.

Refer to *Section 6.3.12: I/O current injection characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 65. SPI characteristics in voltage Range 1 (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	-	16	MHz
		Slave mode receiver			16	
		Slave mode Transmitter 1.71<V_{DD}<3.6V	-	-	12(2)	
		Slave mode Transmitter 2.7<V_{DD}<3.6V	-	-	16(2)	
$Duty_{(SCK)}$	Duty cycle of SPI clock frequency	Slave mode	30	50	70	%
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI presc = 2	4Tpclk	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI presc = 2	2Tpclk	-	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode	Tpclk-2	Tpclk	Tpclk+2	
$t_{su(MI)}$	Data input setup time	Master mode	3	-	-	
$t_{su(SI)}$		Slave mode	3	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	3.5	-	-	
$t_{h(SI)}$		Slave mode	0	-	-	
$t_{a(SO}$	Data output access time	Slave mode	15	-	36	
$t_{dis(SO)}$	Data output disable time	Slave mode	10	-	30	
$t_{v(SO)}$	Data output valid time	Slave mode 1.71<V_{DD}<3.6V	-	14	35	
		Slave mode 2.7<V_{DD}<3.6V	-	14	20	
$t_{v(MO)}$		Master mode	-	4	6	
$t_{h(SO)}$	Data output hold time	Slave mode	10	-	-	
$t_{h(MO)}$		Master mode	3	-	-	

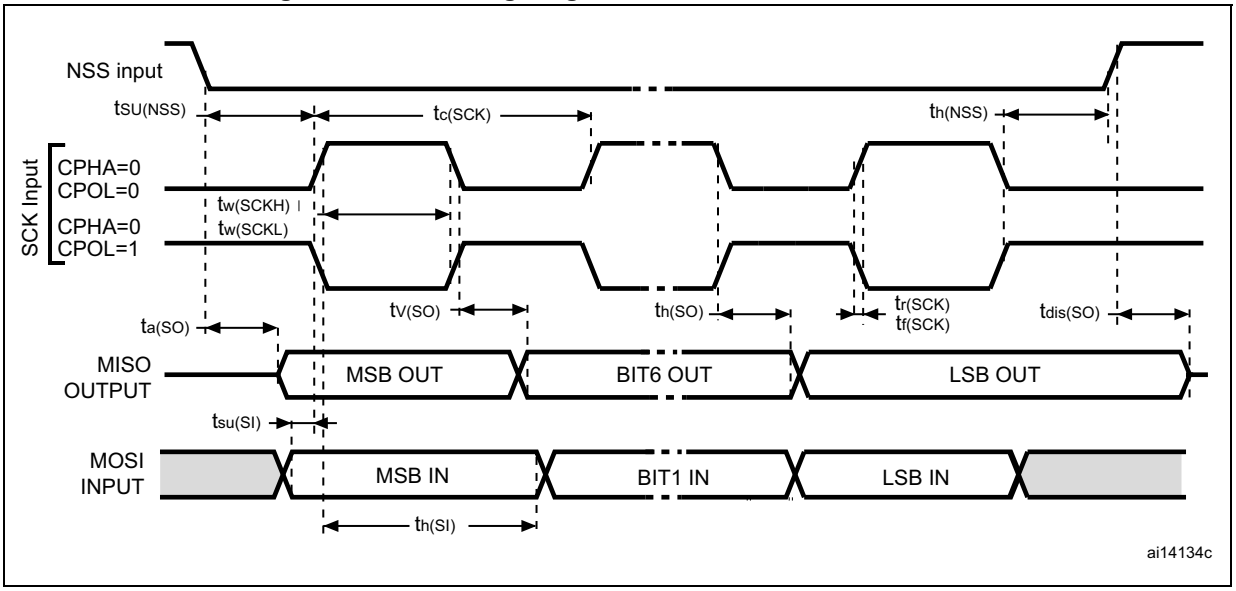
1. Guaranteed by characterization results, not tested in production.
2. The maximum SPI clock frequency in slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)}$ = 0 while $Duty_{(SCK)}$ = 50%.

Table 67. SPI characteristics in voltage Range 3 (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	-	2	MHz
		Slave mode			2(2)	
$Duty_{(SCK)}$	Duty cycle of SPI clock frequency	Slave mode	30	50	70	%
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI presc = 2	4Tpclk	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI presc = 2	2Tpclk	-	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode	Tpclk-2	Tpclk	Tpclk+2	
$t_{su(MI)}$	Data input setup time	Master mode	3	-	-	
$t_{su(SI)}$		Slave mode	3	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	16	-	-	
$t_{h(SI)}$		Slave mode	14	-	-	
$t_{a(SO}$	Data output access time	Slave mode	30	-	70	
$t_{dis(SO)}$	Data output disable time	Slave mode	40	-	80	
$t_{v(SO)}$	Data output valid time	Slave mode	-	26.5	47	
		Master mode	-	4	6	
$t_{v(MO)}$	Data output hold time	Slave mode	20	-	-	
$t_{h(SO)}$		Master mode	3	-	-	

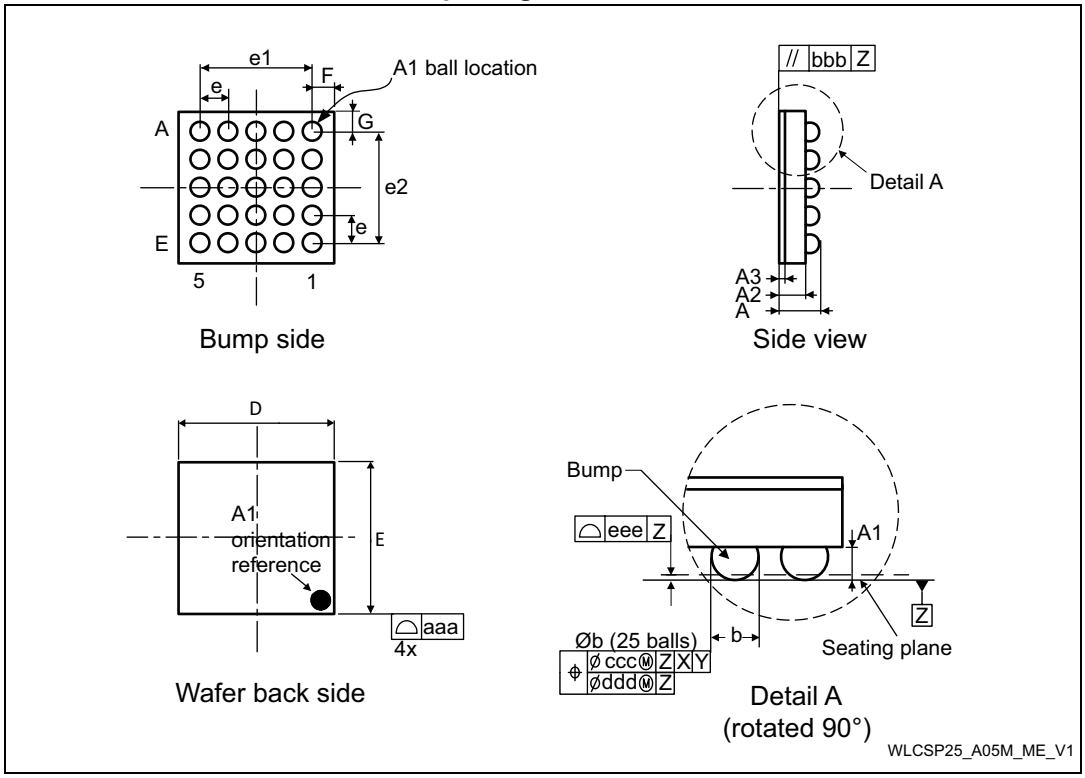
1. Guaranteed by characterization results, not tested in production.
2. The maximum SPI clock frequency in slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)}$ = 0 while $Duty_{(SCK)}$ = 50%.

Figure 30. SPI timing diagram - slave mode and CPHA = 0



7.3 WLCSP25 package information

Figure 39. WLCSP25 - 25-ball, 2.133 x 2.070 mm, 0.4 mm pitch wafer level chip scale package outline



1. Drawing is not to scale.

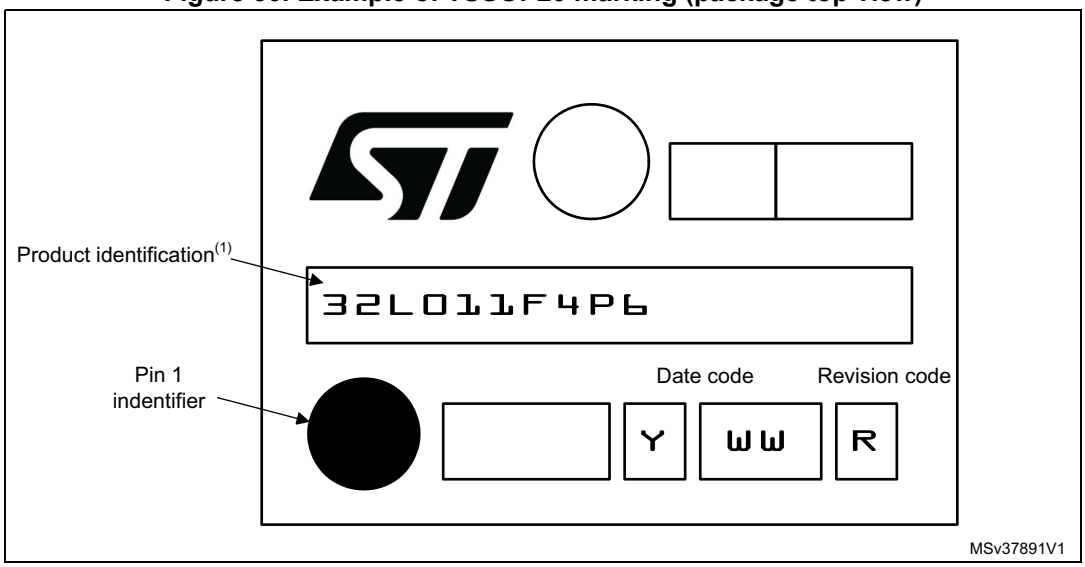
Table 70. WLCSP25 - 25-ball, 2.133 x 2.070 mm, 0.4 mm pitch wafer level chip scale package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.525	0.555	0.585	0.0207	0.0219	0.0230
A1	-	0.175	-	-	0.0069	-
A2	-	0.380	-	-	0.0150	-
A3[2]	-	0.025	-	-	0.0010	-
b[3]	0.220	0.250	0.280	0.0087	0.0098	0.0110
D	2.098	2.133	2.168	0.0826	0.0840	0.0854
E	2.035	2.070	2.105	0.0801	0.0815	0.0829
e	-	0.400	-	-	0.0157	-
e1	-	1.600	-	-	0.0630	-
e2	-	1.600	-	-	0.0630	-
F	-	0.2665	-	-	0.0105	-

Device marking

The following figure gives an example of topside marking versus pin 1 position identifier location.

Figure 50. Example of TSSOP20 marking (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.