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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0+ |
| Core Size | 32-Bit Single-Core |
| Speed | 32MHz |
| Connectivity | I²C, IrDA, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, POR, PWM, WDT |
| Number of I/O | 21 |
| Program Memory Size | 8KB (8K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 512 x 8 |
| RAM Size | 2K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.65V ~ 3.6V |
| Data Converters | A/D 10x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 25-UFBGA, WLCSP |
| Supplier Device Package | 25-WLCSP (2.13x2.07) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l011e3y6tr |

# 1 Introduction

The ultra-low-power STM32L011x3/4 family includes devices in 7 different package types from 14 to 32 pins. The description below gives an overview of the complete range of peripherals proposed in this family.

These features make the ultra-low-power STM32L011x3/4 microcontrollers suitable for a wide range of applications:

- Gas/water meters and industrial sensors
- Healthcare and fitness equipment
- Remote control and user interface
- PC peripherals, gaming, GPS equipment
- Alarm system, wired and wireless sensors, video intercom

This STM32L011x3/4 datasheet should be read in conjunction with the STM32L0x1 reference manual (RM0377).

For information on the ARM® Cortex®-M0+ core please refer to the Cortex®-M0+ Technical Reference Manual, available from the www.arm.com website.

*Figure 1* shows the general block diagram of the device family.

## 3.5 Clock management

The clock controller distributes the clocks coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness. It features:

- **Clock prescaler**

  To get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.

- **Safe clock switching**

  Clock sources can be changed safely on the fly in Run mode through a configuration register.

- **Clock management**

  To reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.

- **System clock source**

  Three different clock sources can be used to drive the master clock SYSCLK:

  – 0-32 MHz high-speed external (HSE bypass), that can supply a PLL
  – 16 MHz high-speed internal RC oscillator (HSI), trimmable by software, that can supply a PLL
  – Multispeed internal RC oscillator (MSI), trimmable by software, able to generate 7 frequencies (65 kHz, 131 kHz, 262 kHz, 524 kHz, 1.05 MHz, 2.1 MHz, 4.2 MHz). When a 32.768 kHz clock source is available in the system (LSE), the MSI frequency can be trimmed by software down to a ±0.5% accuracy.

- **Auxiliary clock source**

  Two ultra-low-power clock sources that can be used to drive the real-time clock:

  – 32.768 kHz low-speed external crystal (LSE)
  – 37 kHz low-speed internal RC (LSI), also used to drive the independent watchdog. The LSI clock can be measured using the high-speed internal RC oscillator for greater precision.

- **RTC clock sources**

  The LSI, LSE or HSE sources can be chosen to clock the RTC, whatever the system clock.

- **Startup clock**

  After reset, the microcontroller restarts by default with an internal 2 MHz clock (MSI). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.

- **Clock security system (CSS)**

  This feature can be enabled by software. If an LSE clock failure occurs, it provides an interrupt or wakeup event which is generated assuming it has been previously enabled. This feature is not available on the HSE clock.

- **Clock-out capability (MCO: microcontroller clock output)**

  It outputs one of the internal clocks for external use by the application.

Several prescalers allow the configuration of the AHB frequency, each APB (APB1 and APB2) domains. The maximum frequency of the AHB and the APB domains is 32 MHz. See *Figure 2* for details on the clock tree.

### 3.14.1 General-purpose timers (TIM2, TIM21)

There are three synchronizable general-purpose timers embedded in the STM32L011x3/4 devices (see *Table 7* for differences).

#### TIM2

TIM2 is based on 16-bit auto-reload up/down counter. It includes a 16-bit prescaler. It features four independent channels each for input capture/output compare, PWM or one-pulse mode output.

The TIM2 general-purpose timers can work together or with the TIM21 general-purpose timer via the Timer Link feature for synchronization or event chaining. Its counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs.

TIM2 has independent DMA request generation.

This timer is capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

#### TIM21

TIM21 is based on a 16-bit auto-reload up/down counter. It includes a 16-bit prescaler. It has two independent channels for input capture/output compare, PWM or one-pulse mode output. It can work together and be synchronized with TIM2 full-featured general-purpose timer.

It can also be used as simple timebase and be clocked by the LSE clock source (32.768 kHz) to provide independent timebase from the main CPU clock.

### 3.14.2 Low-power Timer (LPTIM)

The low-power timer has an independent clock and is running also in Stop mode if it is clocked by LSE, LSI or an external clock. It is able to wakeup the devices from Stop mode.

This low-power timer supports the following features:

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- Configurable output: pulse, PWM
- Continuous / one shot mode
- Selectable software / hardware input trigger
- Selectable clock source
  - Internal clock source: LSE, LSI, HSI or APB clock
  - External clock source over LPTIM1 input (working even with no internal clock source running, used by the Pulse Counter Application)
- Programmable digital glitch filter
- Encoder mode

### 3.14.3 SysTick timer

This timer is dedicated to the OS, but could also be used as a standard downcounter. It is based on a 24-bit downcounter with autoreload capability and a programmable clock source. It features a maskable system interrupt generation when the counter reaches ‘0’.

**Table 9. STM32L011x3/4 I²C implementation**

| I2C features[1] | I2C1 |
|---|---|
| 7-bit addressing mode | X |
| 10-bit addressing mode | X |
| Standard mode (up to 100 kbit/s) | X |
| Fast mode (up to 400 kbit/s) | X |
| Fast Mode Plus with 20 mA output drive I/Os (up to 1 Mbit/s) | X[2] |
| Independent clock | X |
| SMBus | X |
| Wakeup from STOP | X |

1. X = supported.
2. See *Table 13: Pin definitions on page 37* for the list of I/Os that feature Fast Mode Plus capability

### 3.15.2 Universal synchronous/asynchronous receiver transmitter (USART)

The USART interface (USART2) is able to communicate at speeds of up to 4 Mbit/s.

It provides hardware management of the CTS, RTS and RS485 driver enable (DE) signals, multiprocessor communication mode and single-wire half-duplex communication mode. USART2 also supports Smartcard communication (ISO 7816, T=0 protocol) and IrDA SIR ENDEC.

USART2 interface can be served by the DMA controller.

*Table 10* for the supported modes and features of USART interface.

**Table 10. USART implementation**

| USART modes/features[1] | USART2 |
|---|---|
| Hardware flow control for modem | X |
| Continuous communication using DMA | X |
| Multiprocessor communication | X |
| Synchronous mode | - |
| Smartcard mode | X |
| Single-wire half-duplex communication | X |
| IrDA SIR ENDEC block | X |
| LIN mode | - |
| Dual clock domain and wakeup from Stop mode | - |
| Receiver timeout interrupt | - |
| Modbus communication | - |
| Auto baud rate detection (4 modes) | - |
| Driver Enable | X |

1. X = supported.

## 3.17 Serial wire debug port (SW-DP)

An ARM SW-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.

Table 13. Pin definitions (continued)

| Pin number | | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Pin functions | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TSSOP14 | UFQFPN20 | TSSOP20 | UFQFPN28 | LQFP32 | UFQFPN32[1] | WLCSP25 | | | | | Alternate functions | Additional functions |
| 12 | 15 | 18 | 20 | 20 | 20 | C2 | PA10 | I/O | FTf | - | TIM21_CH1, I2C1_SDA, RTC_REFIN, USART2_RX, TIM2_CH3, COMP1_OUT | - |
| - | - | - | - | 21 | 21 | - | PA11 | I/O | FT | - | SPI1_MISO, LPTIM1_OUT, EVENTOUT, USART2_CTS, TIM21_CH2, COMP1_OUT | - |
| - | - | - | - | 22 | 22 | - | PA12 | I/O | FT | - | SPI1_MOSI, EVENTOUT, USART2_RTS, COMP2_OUT | - |
| 13 | 16 | 19 | 21 | 23 | 23 | A1 | PA13 | I/O | FTf | - | SWDIO, LPTIM1_ETR, I2C1_SDA, SPI1_SCK, LPUART1_RX, COMP1_OUT | - |
| 14 | 17 | 20 | 22 | 24 | 24 | A2 | PA14 | I/O | FT | - | SWCLK, LPTIM1_OUT, I2C1_SMBA, USART2_TX, SPI1_MISO, LPUART1_TX, COMP2_OUT | - |
| - | - | - | 23 | 25 | 25 | - | PA15 | I/O | FT | - | SPI1_NSS, TIM2_ETR, EVENTOUT, USART2_RX, TIM2_CH1 | - |
| - | - | - | 24 | 26 | 26 | B2 | PB3 | I/O | FT | - | SPI1_SCK, TIM2_CH2, EVENTOUT | COMP2_INM |
| - | - | - | 25 | 27 | 27 | - | PB4 | I/O | FT | - | SPI1_MISO, EVENTOUT | COMP2_INP |

# 6 Electrical characteristics

## 6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to $V_{SS}$.

### 6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A$ = 25 °C and $T_A$ = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

### 6.1.2 Typical values

Unless otherwise specified, typical data are based on $T_A$ = 25 °C, $V_{DD}$ = 3.6 V (for the 1.65 V ≤ $V_{DD}$ ≤ 3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

### 6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

### 6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 11*.

### 6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 12*.

**Figure 11. Pin loading conditions**

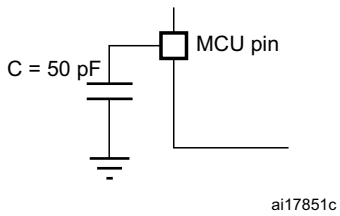
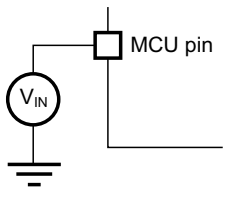
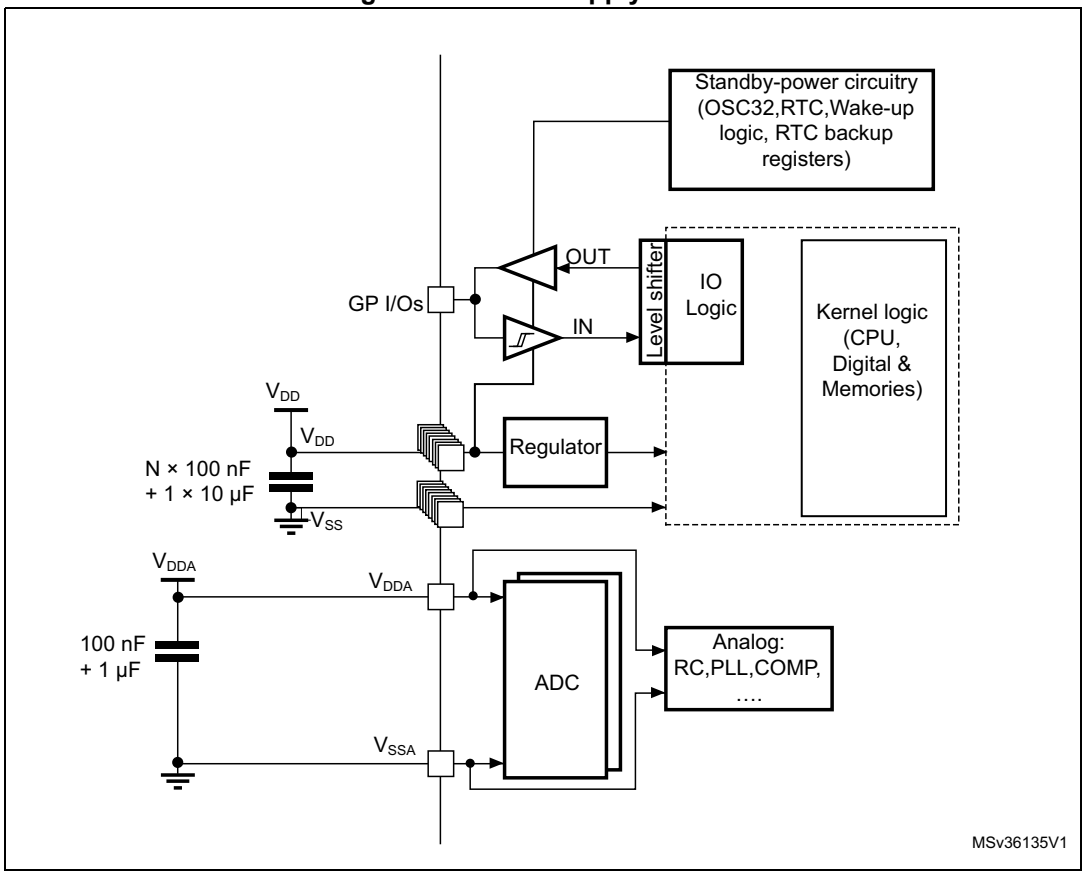



**Figure 12. Pin input voltage**



### 6.1.6 Power supply scheme

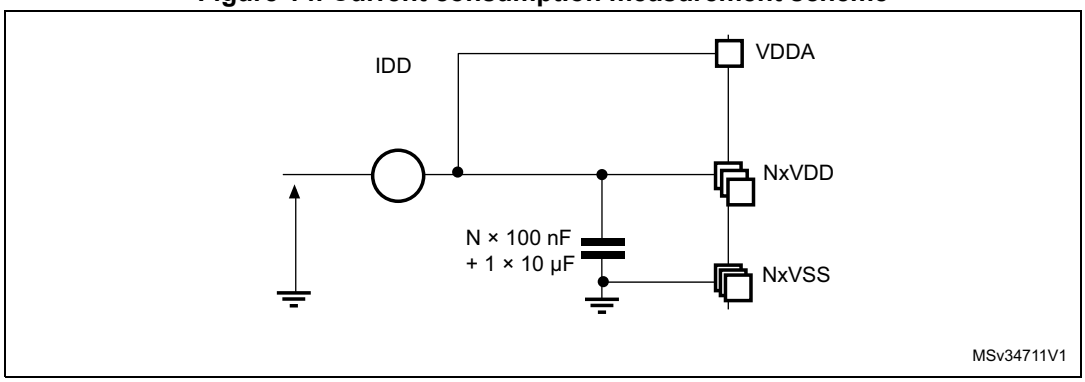
**Figure 13. Power supply scheme**




1. On TSSOP14 package, $V_{DDA}$ is internally connected to $V_{DD}$.
2. $V_{SSA}$ is internally connected to $V_{SS}$ on all packages.

### 6.1.7 Current consumption measurement

**Figure 14. Current consumption measurement scheme**



### 6.3.3 Embedded internal reference voltage

The parameters given in *Table 21* are based on characterization results, unless otherwise specified.

**Table 20. Embedded internal reference voltage calibration values**

| Calibration value name | Description | Memory address |
|---|---|---|
| VREFINT_CAL | Raw data acquired at temperature of 25°C $V_{DDA}$= 3 V | 0x1FF8 0078 - 0x1FF8 0079 |

**Table 21. Embedded internal reference voltage(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{REFINT\ out}$(2) | Internal reference voltage | – 40 °C < $T_J$ < +125 °C | 1.202 | 1.224 | 1.242 | V |
| $T_{VREFINT}$ | Internal reference startup time | - | - | 2 | 3 | ms |
| $V_{VREF\_MEAS}$ | $V_{DDA}$ voltage during $V_{REFINT}$ factory measure | - | 2.99 | 3 | 3.01 | V |
| $A_{VREF\_MEAS}$ | Accuracy of factory-measured $V_{REFINT}$ value(3) | Including uncertainties due to ADC and $V_{DDA}$ values | - | - | ±5 | mV |
| $T_{Coeff}$(4) | Temperature coefficient | –40 °C < $T_J$ < +125 °C | - | 25 | 100 | ppm/°C |
| | | 0 °C < $T_J$ < +50 °C | - | - | 20 | |
| $A_{Coeff}$(4) | Long-term stability | 1000 hours, T= 25 °C | - | - | 1000 | ppm |
| $V_{DDCoeff}$(4) | Voltage coefficient | 3.0 V < $V_{DDA}$ < 3.6 V | - | - | 2000 | ppm/V |
| $T_{S\_vrefint}$(4)(5) | ADC sampling time when reading the internal reference voltage | - | 5 | 10 | - | µs |
| $T_{ADC\_BUF}$(4) | Startup time of reference voltage buffer for ADC | - | - | - | 10 | µs |
| $I_{BUF\_ADC}$(4) | Consumption of reference voltage buffer for ADC | - | - | 13.5 | 25 | µA |
| $I_{VREF\_OUT}$(4) | VREF_OUT output current(6) | - | - | - | 1 | µA |
| $C_{VREF\_OUT}$(4) | VREF_OUT output load | - | - | - | 50 | pF |
| $I_{LPBUF}$(4) | Consumption of reference voltage buffer for VREF_OUT and COMP | - | - | 730 | 1200 | nA |
| $V_{REFINT\_DIV1}$(4) | 1/4 reference voltage | - | 24 | 25 | 26 | % $V_{REFINT}$ |
| $V_{REFINT\_DIV2}$(4) | 1/2 reference voltage | - | 49 | 50 | 51 | |
| $V_{REFINT\_DIV3}$(4) | 3/4 reference voltage | - | 74 | 75 | 76 | |

1. Refer to *Table 33: Peripheral current consumption in Stop and Standby mode* for the value of the internal reference current consumption ($I_{REFINT}$).
2. Guaranteed by test in production.
3. The internal $V_{REF}$ value is individually measured in production and stored in dedicated EEPROM bytes.

time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

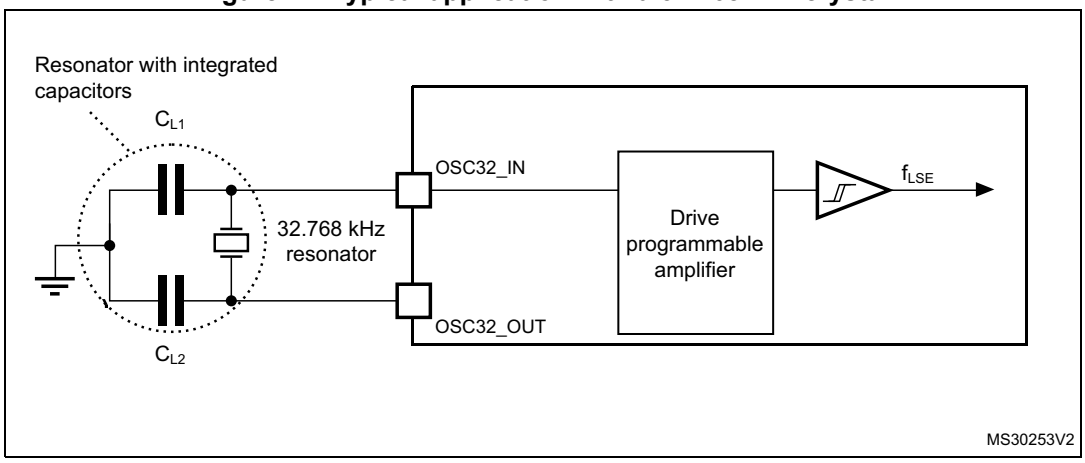
**Table 37. LSE oscillator characteristics(1)**

| Symbol | Parameter | Conditions(2) | Min(2) | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{LSE}$ | LSE oscillator frequency | | - | 32.768 | - | kHz |
| $G_m$ | Maximum critical crystal transconductance | LSEDRV[1:0]=00 lower driving capability | - | - | 0.5 | µA/V |
| | | LSEDRV[1:0]= 01 medium low driving capability | - | - | 0.75 | |
| | | LSEDRV[1:0] = 10 medium high driving capability | - | - | 1.7 | |
| | | LSEDRV[1:0]=11 higher driving capability | - | - | 2.7 | |
| $t_{SU(LSE)}$(3) | Startup time | $V_{DD}$ is stabilized | - | 2 | - | s |

1. Guaranteed by design, not tested in production.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
3. Guaranteed by characterization results, not tested in production. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer. To increase speed, address a lower-drive quartz with a high- driver mode.

*Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website http://www.st.com.*

**Figure 22. Typical application with a 32.768 kHz crystal**




*Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.*

## Flash memory and data EEPROM

**Table 43. Flash memory and data EEPROM characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Operating voltage Read / Write / Erase | - | 1.65 | - | 3.6 | V |
| $t_{prog}$ | Programming time for word or half-page | Erasing | - | 3.28 | 3.94 | ms |
| | | Programming | - | 3.28 | 3.94 | |
| $I_{DD}$ | Average current during the whole programming / erase operation | $T_A$ = 25 °C, $V_{DD}$ = 3.6 V | - | 500 | 700 | µA |
| | Maximum current (peak) during the whole programming / erase operation | | - | 1.5 | 2.5 | mA |

1. Guaranteed by design, not tested in production.

**Table 44. Flash memory and data EEPROM endurance and retention**

| Symbol | Parameter | Conditions | Value | Unit |
|---|---|---|---|---|
| | | | Min(1) | |
| $N_{CYC}$(2) | Cycling (erase / write) Program memory | $T_A$ = -40°C to 105 °C | 10 | kcycles |
| | Cycling (erase / write) EEPROM data memory | | 100 | |
| | Cycling (erase / write) Program memory | $T_A$ = -40°C to 125 °C | 0.2 | |
| | Cycling (erase / write) EEPROM data memory | | 2 | |
| $t_{RET}$(2) | Data retention (program memory) after 10 kcycles at $T_A$ = 85 °C | $T_{RET}$ = +85 °C | 30 | years |
| | Data retention (EEPROM data memory) after 100 kcycles at $T_A$ = 85 °C | | 30 | |
| | Data retention (program memory) after 10 kcycles at $T_A$ = 105 °C | $T_{RET}$ = +105 °C | 10 | |
| | Data retention (EEPROM data memory) after 100 kcycles at $T_A$ = 105 °C | | | |
| | Data retention (program memory) after 200 cycles at $T_A$ = 125 °C | $T_{RET}$ = +125 °C | | |
| | Data retention (EEPROM data memory) after 2 kcycles at $T_A$ = 125 °C | | | |

1. Guaranteed by characterization results, not tested in production.
2. Characterization is done according to JEDEC JESD22-A117.

**Figure 24. $V_{IH}/V_{IL}$ versus VDD (CMOS I/Os)**

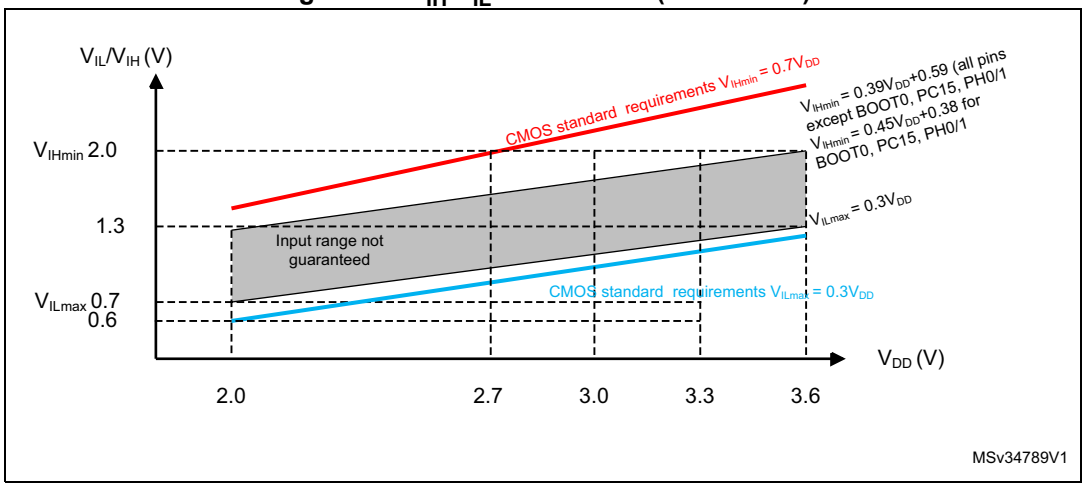
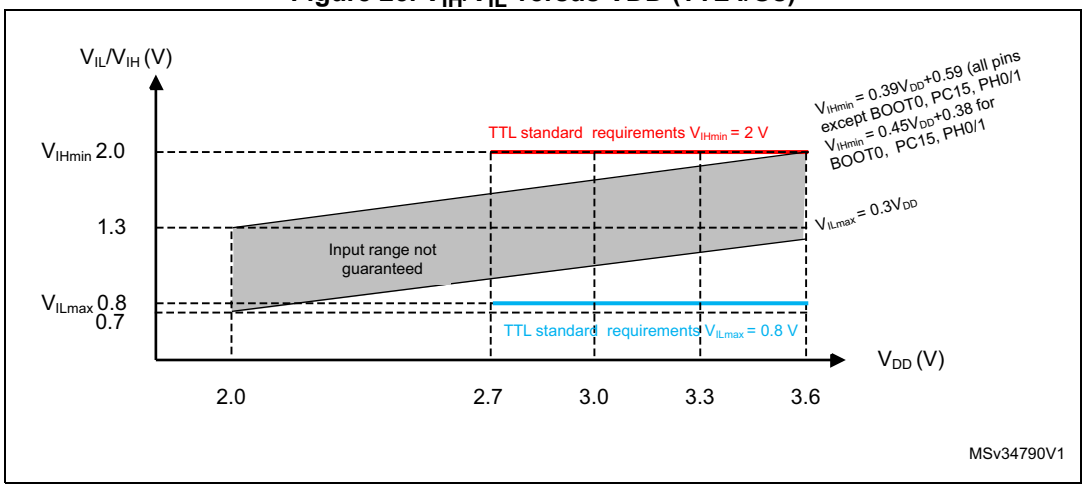



**Figure 25. $V_{IH}/V_{IL}$ versus VDD (TTL I/Os)**




## Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ±15 mA with the non-standard $V_{OL}/V_{OH}$ specifications given in *Table 51*.

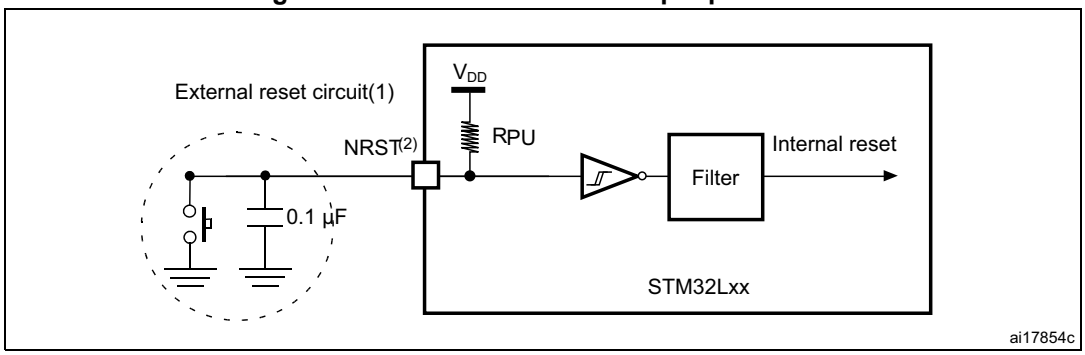
In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating $I_{VDD(\Sigma)}$ (see *Table 16*).
- The sum of the currents sunk by all the I/Os on $V_{SS}$ plus the maximum Run consumption of the MCU sunk on $V_{SS}$ cannot exceed the absolute maximum rating $I_{VSS(\Sigma)}$ (see *Table 16*).

## Output voltage levels

Unless otherwise specified, the parameters given in *Table 51* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in

**Figure 27. Recommended NRST pin protection**




1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 53*. Otherwise the reset will not be taken into account by the device.

## 6.3.15 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 54* are values derived from tests performed under ambient temperature, $f_{PCLK}$ frequency and $V_{DDA}$ supply voltage conditions summarized in *Table 18: General operating conditions*.

*Note: It is recommended to perform a calibration after each power-up.*

**Table 54. ADC characteristics**

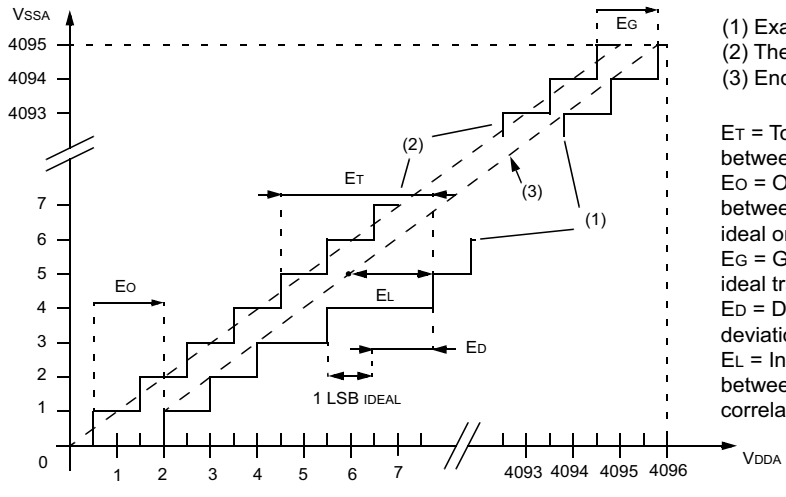
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DDA}$ | Analog supply voltage for ADC ON | Fast channel | 1.65 | - | 3.6 | V |
| | | Standard channels | 1.75(1) | - | 3.6 | |
| $I_{DDA\ (ADC)}$ | Current consumption of the ADC on $V_{DDA}$ | 1.14 Msps | - | 200 | - | µA |
| | | 10 ksps | - | 40 | - | |
| | Current consumption of the ADC on $V_{DD}$(2) | 1.14 Msps | - | 70 | - | |
| | | 10 ksps | - | 1 | - | |
| $f_{ADC}$ | ADC clock frequency | Voltage scaling Range 1 | 0.14 | - | 16 | MHz |
| | | Voltage scaling Range 2 | 0.14 | - | 8 | |
| | | Voltage scaling Range 3 | 0.14 | - | 4 | |
| $f_S$(3) | Sampling rate | - | 0.05 | - | 1.14 | MHz |
| $f_{TRIG}$(3) | External trigger frequency | $f_{ADC}$ = 16 MHz, 16-bit resolution | - | - | 941 | kHz |
| | | - | - | - | 17 | $1/f_{ADC}$ |
| $V_{AIN}$ | Conversion voltage range | - | 0 | - | $V_{DDA}$ | V |
| $R_{AIN}$(3) | External input impedance | See *Equation 1* and *Table 55* for details | - | - | 50 | kΩ |
| $R_{ADC}$(3)(4) | Sampling switch resistance | - | - | - | 1 | kΩ |
| $C_{ADC}$(3) | Internal sample and hold capacitor | - | - | - | 8 | pF |

**Table 56. ADC accuracy(1)(2)(3)(4)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| ET | Total unadjusted error | 1.65 V < $V_{DDA}$ < 3.6 V, range 1/2/3, TSSOP14 package | - | 3 | 5 | LSB |
| EO | Offset error | | - | 2 | 2.5 | |
| EG | Gain error | | - | 2 | 2.5 | |
| EL | Integral linearity error | | - | 1.5 | 2.5 | |
| ED | Differential linearity error | | - | 1 | 1.7 | |
| ENOB | Effective number of bits | | 9.5 | 10.5 | - | bits |
| | Effective number of bits (16-bit mode oversampling with ratio =256)(5) | | 10.7 | 11.6 | - | |
| SINAD | Signal-to-noise distortion | | 59 | 65 | - | dB |
| SNR | Signal-to-noise ratio | | 59 | 65 | - | |
| | Signal-to-noise ratio (16-bit mode oversampling with ratio =256)(5) | | 66 | 73 | - | |
| THD | Total harmonic distortion | | - | -75 | -63 | |

1. ADC DC accuracy values are measured after internal calibration.
2. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.
   Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.12* does not affect the ADC accuracy.
3. Better performance may be achieved in restricted $V_{DDA}$, frequency and temperature ranges.
4. In TSSOP14 package, where $V_{DDA}$ pin is shared with $V_{DD}$ pin, I/O toggling should be minimized to reach the values given in the above table. I/O toggling with loaded I/O pins can generate ripple on $V_{DD}/V_{DDA}$ and degrade the ADC accuracy.
5. This number is obtained by the test board without additional noise, resulting in non-optimized value for oversampling mode.

**Figure 28. ADC accuracy characteristics**




(1) Example of an actual transfer curve
(2) The ideal transfer curve
(3) End point correlation line

$E_T$ = Total Unajusted Error: maximum deviation between the actual and ideal transfer curves.
$E_O$ = Offset Error: maximum deviation between the first actual transition and the first ideal one.
$E_G$ = Gain Error: deviation between the last ideal transition and the last actual one.
$E_D$ = Differential Linearity Error: maximum deviation between actual steps and the ideal ones.
$E_L$ = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

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## 6.3.19 Communications interfaces

### I²C interface characteristics

The I²C interface meets the timings requirements of the I²C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm) : with a bit rate up to 100 kbit/s
- Fast-mode (Fm) : with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+) : with a bit rate up to 1 Mbit/s.

The I²C timing requirements are guaranteed by design when the I²C peripheral is properly configured (refer to the reference manual for details) and when the I2CCLK frequency is greater than the minimum given in *Table 63*. The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not "true" open-drain. When configured as open-drain, the PMOS connected between the I/O pin and VDDIOx is disabled, but is still present. Only FTf I/O pins support Fm+ low level output current maximum requirement (refer to *Section 6.3.13: I/O port characteristics* for the I2C I/Os characteristics).

All I²C SDA and SCL I/Os embed an analog filter (see *Table 62* for the analog filter characteristics).

**Table 62. I2C analog filter characteristics(1)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{AF}$ | Maximum pulse width of spikes that are suppressed by the analog filter | 50(2) | 100(3) | ns |

1. Guaranteed by design, not tested in production.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered

**Table 63. I2C frequency in all I2C modes**

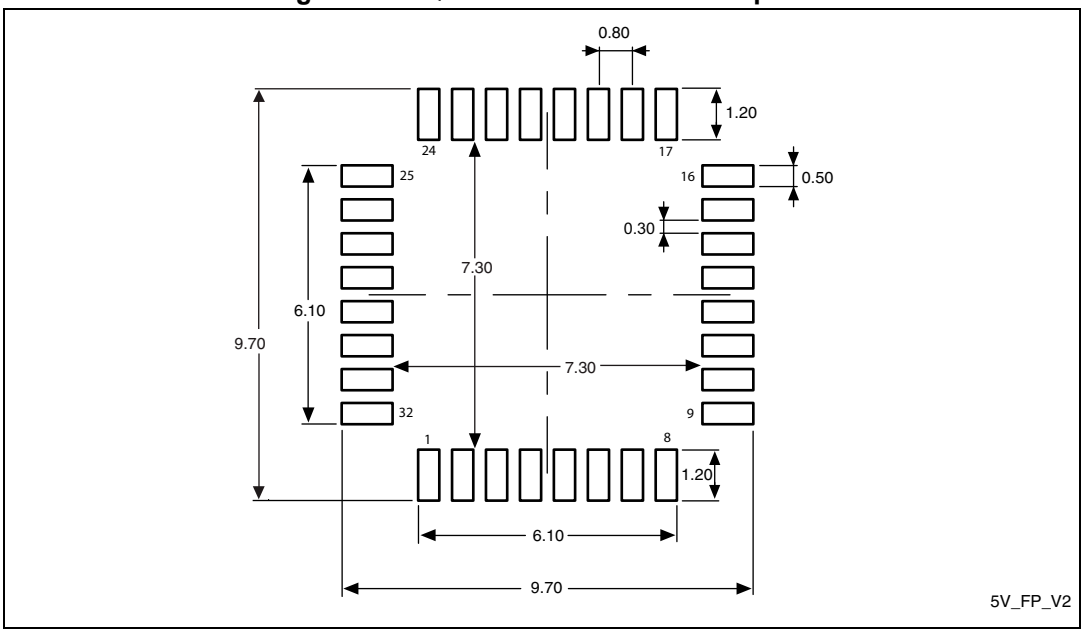
| Symbol | Parameter | Condition | | Min | Unit |
|---|---|---|---|---|---|
| $f_{I2CCLK}$ | I2C clock frequency | Standard-mode | | 2 | MHz |
| | | Fast-mode | | 8 | |
| | | Fast-mode Plus | Analog filter ON, DNF = 0 | 18 | |
| | | | Analog filter OFF, DNF = 1 | 16 | |

**Table 68. LQFP32, 7 x 7 mm, 32-pin low-profile quad flat package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.300 | 0.370 | 0.450 | 0.0118 | 0.0146 | 0.0177 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | 8.800 | 9.000 | 9.200 | 0.3465 | 0.3543 | 0.3622 |
| D1 | 6.800 | 7.000 | 7.200 | 0.2677 | 0.2756 | 0.2835 |
| D3 | - | 5.600 | - | - | 0.2205 | - |
| E | 8.800 | 9.000 | 9.200 | 0.3465 | 0.3543 | 0.3622 |
| E1 | 6.800 | 7.000 | 7.200 | 0.2677 | 0.2756 | 0.2835 |
| E3 | - | 5.600 | - | - | 0.2205 | - |
| e | - | 0.800 | - | - | 0.0315 | - |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| ccc | - | - | 0.100 | - | - | 0.0039 |
| A | - | - | 1.600 | - | - | 0.0630 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

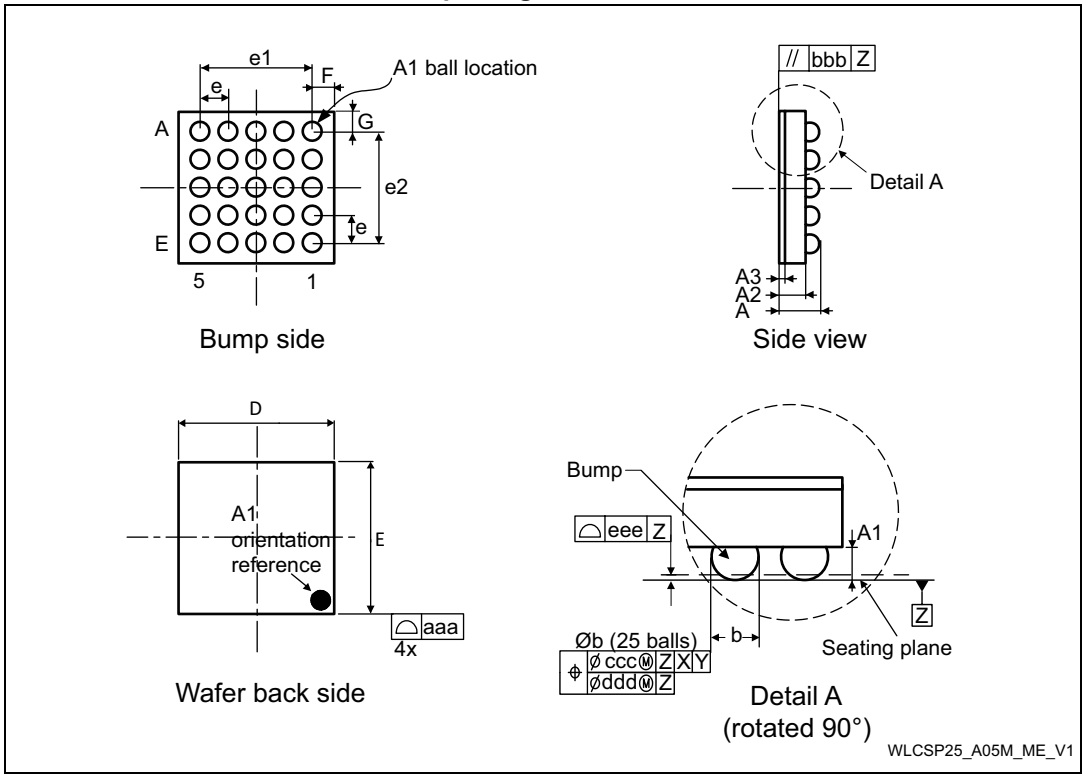
**Figure 34. LQFP32 recommended footprint**




1. Dimensions are expressed in millimeters.

## 7.3 WLCSP25 package information

**Figure 39. WLCSP25 - 25-ball, 2.133 x 2.070 mm, 0.4 mm pitch wafer level chip scale package outline**




1. Drawing is not to scale.

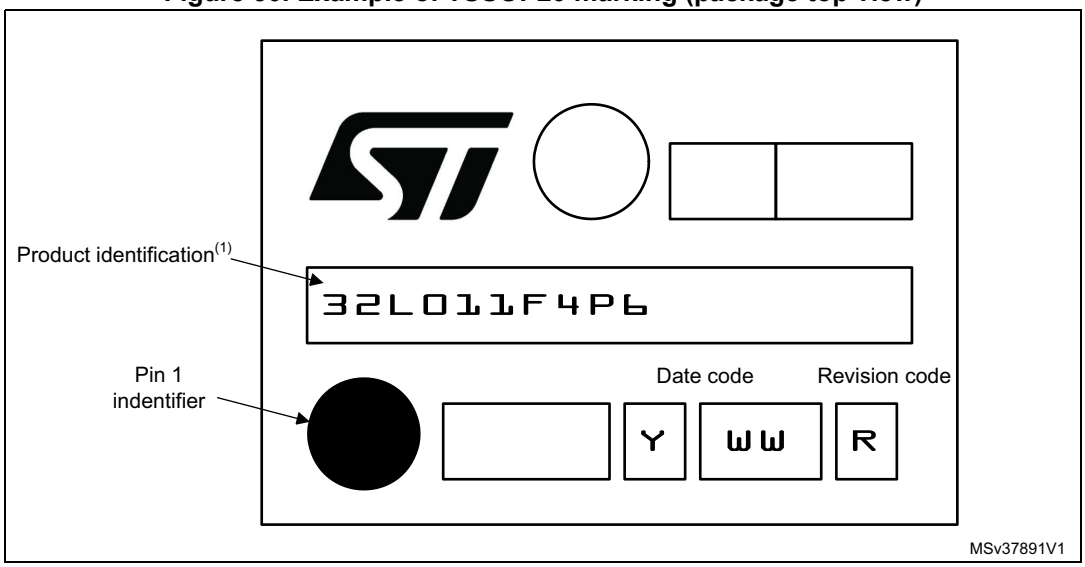
**Table 70. WLCSP25 - 25-ball, 2.133 x 2.070 mm, 0.4 mm pitch wafer level chip scale package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.525 | 0.555 | 0.585 | 0.0207 | 0.0219 | 0.0230 |
| A1 | - | 0.175 | - | - | 0.0069 | - |
| A2 | - | 0.380 | - | - | 0.0150 | - |
| A3[2] | - | 0.025 | - | - | 0.0010 | - |
| b[3] | 0.220 | 0.250 | 0.280 | 0.0087 | 0.0098 | 0.0110 |
| D | 2.098 | 2.133 | 2.168 | 0.0826 | 0.0840 | 0.0854 |
| E | 2.035 | 2.070 | 2.105 | 0.0801 | 0.0815 | 0.0829 |
| e | - | 0.400 | - | - | 0.0157 | - |
| e1 | - | 1.600 | - | - | 0.0630 | - |
| e2 | - | 1.600 | - | - | 0.0630 | - |
| F | - | 0.2665 | - | - | 0.0105 | - |

### Device marking

The following figure gives an example of topside marking versus pin 1 position identifier location.

**Figure 50. Example of TSSOP20 marking (package top view)**

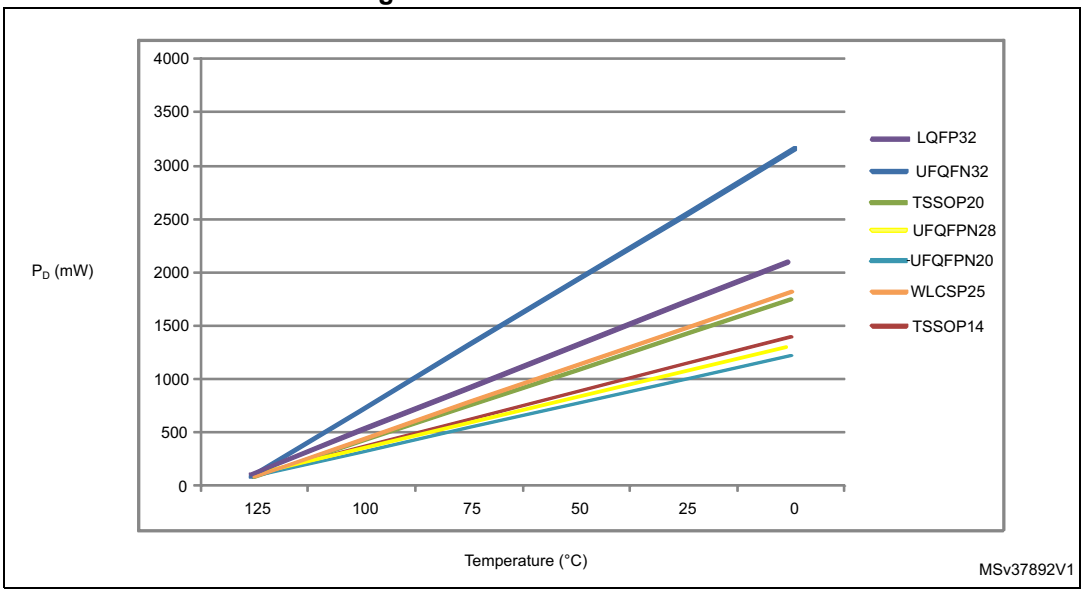



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

**Table 76. Thermal characteristics**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $\Theta_{JA}$ | **Thermal resistance junction-ambient** LQFP32 - 7 x 7 mm / 0.8 mm pitch | 60 | °C/W |
| | **Thermal resistance junction-ambient** UFQFPN32 - 5 x 5 mm / 0.5 mm pitch | 39 | |
| | **Thermal resistance junction-ambient** WLCSP25 - 2.133 x 2.070 mm, 0.4 mm pitch | 70 | |
| | **Thermal resistance junction-ambient** UFQFPN28 - 4 x 4 mm, 0.5 mm pitch | 97 | |
| | **Thermal resistance junction-ambient** UFQFPN20 - 3 x 3 mm, 0.5 mm pitch | 102 | |
| | **Thermal resistance junction-ambient** TSSOP20 - 169 mils | 74 | |
| | **Thermal resistance junction-ambient** TSSOP14 - 169 mils | 95 | |

**Figure 53. Thermal resistance**




1. The above curves are valid for range 3.

### 7.8.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.