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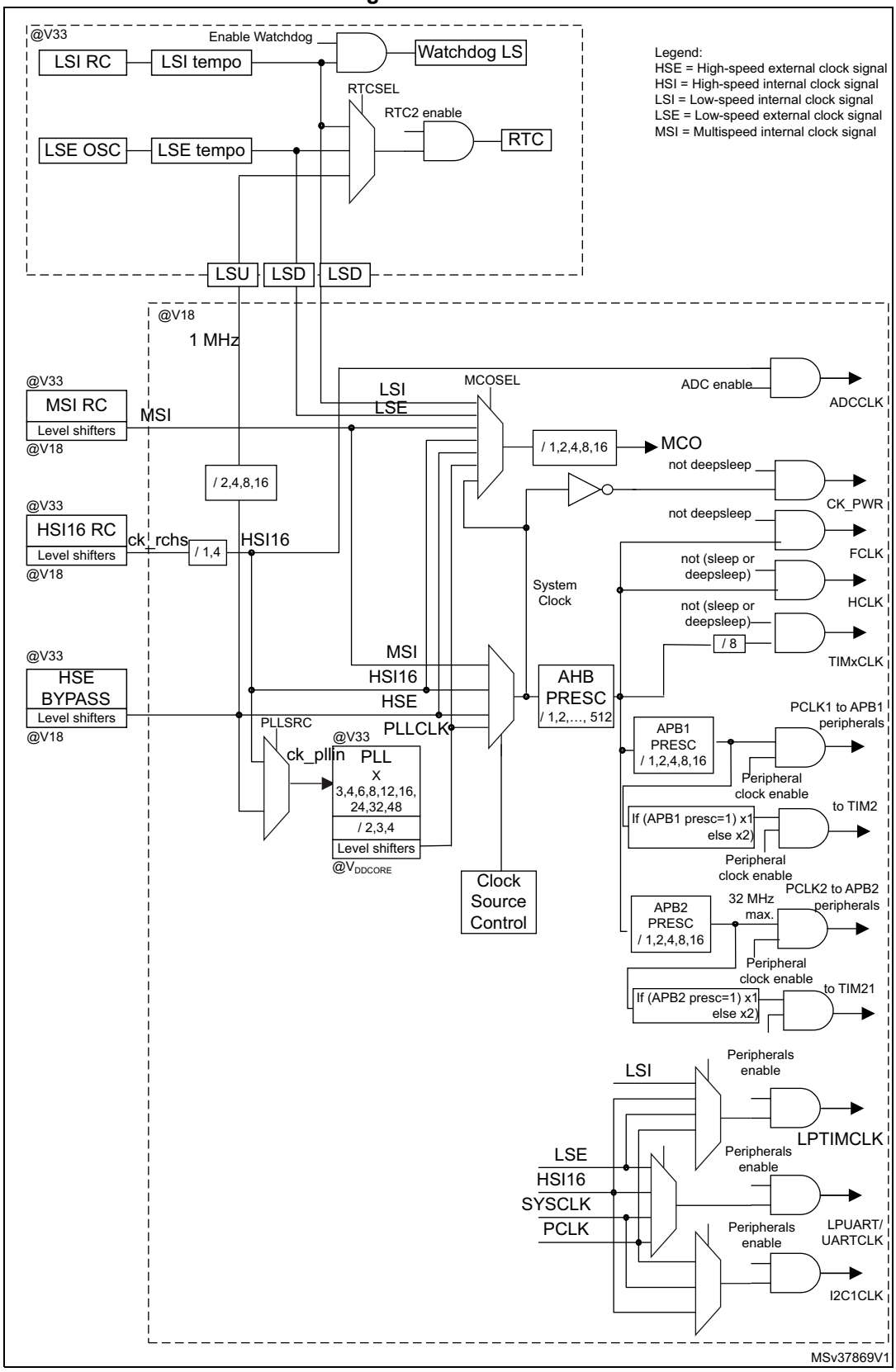
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	21
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	25-UFBGA, WLCSP
Supplier Device Package	25-WLCSP
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l011e4y6tr

Figure 2. Clock tree



3.6 Low-power real-time clock and backup registers

The real time clock (RTC) and the 5 backup registers are supplied in all modes including standby mode. The backup registers are five 32-bit registers used to store 20 bytes of user application data. They are not reset by a system reset, or when the device wakes up from Standby mode.

The RTC is an independent BCD timer/counter. Its main features are the following:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format
- Automatically correction for 28, 29 (leap year), 30, and 31 day of the month
- Two programmable alarms with wake up from Stop and Standby mode capability
- Periodic wakeup from Stop and Standby with programmable resolution and period
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy
- 2 anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection.

The RTC clock sources can be:

- A 32.768 kHz external crystal
- A resonator or oscillator
- The internal low-power RC oscillator (typical frequency of 37 kHz)
- The high-speed external clock

3.7 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions, and can be individually remapped using dedicated alternate function registers. All GPIOs are high current capable. Each GPIO output, speed can be slowed (40 MHz, 10 MHz, 2 MHz, 400 kHz). The alternate function configuration of I/Os can be locked if needed following a specific sequence in order to avoid spurious writing to the I/O registers. The I/O controller is connected to a dedicated IO bus with a toggling speed of up to 32 MHz.

The BOOT0 pin is shared with PB9 GPIO pin. This pin is an input-only pin. If nBOOT_SEL option bit is reset, sampling this pin on NRST rising edge gives the internal BOOT0 state. This pin then works as PB9 pin. The input voltage characteristics of this pin are specific for BOOT0 pin type (see *Table 50: I/O static characteristics*).

Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of 26 edge detector lines used to generate interrupt/event requests. Each line can be individually configured to select the trigger event

(rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 38 GPIOs can be connected to the 16 configurable interrupt/event lines. The 10 other lines are connected to PVD, RTC, USART, I2C, LPUART, LPTIM or comparator events.

3.8 Memories

The STM32L011x3/4 devices have the following features:

- 2 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states. With the enhanced bus matrix, operating the RAM does not lead to any performance penalty during accesses to the system bus (AHB and APB buses).
- The non-volatile memory is divided into three arrays:
  - 8 or 16 Kbytes of embedded Flash program memory
  - 512 bytes of data EEPROM
  - Information block containing 32 user and factory options bytes plus 4 Kbytes of system memory

The user options bytes are used to write-protect or read-out protect the memory (with 4 Kbyte granularity) and/or readout-protect the whole memory with the following options:

- **Level 0**: no protection
- **Level 1**: memory readout protected.

  The Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
- **Level 2**: chip readout protected, debug features (Cortex-M0+ serial wire) and boot in RAM selection disabled (debugline fuse)

The whole non-volatile memory embeds the error correction code (ECC) feature.

3.9 Direct memory access (DMA)

The flexible 5-channel, general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^2C, USART, LPUART, general-purpose timers, and ADC.

3.12 Ultra-low-power comparators and reference voltage

The STM32L011x3/4 embed two comparators sharing the same current bias and reference voltage. The reference voltage can be internal or external (coming from an I/O).

- One comparator with ultra low consumption
- One comparator with rail-to-rail inputs, fast or slow mode.
- The threshold can be one of the following:
  - External I/O pins
  - Internal reference voltage (V_{REFINT})
  - submultiple of Internal reference voltage(1/4, 1/2, 3/4) for the rail to rail comparator.

Both comparators can wake up the devices from Stop mode, and be combined into a window comparator.

The internal reference voltage is available externally via a low-power / low-current output buffer (driving current capability of 1 µA typical).

3.13 System configuration controller

The system configuration controller provides the capability to remap some alternate functions on different I/O ports.

The highly flexible routing interface allows the application firmware to control the routing of different I/Os to the TIM2, TIM21 and LPTIM1 timer input captures. It also controls the routing of internal analog signals to the ADC, COMP1 and COMP2 and the internal reference voltage V_{REFINT}.

3.14 Timers and watchdogs

The ultra-low-power STM32L011x3/4 devices include two general-purpose timers, one low-power timer (LPTIM1), two watchdog timers and the SysTick timer.

Table 7 compares the features of the general-purpose and basic timers.

Table 7. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
TIM2	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TIM21	16-bit	Up, down, up/down	Any integer between 1 and 65536	No	2	No

3.14.1 General-purpose timers (TIM2, TIM21)

There are three synchronizable general-purpose timers embedded in the STM32L011x3/4 devices (see *Table 7* for differences).

TIM2

TIM2 is based on 16-bit auto-reload up/down counter. It includes a 16-bit prescaler. It features four independent channels each for input capture/output compare, PWM or one-pulse mode output.

The TIM2 general-purpose timers can work together or with the TIM21 general-purpose timer via the Timer Link feature for synchronization or event chaining. Its counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs.

TIM2 has independent DMA request generation.

This timer is capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

TIM21

TIM21 is based on a 16-bit auto-reload up/down counter. It includes a 16-bit prescaler. It has two independent channels for input capture/output compare, PWM or one-pulse mode output. It can work together and be synchronized with TIM2 full-featured general-purpose timer.

It can also be used as simple timebase and be clocked by the LSE clock source (32.768 kHz) to provide independent timebase from the main CPU clock.

3.14.2 Low-power Timer (LPTIM)

The low-power timer has an independent clock and is running also in Stop mode if it is clocked by LSE, LSI or an external clock. It is able to wakeup the devices from Stop mode.

This low-power timer supports the following features:

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- Configurable output: pulse, PWM
- Continuous / one shot mode
- Selectable software / hardware input trigger
- Selectable clock source
  - Internal clock source: LSE, LSI, HSI or APB clock
  - External clock source over LPTIM1 input (working even with no internal clock source running, used by the Pulse Counter Application)
- Programmable digital glitch filter
- Encoder mode

3.14.3 SysTick timer

This timer is dedicated to the OS, but could also be used as a standard downcounter. It is based on a 24-bit downcounter with autoreload capability and a programmable clock source. It features a maskable system interrupt generation when the counter reaches ‘0’.

3.15.3 Low-power universal asynchronous receiver transmitter (LPUART)

The devices embed one Low-power UART. The LPUART supports asynchronous serial communication with minimum power consumption. It supports half duplex single wire communication and modem operations (CTS/RTS). It allows multiprocessor communication.

The LPUART has a clock domain independent from the CPU clock, and can wake up the system from Stop mode, using baudrates up to 46 Kbaud. The Wakeup events from Stop mode are programmable and can be:

- Start bit detection
- Or any received data frame
- Or a specific programmed data frame

Only a 32.768 kHz clock (LSE) is needed to allow LPUART communication up to 9600 baud. Therefore, even in Stop mode, the LPUART can wait for an incoming frame while having an extremely low energy consumption. Higher speed clock can be used to reach higher baudrates.

LPUART interface can be served by the DMA controller.

3.15.4 Serial peripheral interface (SPI)

The SPI is able to communicate at up to 16 Mbits/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

The SPI can be served by the DMA controller.

Refer to *Table 11* for the supported modes and features of SPI interface.

Table 11. SPI implementation

SPI features(1)	SPI1
Hardware CRC calculation	X
I2S mode	-
TI mode	X

1. X = supported.

3.16 Cyclic redundancy check (CRC) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

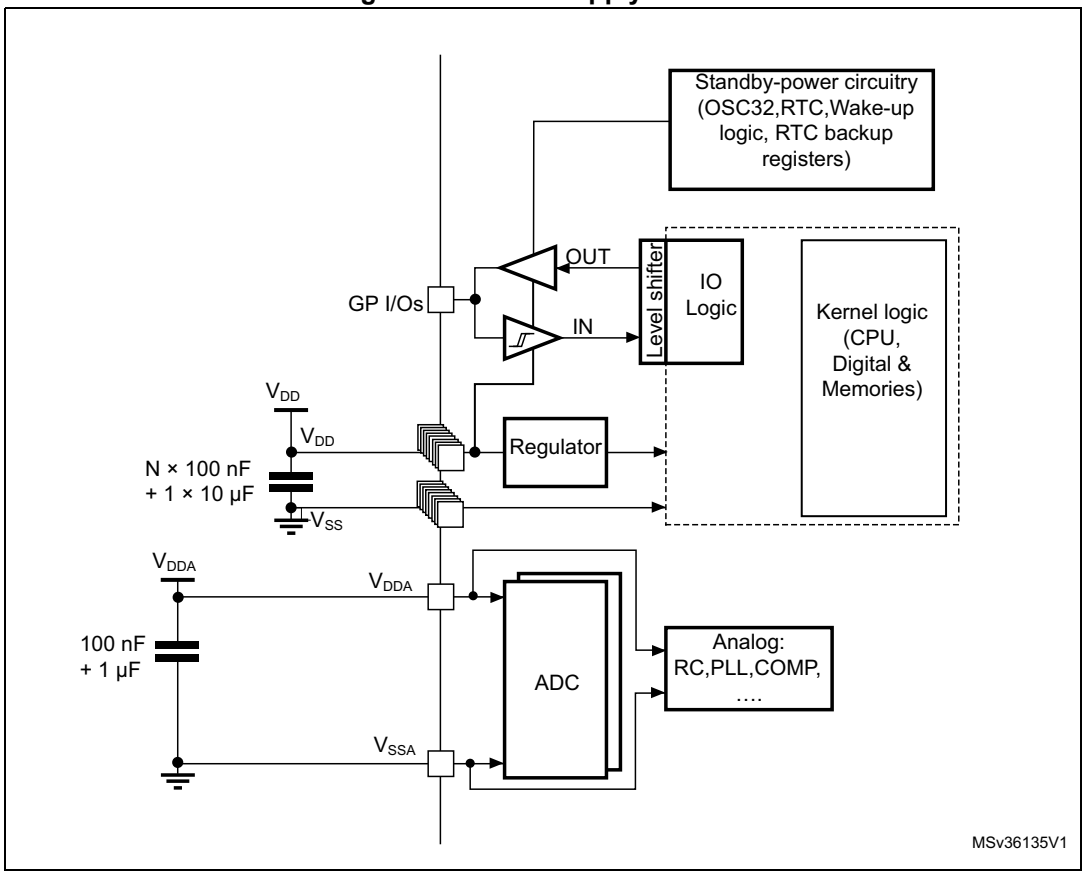
Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at linktime and stored at a given memory location.

Table 13. Pin definitions

Pin number							Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
TSSOP14	UFQFPN20	TSSOP20	UFQFPN28	LQFP32	UFQFPN32[1]	WLCSP25					Alternate functions	Additional functions
2	1	2	2	2	2	B5	PC14-OSC32_IN	I/O	FT	-	-	OSC32_IN
3	2	3	3	3	3	C5	PC15-OSC32_OUT	I/O	TC	-	-	OSC32_OUT
4	3	4	4	4	4	D5	NRST	I/O	RST	(2)	-	-
10	4	5	5	5	5	C4	VDDA	S	-	(3)(4)	-	-
5	5	6	6	6	6	E5	PA0-CK_IN	I/O	TTa	-	USART2_RX, LPTIM1_IN1, TIM2_CH1, USART2_CTS, TIM2_ETR, LPUART1_RX, COMP1_OUT	COMP1_INM, ADC_IN0, RTC_TAMP2/WKUP1/CK_IN
6	6	7	7	7	7	B4	PA1	I/O	FT	-	EVENTOUT, LPTIM1_IN2, TIM2_CH2, I2C1_SMBA, USART2_RTS, TIM21_ETR, LPUART1_TX	COMP1_INP, ADC_IN1
-	-	8	8	8	8	D4	PA2	I/O	TTa	-	TIM21_CH1, TIM2_CH3, USART2_TX, LPUART1_TX, COMP2_OUT	COMP2_INM, ADC_IN2, RTC_TAMP3/RTC_TS/RTC_OUT/WKUP3
-	-	9	9	9	9	E4	PA3	I/O	FT	-	TIM21_CH2, TIM2_CH4, USART2_RX, LPUART1_RX	COMP2_INP, ADC_IN3
7	7	10	10	10	10	B3	PA4	I/O	TTa	-	SPI1_NSS, LPTIM1_IN1, LPTIM1_ETR, I2C1_SCL, USART2_CK, TIM2_ETR, LPUART1_TX, COMP2_OUT	COMP1_INM, COMP2_INM, ADC_IN4

6.1.6 Power supply scheme

Figure 13. Power supply scheme



1. On TSSOP14 package, V_{DDA} is internally connected to V_{DD}.
2. V_{SSA} is internally connected to V_{SS} on all packages.

6.1.7 Current consumption measurement

Figure 14. Current consumption measurement scheme

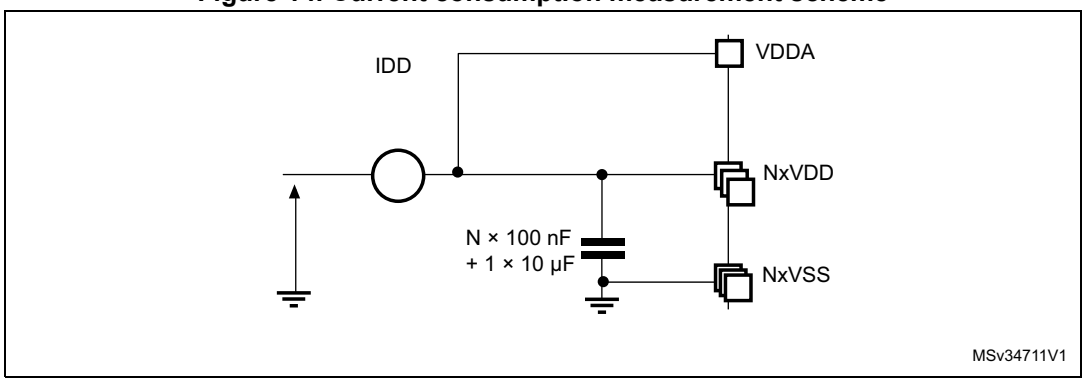


Table 16. Current characteristics

Symbol	Ratings	Max.	Unit
ΣI_{VDD} (2)	Total current into sum of all V_{DD} power lines (source)(1)	105	mA
ΣI_{VSS} (2)	Total current out of sum of all V_{SS} ground lines (sink)(1)	105	
$I_{VDD(PIN)}$	Maximum current into each V_{DD} power pin (source)(1)	100	
$I_{VSS(PIN)}$	Maximum current out of each V_{SS} ground pin (sink)(1)	100	
I_{IO}	Output current sunk by any I/O and control pin except FTf pins	16	
	Output current sunk by FTf pins	22	
	Output current sourced by any I/O and control pin	-16	
$\Sigma I_{IO(PIN)}$ (3)	Total output current sunk by sum of all IOs and control pins(4)	45	
	Total output current sourced by sum of all IOs and control pins	-45	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all IOs and control pins(2)	90	
	Total output current sourced by sum of all IOs and control pins(2)	-90	
$I_{INJ(PIN)}$	Injected current on FT, FFf, RST and B pins	-5/+0(5)	
	Injected current on TC pin	± 5(6)	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(7)	± 25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
3. These values apply only to STM32L011GxUx part number (UFQFPN28 package).
4. This current consumption must be correctly distributed over all I/Os and control pins. In particular, it must be located the closest possible to the couple of supply and ground, and distributed on both sides.
5. Positive current injection is not possible on these I/Os. A negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 15* for maximum allowed input voltage values.
6. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 15: Voltage characteristics* for the maximum allowed input voltage values.
7. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 17. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

Table 18. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
T_A	Temperature range	Maximum power dissipation (range 6)	–40	85	°C
		Maximum power dissipation (range 7)	–40	105	
		Maximum power dissipation (range 3)	–40	125	
T_J	Junction temperature range (range 6)	-40 °C ≤ T_A ≤ 85 °	–40	105	
	Junction temperature range (range 7)	-40 °C ≤ T_A ≤ 105 °C	–40	125	
	Junction temperature range (range 3)	-40 °C ≤ T_A ≤ 125 °C	–40	130	

1. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and normal operation.
2. To sustain a voltage higher than V_{DD}+0.3V, the internal pull-up/pull-down resistors must be disabled.
3. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_J max (see *Table 17: Thermal characteristics on page 47*).

6.3.2 Embedded reset and power control block characteristics

The parameters given in the following table are derived from the tests performed under the ambient temperature condition summarized in *Table 18*.

Table 19. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VDD}(1)	V_{DD} rise time rate	BOR detector enabled	0	-	∞	µs/V
		BOR detector disabled	0	-	1000	
	V_{DD} fall time rate	BOR detector enabled	20	-	∞	
		BOR detector disabled	0	-	1000	
$T_{RSTTEMPO}$(1)	Reset temporization	V_{DD} rising, BOR enabled	-	2	3.3	ms
		V_{DD} rising, BOR disabled(2)	0.4	0.7	1.6	
$V_{POR/PDR}$	Power on/power down reset threshold	Falling edge	1	1.5	1.65	V
		Rising edge	1.3	1.5	1.65	
V_{BOR0}	Brown-out reset threshold 0	Falling edge	1.67	1.7	1.74	
		Rising edge	1.69	1.76	1.8	
V_{BOR1}	Brown-out reset threshold 1	Falling edge	1.87	1.93	1.97	
		Rising edge	1.96	2.03	2.07	
V_{BOR2}	Brown-out reset threshold 2	Falling edge	2.22	2.30	2.35	
		Rising edge	2.31	2.41	2.44	

6.3.3 Embedded internal reference voltage

The parameters given in *Table 21* are based on characterization results, unless otherwise specified.

Table 20. Embedded internal reference voltage calibration values

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at temperature of 25°C V_{DDA}= 3 V	0x1FF8 0078 - 0x1FF8 0079

Table 21. Embedded internal reference voltage(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{REFINT\ out}$(2)	Internal reference voltage	– 40 °C < T_J < +125 °C	1.202	1.224	1.242	V
$T_{VREFINT}$	Internal reference startup time	-	-	2	3	ms
V_{VREF_MEAS}	V_{DDA} voltage during V_{REFINT} factory measure	-	2.99	3	3.01	V
A_{VREF_MEAS}	Accuracy of factory-measured V_{REFINT} value(3)	Including uncertainties due to ADC and V_{DDA} values	-	-	±5	mV
T_{Coeff}(4)	Temperature coefficient	–40 °C < T_J < +125 °C	-	25	100	ppm/°C
		0 °C < T_J < +50 °C	-	-	20	
A_{Coeff}(4)	Long-term stability	1000 hours, T= 25 °C	-	-	1000	ppm
$V_{DDCoeff}$(4)	Voltage coefficient	3.0 V < V_{DDA} < 3.6 V	-	-	2000	ppm/V
$T_{S\_vrefint}$(4)(5)	ADC sampling time when reading the internal reference voltage	-	5	10	-	µs
T_{ADC_BUF}(4)	Startup time of reference voltage buffer for ADC	-	-	-	10	µs
I_{BUF_ADC}(4)	Consumption of reference voltage buffer for ADC	-	-	13.5	25	µA
I_{VREF_OUT}(4)	VREF_OUT output current(6)	-	-	-	1	µA
C_{VREF_OUT}(4)	VREF_OUT output load	-	-	-	50	pF
I_{LPBUF}(4)	Consumption of reference voltage buffer for VREF_OUT and COMP	-	-	730	1200	nA
V_{REFINT_DIV1}(4)	1/4 reference voltage	-	24	25	26	% V_{REFINT}
V_{REFINT_DIV2}(4)	1/2 reference voltage	-	49	50	51	
V_{REFINT_DIV3}(4)	3/4 reference voltage	-	74	75	76	

1. Refer to *Table 33: Peripheral current consumption in Stop and Standby mode* for the value of the internal reference current consumption (I_{REFINT}).
2. Guaranteed by test in production.
3. The internal V_{REF} value is individually measured in production and stored in dedicated EEPROM bytes.

Table 27. Current consumption in Low-power Run mode

Symbol	Parameter	Conditions			Typ	Max(1)	Unit
I_{DD} (LP Run)	Supply current in Low-power run mode	All peripherals OFF, code executed from RAM, Flash switched OFF, V_{DD} from 1.65 V to 3.6 V	MSI clock, 65 kHz f_{HCLK} = 32 kHz	T_A = -40 °C to 25 °C	5.7	8.1	µA
				T_A = 85 °C	6.5	9	
				T_A = 105 °C	8	13	
				T_A = 125 °C	11.5	22	
			MSI clock, 65 kHz f_{HCLK} = 65 kHz	T_A =-40 °C to 25 °C	8.7	11	
				T_A = 85 °C	9.5	12	
				T_A = 105 °C	11	15	
				T_A = 125 °C	15	24	
			MSI clock, 131 kHz f_{HCLK} = 131 kHz	T_A = -40 °C to 25 °C	17	19	
				T_A = 55 °C	17	19.5	
				T_A = 85 °C	17.5	20	
				T_A = 105 °C	19	22	
				T_A = 125 °C	22.5	31	
		All peripherals OFF, code executed from Flash, V_{DD} from 1.65 V to 3.6 V	MSI clock, 65 kHz f_{HCLK} = 32 kHz	T_A = -40 °C to 25 °C	18	22	
				T_A = 85 °C	20	24	
				T_A = 105 °C	22	27	
				T_A = 125 °C	26.5	37	
			MSI clock, 65 kHz f_{HCLK} = 65 kHz	T_A = -40 °C to 25 °C	22	25	
				T_A = 85 °C	24	27	
				T_A = 105 °C	26	30	
				T_A = 125 °C	30.5	39	
			MSI clock, 131 kHz f_{HCLK} = 131 kHz	T_A = -40 °C to 25 °C	32	34	
				T_A = 55 °C	32.5	35	
				T_A = 85 °C	34	37	
				T_A = 105 °C	36	39	
				T_A = 125 °C	40	47	

1. Guaranteed by characterization results at 125 °C, not tested in production, unless otherwise specified.

Figure 17. I_{DD} vs V_{DD}, at T_A= -40/25/55/ 85/105/125 °C, Low-power run mode, code running from RAM, Range 3, MSI (Range 0) at 64 KHz, 0 WS

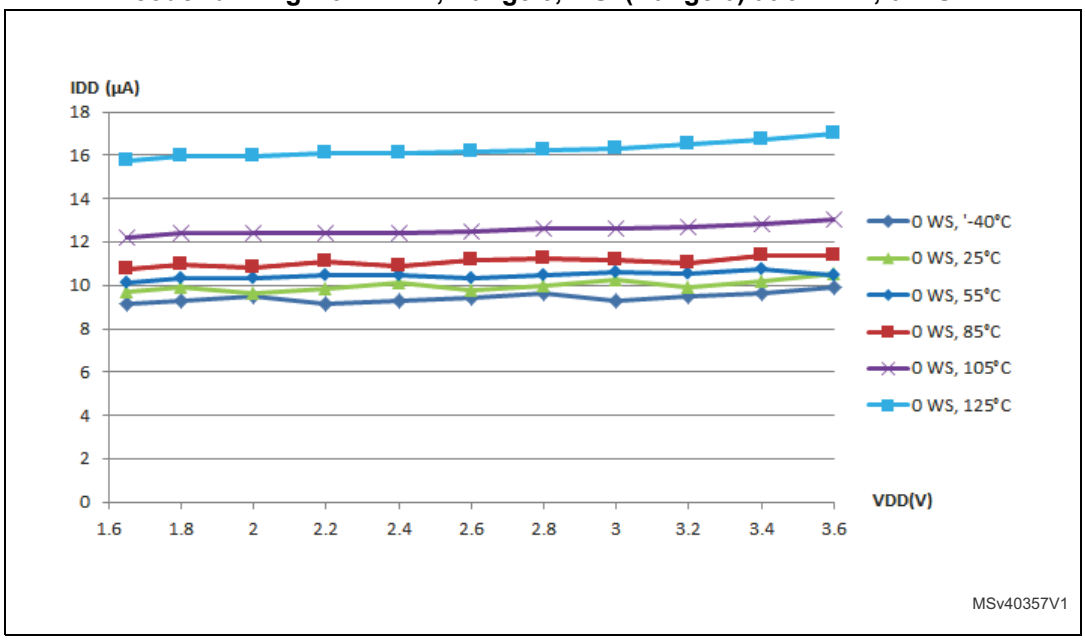


Table 28. Current consumption in Low-power Sleep mode

Symbol	Parameter	Conditions			Typ	Max(1)	Unit
I_{DD} (LP Sleep)	Supply current in Low-power sleep mode	All peripherals OFF, V_{DD} from 1.65 V to 3.6 V	MSI clock, 65 kHz f_{HCLK} = 32 kHz Flash OFF	T_A = -40 °C to 25 °C	2.5(2)	-	µA
			MSI clock, 65 kHz f_{HCLK} = 32 kHz Flash ON	T_A = -40 °C to 25 °C	13	19	
				T_A = 85 °C	15.5	20	
				T_A = 105 °C	17.5	22	
				T_A = 125 °C	21	29	
			MSI clock, 65 kHz f_{HCLK} = 65 kHz, Flash ON	T_A = -40 °C to 25 °C	13.5	19	
				T_A = 85 °C	16	20	
				T_A = 105 °C	18	22	
				T_A = 125 °C	21.5	29	
			MSI clock, 131 kHz f_{HCLK} = 131 kHz, Flash ON	T_A = -40 °C to 25 °C	15.5	21	
				T_A = 55 °C	17	22	
				T_A = 85 °C	18	23	
				T_A = 105 °C	19.5	24	
				T_A = 125 °C	23.5	31	

1. Guaranteed by characterization results at 125 °C, not tested in production, unless otherwise specified.
2. As the CPU is in Sleep mode, the difference between the current consumption with Flash memory ON and OFF (nearly 12 µA) is the same whatever the clock frequency.

Table 54. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{CAL}(3)	Calibration time	f_{ADC} = 16 MHz	5.2			µs
		-	83			$1/f_{ADC}$
$W_{LATENCY}$	ADC_DR register write latency	ADC clock = HSI16	1.5 ADC cycles + 2 f_{PCLK} cycles	-	1.5 ADC cycles + 3 f_{PCLK} cycles	-
		ADC clock = PCLK/2	-	4.5	-	f_{PCLK} cycle
		ADC clock = PCLK/4	-	8.5	-	f_{PCLK} cycle
t_{latr}(3)	Trigger conversion latency	f_{ADC} = f_{PCLK}/2 = 16 MHz	0.266			µs
		f_{ADC} = f_{PCLK}/2	8.5			$1/f_{PCLK}$
		f_{ADC} = f_{PCLK}/4 = 8 MHz	0.516			µs
		f_{ADC} = f_{PCLK}/4	16.5			$1/f_{PCLK}$
		f_{ADC} = f_{HSI16} = 16 MHz	0.252	-	0.260	µs
$Jitter_{ADC}$	ADC jitter on trigger conversion	f_{ADC} = f_{HSI16}	-	1	-	$1/f_{HSI16}$
t_S(3)	Sampling time	f_{ADC} = 16 MHz	0.093	-	10.03	µs
		-	1.5	-	239.5	$1/f_{ADC}$
t_{STAB}(3)	Power-up time	-	0	0	1	µs
t_{ConV}(3)	Total conversion time (including sampling time)	f_{ADC} = 16 MHz	0.875		10.81	µs
		-	14 to 173 (t_S for sampling +12.5 for successive approximation)			$1/f_{ADC}$

1. V_{DDA} minimum value can be decreased in specific temperature conditions. Refer to *Table 55: RAIN max for fADC = 16 MHz*.
2. A current consumption proportional to the APB clock frequency has to be added (see *Table 32: Peripheral current consumption in run or Sleep mode*).
3. Guaranteed by design, not tested in production.
4. Standard channels have an extra protection resistance which depends on supply voltage. Refer to *Table 55: RAIN max for fADC = 16 MHz*.

Equation 1: R_{AIN} max formula

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The simplified formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 55. R_{AIN} max for f_{ADC} = 16 MHz(1)

T_s (cycles)	t_S (µs)	R_{AIN} max for fast channels (kΩ)	R_{AIN} max for standard channels (kΩ)						
			V_{DD} > 2.7 V	V_{DD} > 2.4 V	V_{DD} > 2.0 V	V_{DD} > 1.8 V	V_{DD} > 1.75 V	V_{DD} > 1.65 V and T_A > -10 °C	V_{DD} > 1.65 V and T_A > 25 °C
1.5	0.09	0.5	< 0.1	NA	NA	NA	NA	NA	NA
3.5	0.22	1	0.2	< 0.1	NA	NA	NA	NA	NA
7.5	0.47	2.5	1.7	1.5	< 0.1	NA	NA	NA	NA
12.5	0.78	4	3.2	3	1	NA	NA	NA	NA
19.5	1.22	6.5	5.7	5.5	3.5	NA	NA	NA	< 0.1
39.5	2.47	13	12.2	12	10	NA	NA	NA	5
79.5	4.97	27	26.2	26	24	< 0.1	NA	NA	19
160.5	10.03	50	49.2	49	47	32	< 0.1	< 0.1	42

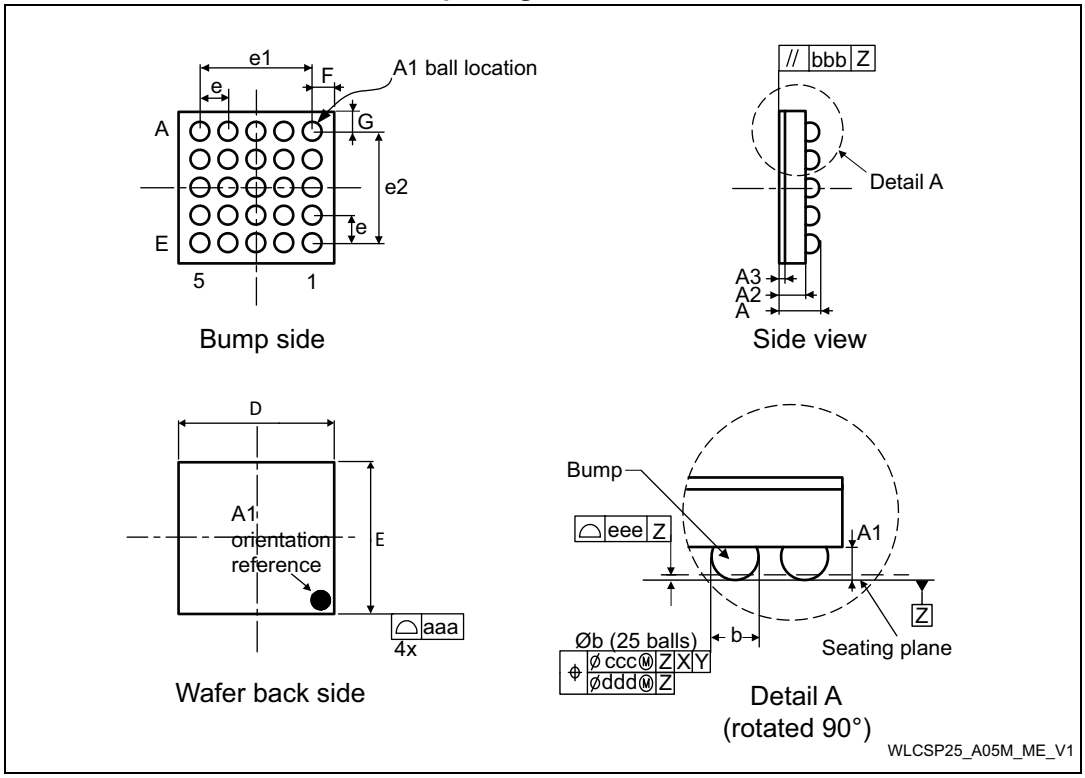
1. Guaranteed by design.

Table 56. ADC accuracy(1)(2)(3)(4)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ET	Total unadjusted error	1.65 V < V_{DDA} < 3.6 V, range 1/2/3, except for TSSOP14 package	-	2	4	LSB
EO	Offset error		-	1	2.5	
EG	Gain error		-	1	2	
EL	Integral linearity error		-	1.5	2.5	
ED	Differential linearity error		-	1	1.5	
ENOB	Effective number of bits		10.2	11		bits
	Effective number of bits (16-bit mode oversampling with ratio =256)(5)		11.3	12.1	-	
SINAD	Signal-to-noise distortion		62	67.8	-	dB
SNR	Signal-to-noise ratio		63	68	-	
	Signal-to-noise ratio (16-bit mode oversampling with ratio =256)(5)		70	76	-	
THD	Total harmonic distortion		-	-81	-68.5	

7.3 WLCSP25 package information

Figure 39. WLCSP25 - 25-ball, 2.133 x 2.070 mm, 0.4 mm pitch wafer level chip scale package outline



1. Drawing is not to scale.

Table 70. WLCSP25 - 25-ball, 2.133 x 2.070 mm, 0.4 mm pitch wafer level chip scale package mechanical data

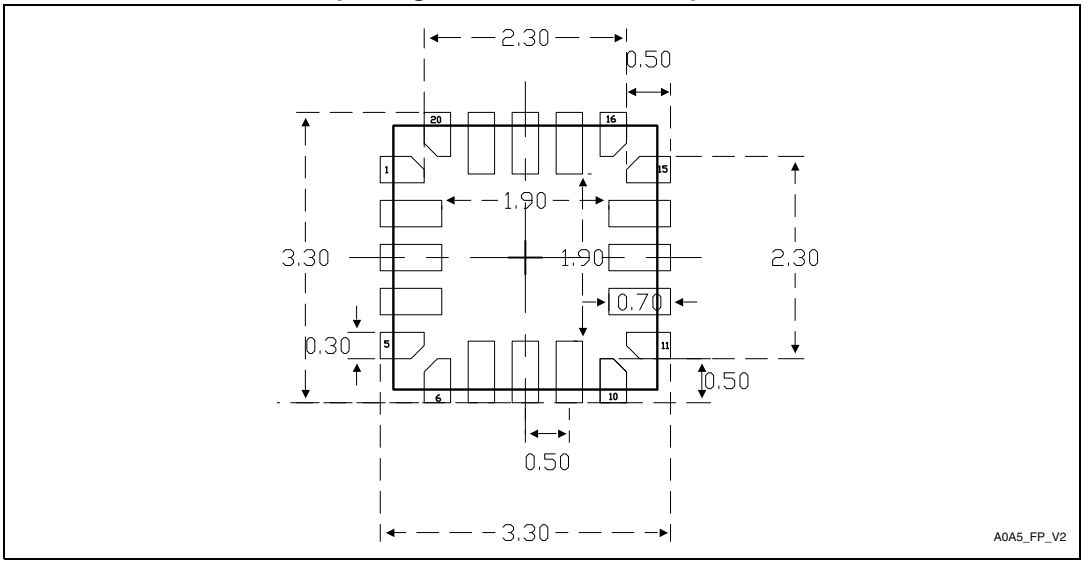
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.525	0.555	0.585	0.0207	0.0219	0.0230
A1	-	0.175	-	-	0.0069	-
A2	-	0.380	-	-	0.0150	-
A3[2]	-	0.025	-	-	0.0010	-
b[3]	0.220	0.250	0.280	0.0087	0.0098	0.0110
D	2.098	2.133	2.168	0.0826	0.0840	0.0854
E	2.035	2.070	2.105	0.0801	0.0815	0.0829
e	-	0.400	-	-	0.0157	-
e1	-	1.600	-	-	0.0630	-
e2	-	1.600	-	-	0.0630	-
F	-	0.2665	-	-	0.0105	-

Table 73. UFQFPN20 - 20-lead, 3x3 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
A3	-	0.152	-	-	0.060	-
D	-	3.000	-	-	0.1181	-
E	-	3.000	-	-	0.1181	-
L1	0.500	0.550	0.600	0.0197	0.0217	0.0236
L2	0.300	0.350	0.400	0.0118	0.0138	0.0157
L3	-	0.375	-	-	0.0148	-
L4	-	0.200	-	-	0.0079	-
L5	-	0.150	-	-	0.0059	-
b	0.180	0.250	0.300	0.0071	0.0098	0.0118
e	-	0.500	-	-	0.0197	-
ddd	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 46. UFQFPN20 - 20-lead, 3x3 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package recommended footprint

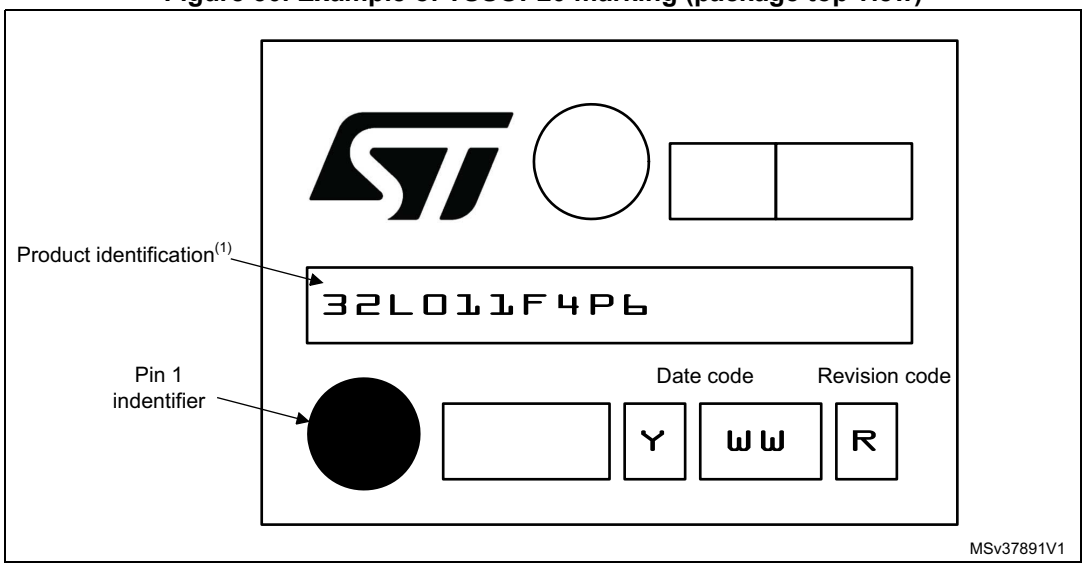


1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking versus pin 1 position identifier location.

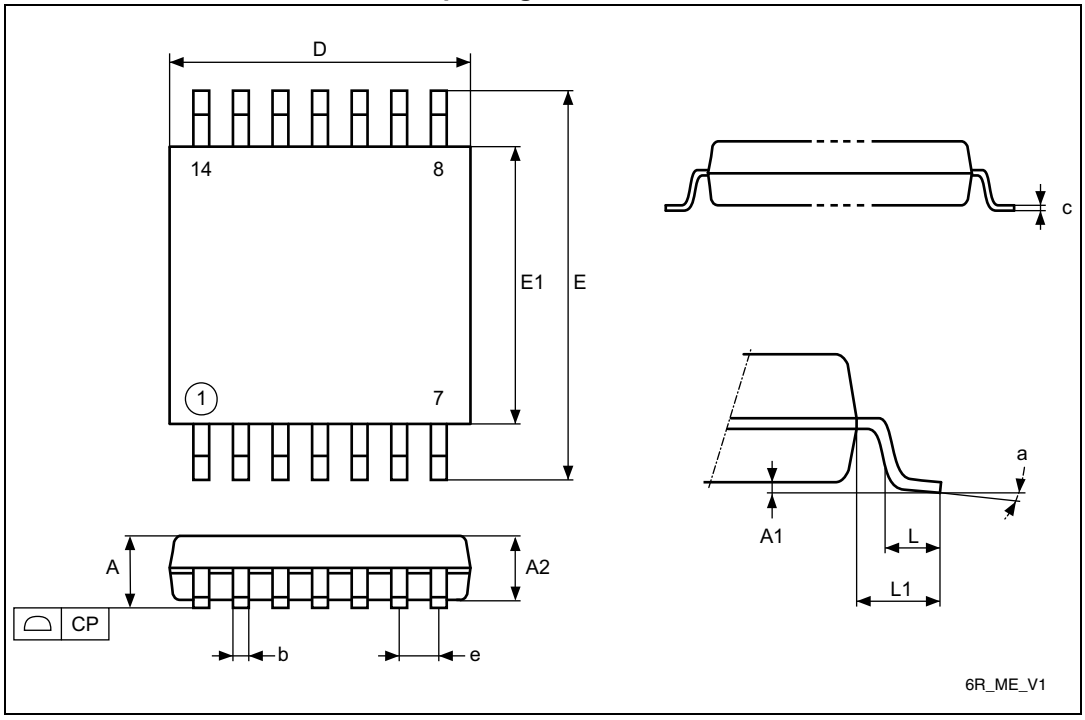
Figure 50. Example of TSSOP20 marking (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

7.7 TSSOP14 package information

Figure 51.TSSOP14 – 14-lead thin shrink small outline, 5.0 x 4.4 mm, 0.65 mm pitch, package outline



1. Drawing is not to scale.

Table 75. TSSOP14 – 14-lead thin shrink small outline, 5.0 x 4.4 mm, 0.65 mm pitch, package mechanical data

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.200	-	-	0.0472
A1	0.050	-	0.150	0.0020	-	0.0059
A2	0.800	1.000	1.050	0.0315	0.0394	0.0413
b	0.190	-	0.300	0.0075	-	0.0118
c	0.090	-	0.200	0.0035	-	0.0079
CP	-	-	0.100	-	-	0.0039
D	4.900	5.000	5.100	0.1929	0.1969	0.2008
e	-	0.650	-	-	0.0256	-
E	6.200	6.400	6.600	0.2441	0.2520	0.2598
E1	4.300	4.400	4.500	0.1693	0.1732	0.1772
L	0.500	0.600	0.750	0.0197	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
a	0°	-	8°	0°	-	8°

8 Part numbering

Table 77. STM32L011x3/4 ordering information scheme

Example: STM32 L 011 K 4 T 6 D xxx

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

L = Low power

Device subfamily

011 = Access line

Pin count

K = 32 pins

G = 28 pins

E = 25 pins

F = 20 pins

D = 14 pins

Flash memory size

3 = 8 Kbytes

4 = 16 Kbytes

Package

T = LQFP

U = UFQFPN

Y = WLCSP

P = TSSOP

Temperature range

6 = Industrial temperature range, –40 to 85 °C

7 = Industrial temperature range, –40 to 105 °C

3 = Industrial temperature range, –40 to 125 °C

Options

No character = V_{DD} range: 1.8 to 3.6 V and BOR enabled

D = V_{DD} range: 1.65 to 3.6 V and BOR disabled

Packing

TR = tape and reel

No character = tray or tube

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.