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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I <sup>2</sup> C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	16
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 9x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l011f3p6">https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l011f3p6</a>

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## 2 Description

The access line ultra-low-power STM32L011x3/4 family incorporates the high-performance ARM® Cortex®-M0+ 32-bit RISC core operating at a 32 MHz frequency, high-speed embedded memories (up to 16 Kbytes of Flash program memory, 512 bytes of data EEPROM and 2 Kbytes of RAM) plus an extensive range of enhanced I/Os and peripherals.

The STM32L011x3/4 devices provide high power efficiency for a wide range of performance. It is achieved with a large choice of internal and external clock sources, an internal voltage adaptation and several low-power modes.

The STM32L011x3/4 devices offer several analog features, one 12-bit ADC with hardware oversampling, two ultra-low-power comparators, several timers, one low-power timer (LPTIM), three general-purpose 16-bit timers, one RTC and one SysTick which can be used as timebases. They also feature two watchdogs, one watchdog with independent clock and window capability and one window watchdog based on bus clock.

Moreover, the STM32L011x3/4 devices embed standard and advanced communication interfaces: one I2C, one SPI, one USART, and a low-power UART (LPUART).

The STM32L011x3/4 also include a real-time clock and a set of backup registers that remain powered in Standby mode.

The ultra-low-power STM32L011x3/4 devices operate from a 1.8 to 3.6 V power supply (down to 1.65 V at power down) with BOR and from a 1.65 to 3.6 V power supply without BOR option. They are available in the -40 to +125 °C temperature range. A comprehensive set of power-saving modes allows the design of low-power applications.



## 2.2 Ultra-low-power device continuum

The ultra-low-power family offers a large choice of core and features, from 8-bit proprietary core up to ARM® Cortex®-M4, including ARM® Cortex®-M3 and ARM® Cortex®-M0+. The STM32Lx series are the best choice to answer your needs in terms of ultra-low-power features. The STM32 Ultra-low-power series are the best solution for applications such as gas/water meter, keyboard/mouse or fitness and healthcare application. Several built-in features like LCD drivers, dual-bank memory, low-power Run mode, operational amplifiers, 128-bit AES, DAC, crystal-less USB and many other definitely help you building a highly cost optimized application by reducing BOM cost. STMicroelectronics, as a reliable and long-term manufacturer, ensures as much as possible pin-to-pin compatibility between all STM8Lx and STM32Lx on one hand, and between all STM32Lx and STM32Fx on the other hand. Thanks to this unprecedented scalability, your legacy application can be upgraded to respond to the latest market feature and efficiency requirements.

## 3 Functional overview

### 3.1 Low-power modes

The ultra-low-power STM32L011x3/4 supports dynamic voltage scaling to optimize its power consumption in Run mode. The voltage from the internal low-drop regulator that supplies the logic can be adjusted according to the system's maximum operating frequency and the external voltage supply.

There are three power consumption ranges:

- Range 1 ( $V_{DD}$  range limited to 1.71-3.6 V), with the CPU running at up to 32 MHz
- Range 2 (full  $V_{DD}$  range), with a maximum CPU frequency of 16 MHz
- Range 3 (full  $V_{DD}$  range), with a maximum CPU frequency limited to 4.2 MHz

Seven low-power modes are provided to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

- **Sleep mode**

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs. Sleep mode power consumption at 16 MHz is about 1 mA with all peripherals off.

- **Low-power run mode**

This mode is achieved with the multispeed internal (MSI) RC oscillator set to the low-speed clock (max 131 kHz), execution from SRAM or Flash memory, and internal regulator in low-power mode to minimize the regulator's operating current. In Low-power run mode, the clock frequency and the number of enabled peripherals are both limited.

- **Low-power sleep mode**

This mode is achieved by entering Sleep mode with the internal voltage regulator in low-power mode to minimize the regulator's operating current. In Low-power sleep mode, both the clock frequency and the number of enabled peripherals are limited; a typical example would be to have a timer running at 32 kHz.

When wakeup is triggered by an event or an interrupt, the system reverts to the Run mode with the regulator on.

- **Stop mode with RTC**

The Stop mode achieves the lowest power consumption while retaining the RAM and register contents and real time clock. All clocks in the  $V_{CORE}$  domain are stopped, the PLL, MSI RC, HSE and HSI RC oscillators are disabled. The LSE or LSI is still running. The voltage regulator is in the low-power mode.

Some peripherals featuring wakeup capability can enable the HSI RC during Stop mode to detect their wakeup condition.

The device can be woken up from Stop mode by any of the EXTI line, in 3.5  $\mu$ s, the processor can serve the interrupt or resume the code. The EXTI line source can be any GPIO. It can be the PVD output, the comparator 1 event or comparator 2 event

**Table 3. Functionalities depending on the operating power supply range (continued)**

Operating power supply range	Functionalities depending on the operating power supply range		
	ADC operation	Dynamic voltage scaling range	I/O operation
$V_{DD} = 1.8$ to $2.0$ V <sup>(1)</sup>	Conversion time up to 1.14 Msp/s	Range1, range 2 or range 3	Degraded speed performance
$V_{DD} = 2.0$ to $2.4$ V	Conversion time up to 1.14 Msp/s	Range 1, range 2 or range 3	Full speed operation
$V_{DD} = 2.4$ to $3.6$ V	Conversion time up to 1.14 Msp/s	Range 1, range 2 or range 3	Full speed operation

1. CPU frequency changes from initial to final must respect the condition:  $f_{CPU\ initial} < 4f_{CPU\ initial}$ . It must also respect 5  $\mu$ s delay between two changes. For example to switch from 4.2 MHz to 32 MHz, you can switch from 4.2 MHz to 16 MHz, wait 5  $\mu$ s, then switch from 16 MHz to 32 MHz.

**Table 4. CPU frequency range depending on dynamic voltage scaling**

CPU frequency range	Dynamic voltage scaling range
16 MHz to 32 MHz (1ws) 32 kHz to 16 MHz (0ws)	Range 1
8 MHz to 16 MHz (1ws) 32 kHz to 8 MHz (0ws)	Range 2
32 kHz to 4.2 MHz (0ws)	Range 3

**Table 5. Functionalities depending on the working mode (from Run/active down to standby) <sup>(1)(2)</sup>**

IPs	Run/Active	Sleep	Low-power run	Low-power sleep	Stop		Standby	
						Wakeup capability		Wakeup capability
CPU	Y	-	Y	-	-	-	-	-
Flash memory	O	O	O	O	-	-	-	-
RAM	Y	Y	Y	Y	Y	-	-	-
Backup registers	Y	Y	Y	Y	Y	-	Y	-
EEPROM	O	O	O	O	-	-	-	-
Brown-out reset (BOR)	O	O	O	O	O	O	O	O
DMA	O	O	O	O	-	-	-	-

**Table 5. Functionalities depending on the working mode  
(from Run/active down to standby) (continued)<sup>(1)(2)</sup>**

IPs	Run/Active	Sleep	Low-power run	Low-power sleep	Stop	Standby
					Wakeup capability	Wakeup capability
Wakeup time to Run mode	0 $\mu$ s	6 CPU cycles	3 $\mu$ s	7 CPU cycles	5 $\mu$ s	65 $\mu$ s
Consumption $V_{DD}=1.8$ to 3.6 V (Typ)	Down to 128 $\mu$ A/MHz (from Flash)	Down to 31 $\mu$ A/MHz (from Flash)	Down to 7 $\mu$ A	Down to 3.8 $\mu$ A	0.29 $\mu$ A (No RTC) $V_{DD}=1.8$ V	0.18 $\mu$ A (No RTC) $V_{DD}=1.8$ V
					0.54 $\mu$ A (with RTC) $V_{DD}=1.8$ V	0.41 $\mu$ A (with RTC) $V_{DD}=1.8$ V
					0.34 $\mu$ A (No RTC) $V_{DD}=3.0$ V	0.23 $\mu$ A (No RTC) $V_{DD}=3.0$ V
					0.67 $\mu$ A (with RTC) $V_{DD}=3.0$ V	0.53 $\mu$ A (with RTC) $V_{DD}=3.0$ V

- Legend:  
 "Y" = Yes (enable).  
 "O" = Optional, can be enabled/disabled by software  
 "-" = Not available
- The consumption values given in this table are preliminary data given for indication. They are subject to slight changes.
- Some peripherals with wakeup from Stop capability can request HSI to be enabled. In this case, HSI is woken up by the peripheral, and only feeds the peripheral which requested it. HSI is automatically put off when the peripheral does not need it anymore.
- UART and LPUART reception is functional in Stop mode. It generates a wakeup interrupt on Start. To generate a wakeup on address match or received frame event, the LPUART can run on LSE clock while the UART has to wake up or keep running the HSI clock.
- I2C address detection is functional in Stop mode. It generates a wakeup interrupt in case of address match. It will wake up the HSI during reception.

## 3.2 Interconnect matrix

Several peripherals are directly interconnected. This allows autonomous communication between peripherals, thus saving CPU resources and power consumption. In addition, these hardware connections allow fast and predictable latency.

Depending on peripherals, these interconnections can operate in Run, Sleep, Low-power run, Low-power sleep and Stop modes.

**Table 6. STM32L011x3/4 peripherals interconnect matrix**

Interconnect source	Interconnect destination	Interconnect action	Run	Sleep	Low-power run	Low-power sleep	Stop
COMPx	TIM2, TIM21	Timer input channel, trigger from analog signals comparison	Y	Y	Y	Y	-
	LPTIM1	Timer input channel, trigger from analog signals comparison	Y	Y	Y	Y	Y

(rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 38 GPIOs can be connected to the 16 configurable interrupt/event lines. The 10 other lines are connected to PVD, RTC, USART, I2C, LPUART, LPTIM or comparator events.

## 3.8 Memories

The STM32L011x3/4 devices have the following features:

- 2 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states. With the enhanced bus matrix, operating the RAM does not lead to any performance penalty during accesses to the system bus (AHB and APB buses).
- The non-volatile memory is divided into three arrays:
  - 8 or 16 Kbytes of embedded Flash program memory
  - 512 bytes of data EEPROM
  - Information block containing 32 user and factory options bytes plus 4 Kbytes of system memory

The user options bytes are used to write-protect or read-out protect the memory (with 4 Kbyte granularity) and/or readout-protect the whole memory with the following options:

- **Level 0:** no protection
- **Level 1:** memory readout protected.  
The Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
- **Level 2:** chip readout protected, debug features (Cortex-M0+ serial wire) and boot in RAM selection disabled (debugline fuse)

The whole non-volatile memory embeds the error correction code (ECC) feature.

## 3.9 Direct memory access (DMA)

The flexible 5-channel, general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I<sup>2</sup>C, USART, LPUART, general-purpose timers, and ADC.



### 3.14.1 General-purpose timers (TIM2, TIM21)

There are three synchronizable general-purpose timers embedded in the STM32L011x3/4 devices (see [Table 7](#) for differences).

#### TIM2

TIM2 is based on 16-bit auto-reload up/down counter. It includes a 16-bit prescaler. It features four independent channels each for input capture/output compare, PWM or one-pulse mode output.

The TIM2 general-purpose timers can work together or with the TIM21 general-purpose timer via the Timer Link feature for synchronization or event chaining. Its counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs.

TIM2 has independent DMA request generation.

This timer is capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

#### TIM21

TIM21 is based on a 16-bit auto-reload up/down counter. It includes a 16-bit prescaler. It has two independent channels for input capture/output compare, PWM or one-pulse mode output. It can work together and be synchronized with TIM2 full-featured general-purpose timer.

It can also be used as simple timebase and be clocked by the LSE clock source (32.768 kHz) to provide independent timebase from the main CPU clock.

### 3.14.2 Low-power Timer (LPTIM)

The low-power timer has an independent clock and is running also in Stop mode if it is clocked by LSE, LSI or an external clock. It is able to wakeup the devices from Stop mode.

This low-power timer supports the following features:

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- Configurable output: pulse, PWM
- Continuous / one shot mode
- Selectable software / hardware input trigger
- Selectable clock source
  - Internal clock source: LSE, LSI, HSI or APB clock
  - External clock source over LPTIM1 input (working even with no internal clock source running, used by the Pulse Counter Application)
- Programmable digital glitch filter
- Encoder mode

### 3.14.3 SysTick timer

This timer is dedicated to the OS, but could also be used as a standard downcounter. It is based on a 24-bit downcounter with autoreload capability and a programmable clock source. It features a maskable system interrupt generation when the counter reaches '0'.

### 3.17 Serial wire debug port (SW-DP)

An ARM SW-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.

Table 13. Pin definitions

Pin number							Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
TSSOP14	UFQFPN20	TSSOP20	UFQFPN28	LQFP32	UFQFPN32 <sup>(1)</sup>	WLCSP25					Alternate functions	Additional functions
2	1	2	2	2	2	B5	PC14- OSC32_IN	I/O	FT	-	-	OSC32_IN
3	2	3	3	3	3	C5	PC15- OSC32_OUT	I/O	TC	-	-	OSC32_OUT
4	3	4	4	4	4	D5	NRST	I/O	RST	(2)	-	-
10	4	5	5	5	5	C4	VDDA	S	-	(3)(4)	-	-
5	5	6	6	6	6	E5	PA0-CK_IN	I/O	TTa	-	USART2_RX, LPTIM1_IN1, TIM2_CH1, USART2_CTS, TIM2_ETR, LPUART1_RX, COMP1_OUT	COMP1_INM, ADC_IN0, RTC_TAMP2/WKU P1/CK_IN
6	6	7	7	7	7	B4	PA1	I/O	FT	-	EVENTOUT, LPTIM1_IN2, TIM2_CH2, I2C1_SMBA, USART2_RTS, TIM21_ETR, LPUART1_TX	COMP1_INP, ADC_IN1
-	-	8	8	8	8	D4	PA2	I/O	TTa	-	TIM21_CH1, TIM2_CH3, USART2_TX, LPUART1_TX, COMP2_OUT	COMP2_INM, ADC_IN2, RTC_TAMP3/RTC_ TS/RTC_OUT/WKU P3
-	-	9	9	9	9	E4	PA3	I/O	FT	-	TIM21_CH2, TIM2_CH4, USART2_RX, LPUART1_RX	COMP2_INP, ADC_IN3
7	7	10	10	10	10	B3	PA4	I/O	TTa	-	SPI1_NSS, LPTIM1_IN1, LPTIM1_ETR, I2C1_SCL, USART2_CK, TIM2_ETR, LPUART1_TX, COMP2_OUT	COMP1_INM, COMP2_INM, ADC_IN4

Table 22. Current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions		f <sub>HCLK</sub>	Typ	Max <sup>(1)</sup>	Unit
I <sub>DD</sub> (Run from Flash)	Supply current in Run mode, code executed from Flash	f <sub>HSE</sub> = f <sub>HCLK</sub> up to 16 MHz included, f <sub>HSE</sub> = f <sub>HCLK</sub> /2 above 16 MHz (PLL ON) <sup>(2)</sup>	Range 3, V <sub>CORE</sub> =1.2 V, VOS[1:0]=11	1 MHz	140	180	μA
				2 MHz	245	290	
				4 MHz	460	540	
			Range 2, V <sub>CORE</sub> =1.5 V, VOS[1:0]=10,	4 MHz	0.56	0.65	mA
				8 MHz	1.1	1.3	
				16 MHz	2.1	2.4	
			Range 1, V <sub>CORE</sub> =1.8 V, VOS[1:0]=01	8 MHz	1.3	1.6	
				16 MHz	2.6	3	
				32 MHz	5.3	6.5	
		MSI clock	Range 3, V <sub>CORE</sub> =1.2 V, VOS[1:0]=11	65 kHz	34.5	54	μA
				524 kHz	86	120	
				4.2 MHz	505	560	
		HSI clock	Range 2, V <sub>CORE</sub> =1.5 V, VOS[1:0]=10,	16 MHz	2.2	2.6	mA
				32 MHz	5.4	5.9	

1. Guaranteed by characterization results at 125 °C, not tested in production, unless otherwise specified.

2. Oscillator bypassed (HSEBYP = 1 in RCC\_CR register).

Table 23. Current consumption in Run mode vs code type, code with data processing running from Flash

Symbol	Parameter	Conditions			f <sub>HCLK</sub>	Typ	Unit
I <sub>DD</sub> (Run from Flash)	Supply current in Run mode, code executed from Flash	f <sub>HSE</sub> = f <sub>HCLK</sub> up to 16 MHz included, f <sub>HSE</sub> = f <sub>HCLK</sub> /2 above 16 MHz (PLL ON) <sup>(1)</sup>	Range 3, V <sub>CORE</sub> =1.2 V, VOS[1:0]=11	Dhrystone	4 MHz	460	μA
				CoreMark		440	
				Fibonacci		330	
				while(1)		305	
				while(1), prefetch OFF		320	
			Range 1, VOS[1:0]=01, V <sub>CORE</sub> =1.8 V	Dhrystone	32 MHz	5.4	mA
				CoreMark		4.9	
				Fibonacci		5	
				while(1)		4.35	
				while(1), prefetch OFF		3.7	

1. Oscillator bypassed (HSEBYP = 1 in RCC\_CR register).

Figure 17.  $I_{DD}$  vs  $V_{DD}$ , at  $T_A = -40/25/55/ 85/105/125\text{ }^{\circ}\text{C}$ , Low-power run mode, code running from RAM, Range 3, MSI (Range 0) at 64 KHz, 0 WS

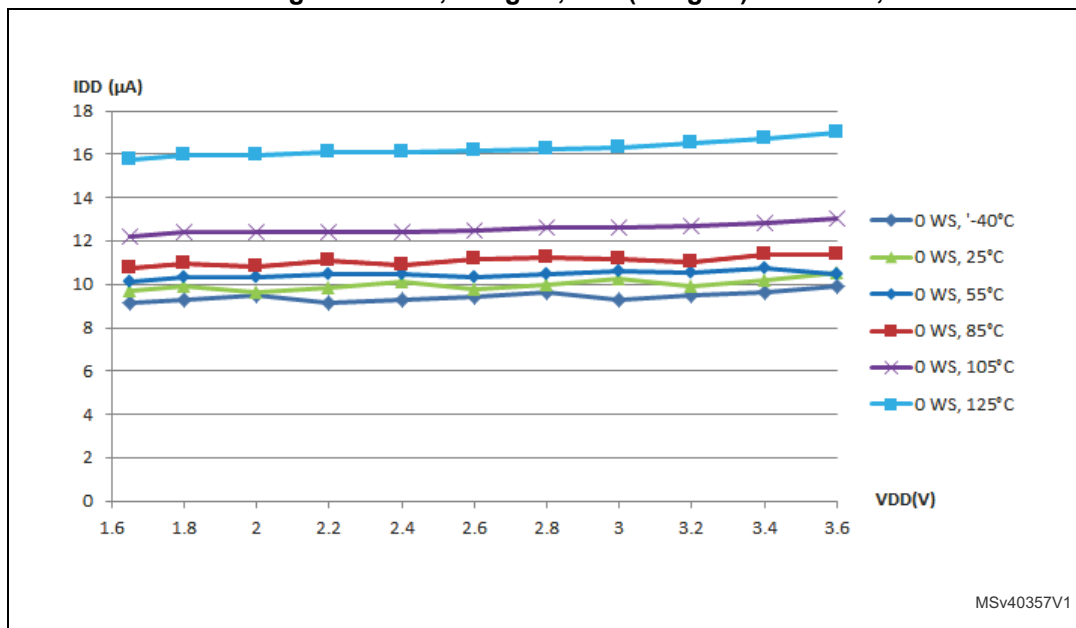


Table 28. Current consumption in Low-power Sleep mode

Symbol	Parameter	Conditions			Typ	Max <sup>(1)</sup>	Unit
I <sub>DD</sub> (LP Sleep)	Supply current in Low-power sleep mode	All peripherals OFF, V <sub>DD</sub> from 1.65 V to 3.6 V	MSI clock, 65 kHz f <sub>HCLK</sub> = 32 kHz Flash OFF	T <sub>A</sub> = -40 °C to 25 °C	2.5 <sup>(2)</sup>	-	μA
			MSI clock, 65 kHz f <sub>HCLK</sub> = 32 kHz Flash ON	T <sub>A</sub> = -40 °C to 25 °C	13	19	
				T <sub>A</sub> = 85 °C	15.5	20	
				T <sub>A</sub> = 105 °C	17.5	22	
				T <sub>A</sub> = 125 °C	21	29	
			MSI clock, 65 kHz f <sub>HCLK</sub> = 65 kHz, Flash ON	T <sub>A</sub> = -40 °C to 25 °C	13.5	19	
				T <sub>A</sub> = 85 °C	16	20	
				T <sub>A</sub> = 105 °C	18	22	
				T <sub>A</sub> = 125 °C	21.5	29	
			MSI clock, 131 kHz f <sub>HCLK</sub> = 131 kHz, Flash ON	T <sub>A</sub> = -40 °C to 25 °C	15.5	21	
				T <sub>A</sub> = 55 °C	17	22	
				T <sub>A</sub> = 85 °C	18	23	
				T <sub>A</sub> = 105 °C	19.5	24	
				T <sub>A</sub> = 125 °C	23.5	31	

1. Guaranteed by characterization results at  $125\text{ }^{\circ}\text{C}$ , not tested in production, unless otherwise specified.

2. As the CPU is in Sleep mode, the difference between the current consumption with Flash memory ON and OFF (nearly  $12\text{ }\mu\text{A}$ ) is the same whatever the clock frequency.

### Low-speed external user clock generated from an external source

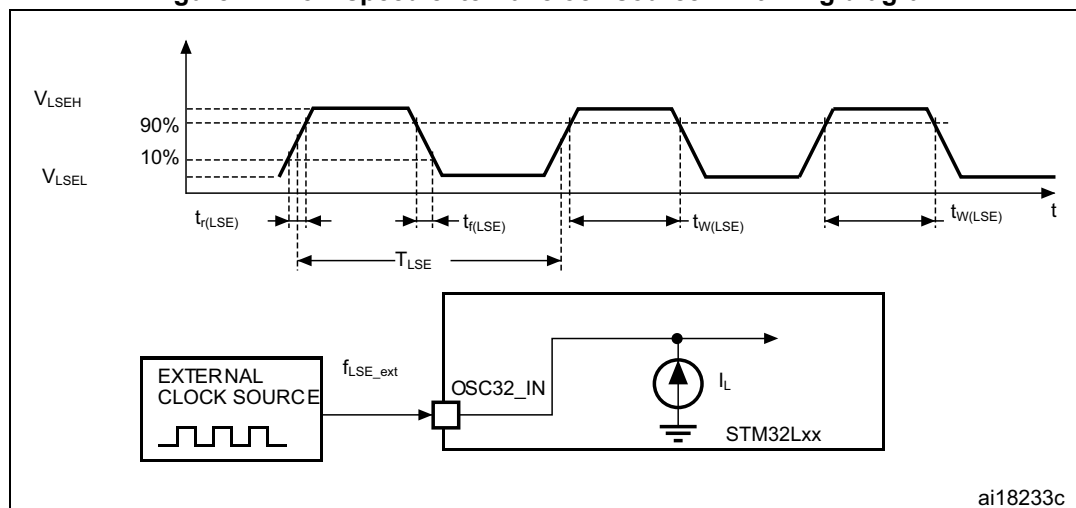
The characteristics given in the following table result from tests performed using a low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in [Table 18](#).

**Table 36. Low-speed external user clock characteristics<sup>(1)</sup>**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{LSE\_ext}$	User external clock source frequency	-	-	32.768	1000	kHz
$V_{LSEH}$	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-	$V_{DD}$	V
$V_{LSEL}$	OSC32_IN input pin low level voltage		$V_{SS}$	-	$0.3V_{DD}$	
$t_{w(LSE)}$ $t_{w(LSE)}$	OSC32_IN high or low time		465	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time		-	-	10	
$C_{IN(LSE)}$	OSC32_IN input capacitance	-	-	0.6	-	pF
$DuCy(LSE)$	Duty cycle	-	45	-	55	%
$I_L$	OSC32_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	$\pm 1$	$\mu A$

1. Guaranteed by design, not tested in production

**Figure 21. Low-speed external clock source AC timing diagram**



### Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in [Table 37](#). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization

time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

**Table 37. LSE oscillator characteristics<sup>(1)</sup>**

Symbol	Parameter	Conditions <sup>(2)</sup>	Min <sup>(2)</sup>	Typ	Max	Unit
$f_{LSE}$	LSE oscillator frequency		-	32.768	-	kHz
$G_m$	Maximum critical crystal transconductance	LSEDRV[1:0]=00 lower driving capability	-	-	0.5	$\mu A/V$
		LSEDRV[1:0]=01 medium low driving capability	-	-	0.75	
		LSEDRV[1:0]=10 medium high driving capability	-	-	1.7	
		LSEDRV[1:0]=11 higher driving capability	-	-	2.7	
$t_{SU(LSE)}$ <sup>(3)</sup>	Startup time	$V_{DD}$ is stabilized	-	2	-	s

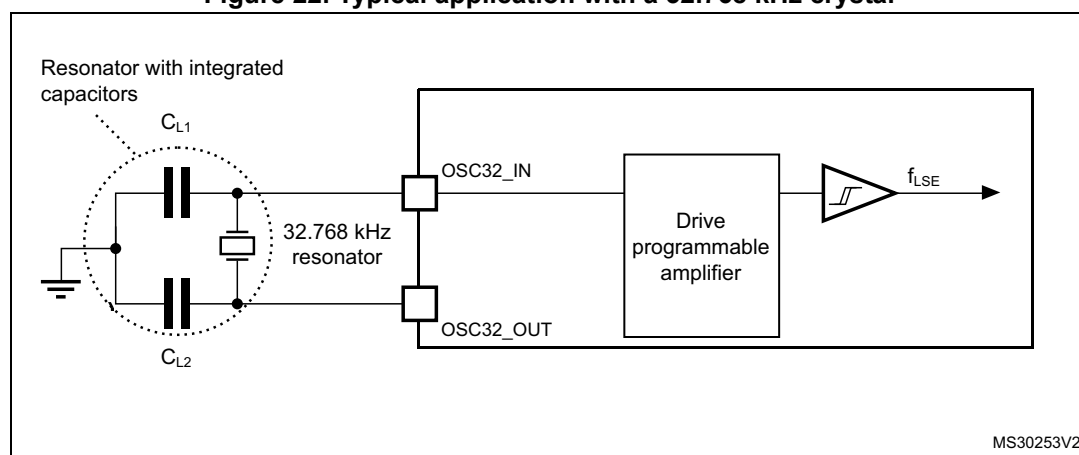
1. Guaranteed by design, not tested in production.

2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 "Oscillator design guide for ST microcontrollers".

3. Guaranteed by characterization results, not tested in production.  $t_{SU(LSE)}$  is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer. To increase speed, address a lower-drive quartz with a high-driver mode.

**Note:** For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website <http://www.st.com>.

**Figure 22. Typical application with a 32.768 kHz crystal**



**Note:** An external resistor is not required between  $OSC32\_IN$  and  $OSC32\_OUT$  and it is forbidden to add one.

### Input/output AC characteristics

The definition and values of input/output AC characteristics are given in [Figure 26](#) and [Table 52](#), respectively.

Unless otherwise specified, the parameters given in [Table 52](#) are derived from tests performed under ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 18](#).

**Table 52. I/O AC characteristics<sup>(1)(2)</sup>**

OSPEEDRx [1:0] bit value <sup>(1)</sup>	Symbol	Parameter	Conditions	Min	Max <sup>(3)</sup>	Unit
00	$f_{\max(\text{IO})\text{out}}$	Maximum frequency <sup>(4)</sup>	$C_L = 50 \text{ pF}$ , $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	400	kHz
			$C_L = 50 \text{ pF}$ , $V_{DD} = 1.65 \text{ V to } 2.7 \text{ V}$	-	100	
	$t_{f(\text{IO})\text{out}}$ $t_{r(\text{IO})\text{out}}$	Output rise and fall time	$C_L = 50 \text{ pF}$ , $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	125	ns
			$C_L = 50 \text{ pF}$ , $V_{DD} = 1.65 \text{ V to } 2.7 \text{ V}$	-	320	
01	$f_{\max(\text{IO})\text{out}}$	Maximum frequency <sup>(4)</sup>	$C_L = 50 \text{ pF}$ , $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	2	MHz
			$C_L = 50 \text{ pF}$ , $V_{DD} = 1.65 \text{ V to } 2.7 \text{ V}$	-	0.6	
	$t_{f(\text{IO})\text{out}}$ $t_{r(\text{IO})\text{out}}$	Output rise and fall time	$C_L = 50 \text{ pF}$ , $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	30	ns
			$C_L = 50 \text{ pF}$ , $V_{DD} = 1.65 \text{ V to } 2.7 \text{ V}$	-	65	
10	$F_{\max(\text{IO})\text{out}}$	Maximum frequency <sup>(4)</sup>	$C_L = 50 \text{ pF}$ , $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	10	MHz
			$C_L = 50 \text{ pF}$ , $V_{DD} = 1.65 \text{ V to } 2.7 \text{ V}$	-	2	
	$t_{f(\text{IO})\text{out}}$ $t_{r(\text{IO})\text{out}}$	Output rise and fall time	$C_L = 50 \text{ pF}$ , $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	13	ns
			$C_L = 50 \text{ pF}$ , $V_{DD} = 1.65 \text{ V to } 2.7 \text{ V}$	-	28	
11	$F_{\max(\text{IO})\text{out}}$	Maximum frequency <sup>(4)</sup>	$C_L = 30 \text{ pF}$ , $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	35	MHz
			$C_L = 50 \text{ pF}$ , $V_{DD} = 1.65 \text{ V to } 2.7 \text{ V}$	-	10	
	$t_{f(\text{IO})\text{out}}$ $t_{r(\text{IO})\text{out}}$	Output rise and fall time	$C_L = 30 \text{ pF}$ , $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	6	ns
			$C_L = 50 \text{ pF}$ , $V_{DD} = 1.65 \text{ V to } 2.7 \text{ V}$	-	17	
-	$t_{\text{EXTI}pw}$	Pulse width of external signals detected by the EXTI controller	-	8	-	ns

1. The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the line reference manual for a description of GPIO Port configuration register.
2. BOOT0/PB9 maximum input frequency is 10 kHz ( $1.65 \text{ V} < V_{DD} < 2.7 \text{ V}$ ) and 5 MHz ( $2.7 \text{ V} < V_{DD} < 3.6 \text{ V}$ ).
3. Guaranteed by design. Not tested in production.
4. The maximum frequency is defined in [Figure 26](#).



### SPI characteristics

Unless otherwise specified, the parameters given in the following tables are derived from tests performed under ambient temperature,  $f_{PCLKx}$  frequency and  $V_{DD}$  supply voltage conditions summarized in [Table 18](#).

Refer to [Section 6.3.12: I/O current injection characteristics](#) for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

**Table 65. SPI characteristics in voltage Range 1 <sup>(1)</sup>**

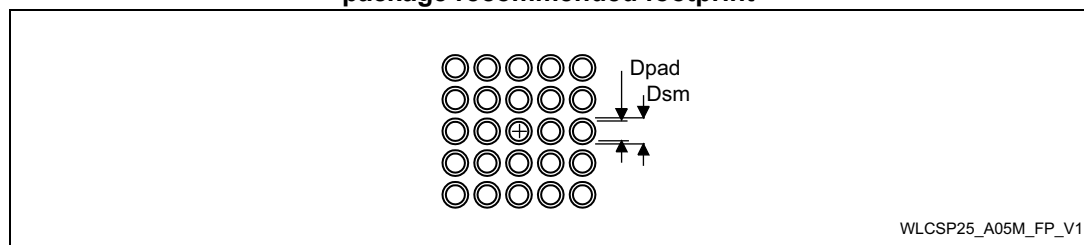
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{SCK}$ $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	-	16	MHz
		Slave mode receiver			16	
		Slave mode Transmitter $1.71 < V_{DD} < 3.6V$	-	-	12 <sup>(2)</sup>	
		Slave mode Transmitter $2.7 < V_{DD} < 3.6V$	-	-	16 <sup>(2)</sup>	
Duty <sub>(SCK)</sub>	Duty cycle of SPI clock frequency	Slave mode	30	50	70	%
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI presc = 2	4T <sub>pclk</sub>	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI presc = 2	2T <sub>pclk</sub>	-	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode	T <sub>pclk</sub> -2	T <sub>pclk</sub>	T <sub>pclk</sub> +2	
$t_{su(MI)}$	Data input setup time	Master mode	3	-	-	
$t_{su(SI)}$		Slave mode	3	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	3.5	-	-	
$t_{h(SI)}$		Slave mode	0	-	-	
$t_{a(SO)}$	Data output access time	Slave mode	15	-	36	
$t_{dis(SO)}$	Data output disable time	Slave mode	10	-	30	
$t_{v(SO)}$	Data output valid time	Slave mode $1.71 < V_{DD} < 3.6V$	-	14	35	
		Slave mode $2.7 < V_{DD} < 3.6V$	-	14	20	
$t_{v(MO)}$		Master mode	-	4	6	
$t_{h(SO)}$	Data output hold time	Slave mode	10	-	-	
$t_{h(MO)}$		Master mode	3	-	-	

1. Guaranteed by characterization results, not tested in production.
2. The maximum SPI clock frequency in slave transmitter mode is determined by the sum of  $t_{v(SO)}$  and  $t_{su(MI)}$  which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having  $t_{su(MI)} = 0$  while Duty<sub>(SCK)</sub> = 50%.

**Table 70. WLCSP25 - 25-ball, 2.133 x 2.070 mm, 0.4 mm pitch wafer level chip scale package mechanical data (continued)**

G	-	0.235	-	-	0.0093	-
aaa	-	-	0.100	-	-	0.0039
bbb	-	-	0.100	-	-	0.0039
ccc	-	-	0.100	-	-	0.0039
ddd	-	-	0.050	-	-	0.0020
eee	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Back side coating.
3. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

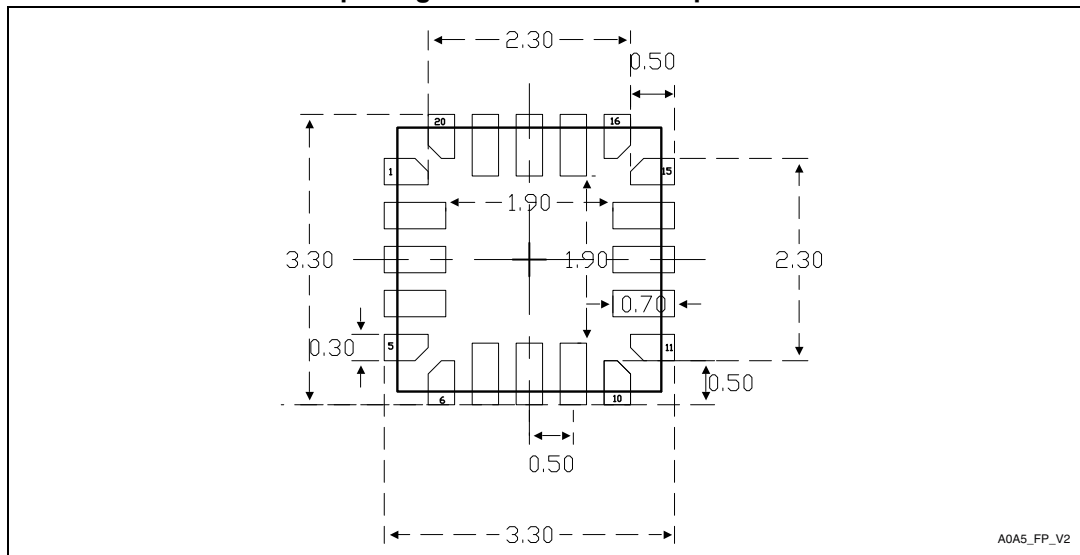
**Figure 40. WLCSP25 - 25-ball, 2.133 x 2.070 mm, 0.4 mm pitch wafer level chip scale package recommended footprint****Table 71. WLCSP25 recommended PCB design rules (0.4 mm pitch)**

Dimension	Recommended values
Pitch	0.4 mm
Dpad	0.225 mm
Dsm	0.290 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.250 mm
Stencil thickness	0.100 mm

**Table 73. UFQFPN20 - 20-lead, 3x3 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data**

Symbol	millimeters			inches <sup>(1)</sup>		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
A3	-	0.152	-	-	0.060	-
D	-	3.000	-	-	0.1181	-
E	-	3.000	-	-	0.1181	-
L1	0.500	0.550	0.600	0.0197	0.0217	0.0236
L2	0.300	0.350	0.400	0.0118	0.0138	0.0157
L3	-	0.375	-	-	0.0148	-
L4	-	0.200	-	-	0.0079	-
L5	-	0.150	-	-	0.0059	-
b	0.180	0.250	0.300	0.0071	0.0098	0.0118
e	-	0.500	-	-	0.0197	-
ddd	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

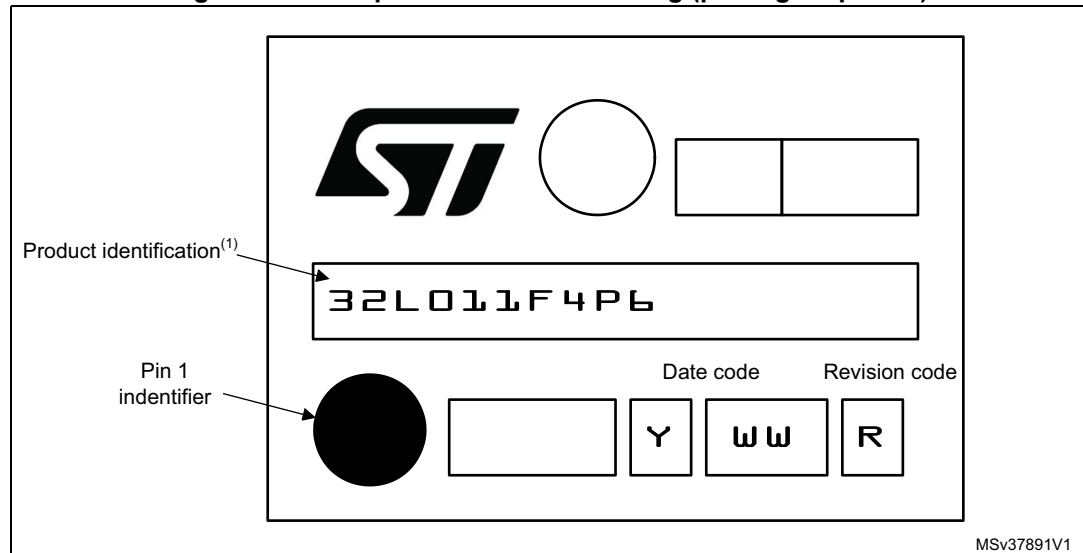
**Figure 46. UFQFPN20 - 20-lead, 3x3 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package recommended footprint**

1. Dimensions are expressed in millimeters.

## Device marking

The following figure gives an example of topside marking versus pin 1 position identifier location.

**Figure 50. Example of TSSOP20 marking (package top view)**

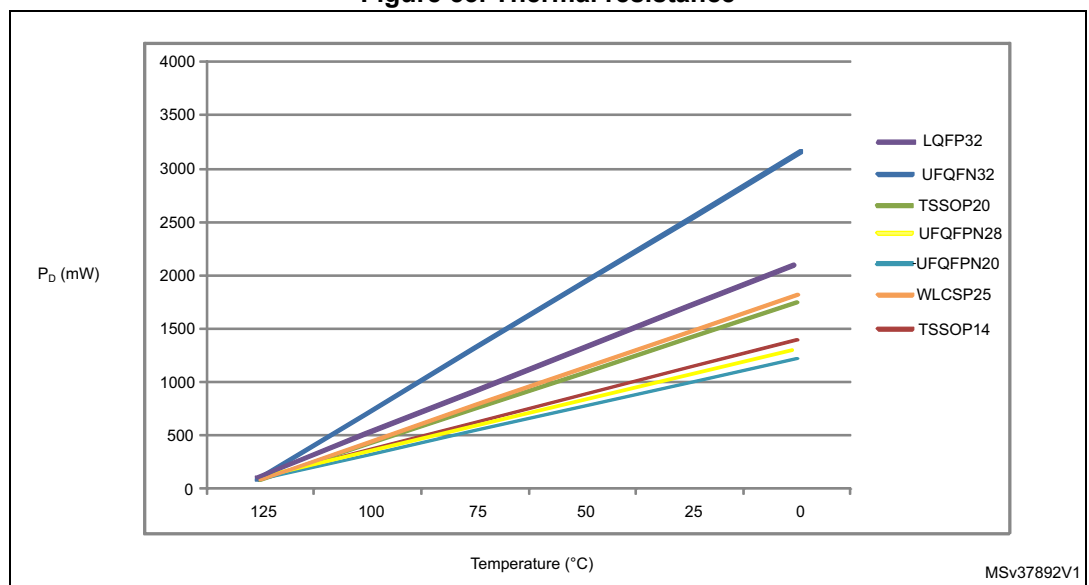


1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 76. Thermal characteristics

Symbol	Parameter	Value	Unit
$\Theta_{JA}$	<b>Thermal resistance junction-ambient</b> LQFP32 - 7 x 7 mm / 0.8 mm pitch	60	°C/W
	<b>Thermal resistance junction-ambient</b> UFQFPN32 - 5 x 5 mm / 0.5 mm pitch	39	
	<b>Thermal resistance junction-ambient</b> WLCSP25 - 2.133 x 2.070 mm, 0.4 mm pitch	70	
	<b>Thermal resistance junction-ambient</b> UFQFPN28 - 4 x 4 mm, 0.5 mm pitch	97	
	<b>Thermal resistance junction-ambient</b> UFQFPN20 - 3 x 3 mm, 0.5 mm pitch	102	
	<b>Thermal resistance junction-ambient</b> TSSOP20 - 169 mils	74	
	<b>Thermal resistance junction-ambient</b> TSSOP14 - 169 mils	95	

Figure 53. Thermal resistance



1. The above curves are valid for range 3.

### 7.8.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from [www.jedec.org](http://www.jedec.org).