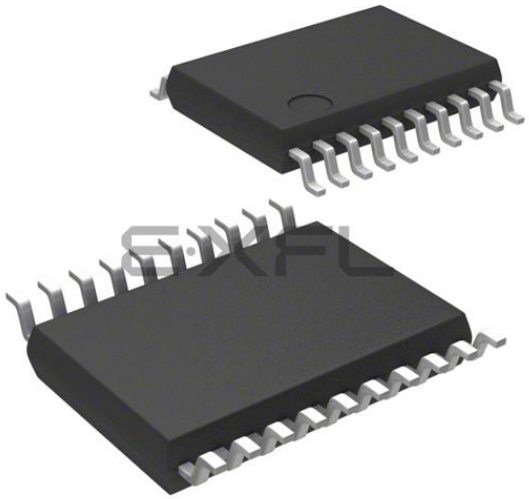


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	16
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 9x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l011f3p6tr

Contents

1 Introduction 9

2 Description 10

2.1 Device overview 11

2.2 Ultra-low-power device continuum 13

3 Functional overview 14

3.1 Low-power modes 14

3.2 Interconnect matrix 18

3.3 ARM® Cortex®-M0+ core 19

3.4 Reset and supply management 20

3.4.1 Power supply schemes 20

3.4.2 Power supply supervisor 20

3.4.3 Voltage regulator 21

3.4.4 Boot modes 21

3.5 Clock management 22

3.6 Low-power real-time clock and backup registers 24

3.7 General-purpose inputs/outputs (GPIOs) 24

3.8 Memories 25

3.9 Direct memory access (DMA) 25

3.10 Analog-to-digital converter (ADC) 26

3.11 Temperature sensor 26

3.11.1 Internal voltage reference (V_{REFINT}) 26

3.12 Ultra-low-power comparators and reference voltage 27

3.13 System configuration controller 27

3.14 Timers and watchdogs 27

3.14.1 General-purpose timers (TIM2, TIM21) 28

3.14.2 Low-power Timer (LPTIM) 28

3.14.3 SysTick timer 28

3.14.4 Independent watchdog (IWDG) 29

3.14.5 Window watchdog (WWDG) 29

3.15 Communication interfaces 29

3.14.4 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 37 kHz internal RC and, as it operates independently of the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes. The counter can be frozen in debug mode.

3.14.5 Window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.15 Communication interfaces

3.15.1 I^2C bus

One I^2C interface (I2C1) can operate in multimaster or slave modes. The I^2C interface can support Standard mode (Sm, up to 100 kbit/s), Fast mode (Fm, up to 400 kbit/s) and Fast Mode Plus (Fm+, up to 1 Mbit/s) with 20 mA output drive on some I/Os.

The I^2C interface supports 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (2 addresses, 1 with configurable mask). They also include programmable analog and digital noise filters.

Table 8. Comparison of I2C analog and digital filters

	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2C peripheral clocks
Benefits	Available in Stop mode	1. Extra filtering capability vs. standard requirements. 2. Stable length
Drawbacks	Variations depending on temperature, voltage, process	Wakeup from Stop on address match is not available when digital filter is enabled.

In addition, I2C1 provides hardware support for SMBus 2.0 and PMBus 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts verifications and ALERT protocol management. I2C1 also has a clock domain independent from the CPU clock, allowing the I2C1 to wake up the MCU from Stop mode on address match.

The I2C interface can be served by the DMA controller.

Refer to *Table 9* for the supported modes and features of I2C interface.

Table 9. STM32L011x3/4 I²C implementation

I2C features[1]	I2C1
7-bit addressing mode	X
10-bit addressing mode	X
Standard mode (up to 100 kbit/s)	X
Fast mode (up to 400 kbit/s)	X
Fast Mode Plus with 20 mA output drive I/Os (up to 1 Mbit/s)	X[2]
Independent clock	X
SMBus	X
Wakeup from STOP	X

1. X = supported.
2. See *Table 13: Pin definitions on page 37* for the list of I/Os that feature Fast Mode Plus capability

3.15.2 Universal synchronous/asynchronous receiver transmitter (USART)

The USART interface (USART2) is able to communicate at speeds of up to 4 Mbit/s.

It provides hardware management of the CTS, RTS and RS485 driver enable (DE) signals, multiprocessor communication mode and single-wire half-duplex communication mode. USART2 also supports Smartcard communication (ISO 7816, T=0 protocol) and IrDA SIR ENDEC.

USART2 interface can be served by the DMA controller.

Table 10 for the supported modes and features of USART interface.

Table 10. USART implementation

USART modes/features[1]	USART2
Hardware flow control for modem	X
Continuous communication using DMA	X
Multiprocessor communication	X
Synchronous mode	-
Smartcard mode	X
Single-wire half-duplex communication	X
IrDA SIR ENDEC block	X
LIN mode	-
Dual clock domain and wakeup from Stop mode	-
Receiver timeout interrupt	-
Modbus communication	-
Auto baud rate detection (4 modes)	-
Driver Enable	X

1. X = supported.

Table 13. Pin definitions (continued)

Pin number							Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
TSSOP14	UFQFPN20	TSSOP20	UFQFPN28	LQFP32	UFQFPN32[1]	WLCSP25					Alternate functions	Additional functions
12	15	18	20	20	20	C2	PA10	I/O	FTf	-	TIM21_CH1, I2C1_SDA, RTC_REFIN, USART2_RX, TIM2_CH3, COMP1_OUT	-
-	-	-	-	21	21	-	PA11	I/O	FT	-	SPI1_MISO, LPTIM1_OUT, EVENTOUT, USART2_CTS, TIM21_CH2, COMP1_OUT	-
-	-	-	-	22	22	-	PA12	I/O	FT	-	SPI1_MOSI, EVENTOUT, USART2_RTS, COMP2_OUT	-
13	16	19	21	23	23	A1	PA13	I/O	FTf	-	SWDIO, LPTIM1_ETR, I2C1_SDA, SPI1_SCK, LPUART1_RX, COMP1_OUT	-
14	17	20	22	24	24	A2	PA14	I/O	FT	-	SWCLK, LPTIM1_OUT, I2C1_SMBA, USART2_TX, SPI1_MISO, LPUART1_TX, COMP2_OUT	-
-	-	-	23	25	25	-	PA15	I/O	FT	-	SPI1_NSS, TIM2_ETR, EVENTOUT, USART2_RX, TIM2_CH1	-
-	-	-	24	26	26	B2	PB3	I/O	FT	-	SPI1_SCK, TIM2_CH2, EVENTOUT	COMP2_INM
-	-	-	25	27	27	-	PB4	I/O	FT	-	SPI1_MISO, EVENTOUT	COMP2_INP

Table 13. Pin definitions (continued)

Pin number							Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
TSSOP14	UFQFPN20	TSSOP20	UFQFPN28	LQFP32	UFQFPN32[1]	WLCSP25					Alternate functions	Additional functions
-	-	-	26	28	28	-	PB5	I/O	FT	-	SPI1_MOSI, LPTIM1_IN1, I2C1_SMBA, TIM21_CH1	COMP2_INP
-	18	-	27	29	29	A3	PB6	I/O	FTf	-	USART2_TX, I2C1_SCL, LPTIM1_ETR, TIM2_CH3, LPUART1_TX	COMP2_INP
-	19	-	28	30	30	A4	PB7	I/O	FTf	-	USART2_RX, I2C1_SDA, LPTIM1_IN2, TIM2_CH4, LPUART1_RX	COMP2_INP, VREF_PVD_IN
1	20	1	1	31	31	A5	PB9-BOOT0	I	B	-	-	BOOT0 (Boot memory selection)
-	-	-	-	-	32	-	PB8	I/O	FTf	-	USART2_TX, EVENTOUT, I2C1_SCL, SPI1_NSS	-
-	-	-	-	32	-	-	VSS	S	-	(5)	-	-
-	-	-	-	1	1	-	VDD	S	-	(6)	-	-

1. V_{SS} pins are connected to the exposed pad (see *Figure 36: UFQFPN32, 5 x 5 mm, 32-pin package outline*).
2. Device reset input/internal reset output (active low).
3. Analog power supply.
4. On TSSOP14 package, V_{DDA} is internally connected to V_{DD}.
5. Digital and analog ground.
6. Digital power supply.

4. Guaranteed by design, not tested in production.
5. Shortest sampling time can be determined in the application by multiple iterations.
6. To guarantee less than 1% VREF_OUT deviation.

6.3.4 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code. The current consumption is measured as described in *Figure 14: Current consumption measurement scheme*.

All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to Dhrystone 2.1 code if not specified otherwise.

The current consumption values are derived from the tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 18: General operating conditions* unless otherwise specified.

The MCU is placed under the following conditions:

- All I/O pins are configured in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time and prefetch is adjusted depending on f_{HCLK} frequency and voltage range to provide the best CPU performance unless otherwise specified.
- When the peripherals are enabled $f_{APB1} = f_{APB2} = f_{APB}$
- When PLL is ON, the PLL inputs are equal to HSI = 16 MHz (if internal clock is used) or HSE = 16 MHz (if HSE bypass mode is used)
- The HSE user clock is applied to CK_IN. It follows the characteristic specified in *Table 35: High-speed external user clock characteristics*
- For maximum current consumption $V_{DD} = V_{DDA} = 3.6$ V is applied to all supply pins
- For typical current consumption $V_{DD} = V_{DDA} = 3.0$ V is applied to all supply pins if not specified otherwise

Table 29. Typical and maximum current consumptions in Stop mode

Symbol	Parameter	Conditions	Typ	Max(1)	Unit
I_{DD} (Stop)	Supply current in Stop mode	T_A = -40°C to 25°C	0.34	0.99	µA
		T_A = 55°C	0.43	1.9	
		T_A= 85°C	0.94	4.2	
		T_A = 105°C	2.0	9	
		T_A = 125°C	4.9	19	

1. Guaranteed by characterization results at 125 °C, not tested in production, unless otherwise specified.

Figure 18. I_{DD} vs V_{DD}, at T_A= -40/25/55/ 85/105/125 °C, Stop mode with RTC enabled and running on LSE Low drive

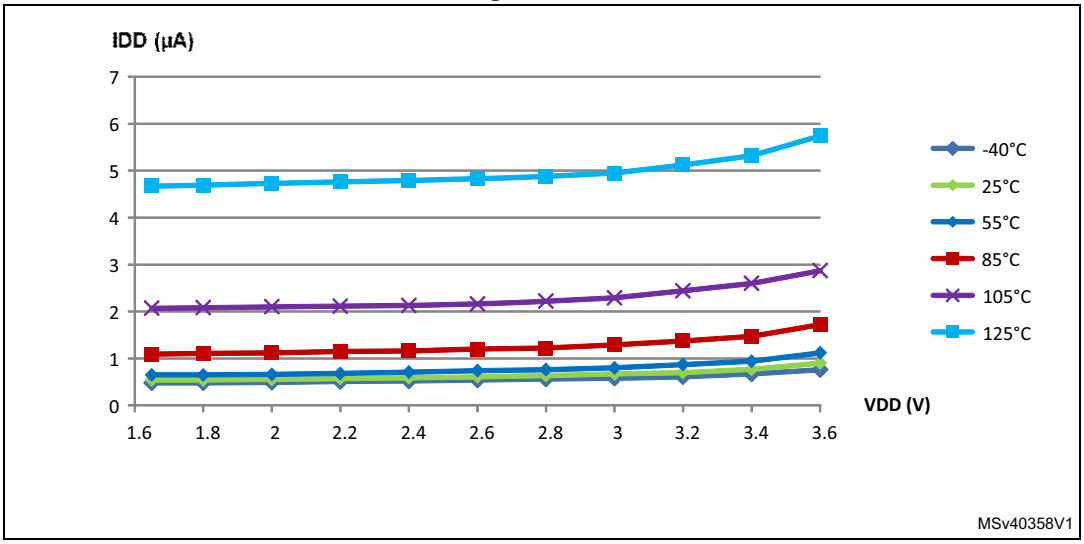
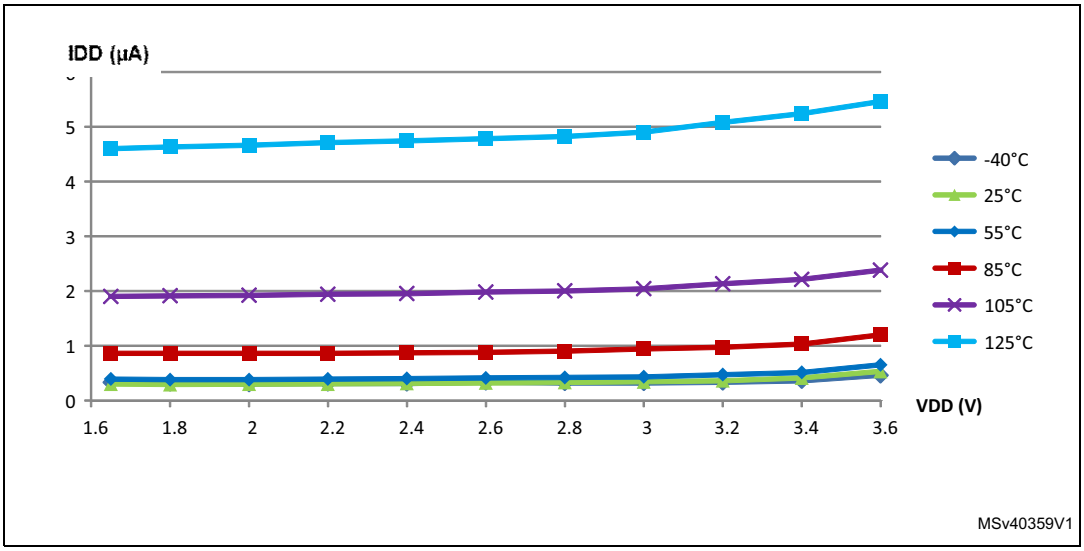


Figure 19. I_{DD} vs V_{DD}, at T_A= -40/25/55/85/105/125 °C, Stop mode with RTC disabled, all clocks OFF



Low-speed external user clock generated from an external source

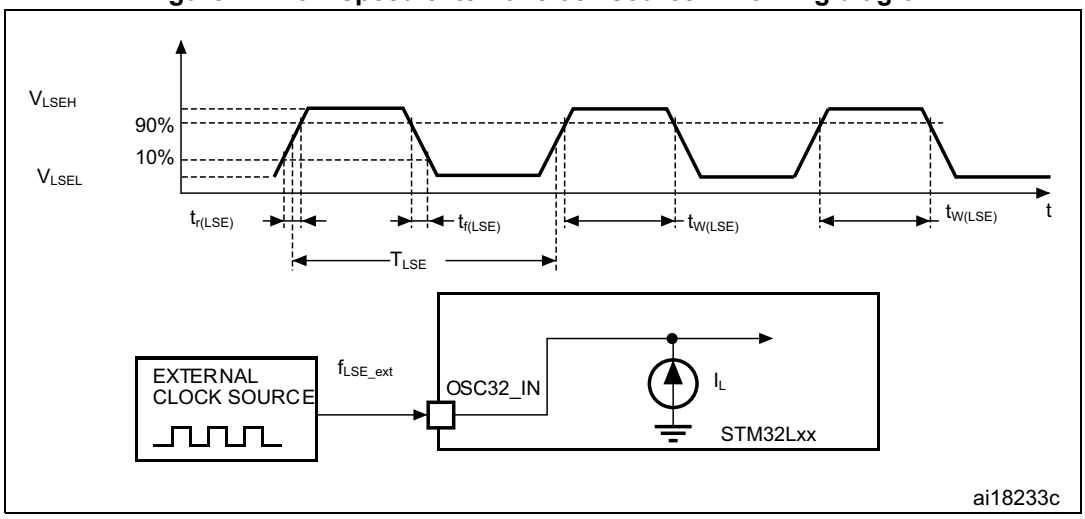
The characteristics given in the following table result from tests performed using a low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 18*.

Table 36. Low-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	-	$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage	-	V_{SS}	-	$0.3V_{DD}$	V
$t_{w(LSE)}$ $t_{w(LSE)}$	OSC32_IN high or low time	-	465	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time	-	-	-	10	ns
$C_{IN(LSE)}$	OSC32_IN input capacitance	-	-	0.6	-	pF
$DuCy_{(LSE)}$	Duty cycle	-	45	-	55	%
I_L	OSC32_IN Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	µA

1. Guaranteed by design, not tested in production

Figure 21. Low-speed external clock source AC timing diagram



Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 37*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization

Low-speed internal (LSI) RC oscillator

Table 39. LSI oscillator characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}(1)	LSI frequency	26	38	56	kHz
D_{LSI}(2)	LSI oscillator frequency drift 0°C ≤ T_A ≤ 85°C	-10	-	4	%
$t_{su(LSI)}$(3)	LSI oscillator startup time	-	-	200	µs
$I_{DD(LSI)}$(3)	LSI oscillator power consumption	-	400	510	nA

1. Guaranteed by test in production.
2. This is a deviation for an individual part, once the initial frequency has been measured.
3. Guaranteed by design, not tested in production.

Multi-speed internal (MSI) RC oscillator

Table 40. MSI oscillator characteristics

Symbol	Parameter	Condition	Typ	Max	Unit
f_{MSI}	Frequency after factory calibration, done at V_{DD}= 3.3 V and T_A = 25 °C	MSI range 0	65.5	-	kHz
		MSI range 1	131	-	
		MSI range 2	262	-	
		MSI range 3	524	-	
		MSI range 4	1.05	-	MHz
		MSI range 5	2.1	-	
		MSI range 6	4.2	-	
ACC_{MSI}	Frequency error after factory calibration	-	±0.5	-	%
$D_{TEMP(MSI)}$(1)	MSI oscillator frequency drift 0 °C ≤ T_A ≤ 85 °C	-	±3	-	%
$D_{VOLT(MSI)}$(1)	MSI oscillator frequency drift 1.65 V ≤ V_{DD} ≤ 3.6 V, T_A = 25 °C	-	-	2.5	%/V
$I_{DD(MSI)}$(2)	MSI oscillator power consumption	MSI range 0	0.75	-	µA
		MSI range 1	1	-	
		MSI range 2	1.5	-	
		MSI range 3	2.5	-	
		MSI range 4	4.5	-	
		MSI range 5	8	-	
		MSI range 6	15	-	

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 46. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. frequency range (32 MHz voltage Range 1)	Unit
S_{EMI}	Peak level	V_{DD} = 3.3 V, T_A = 25 °C, LQFP32 package compliant with IEC 61967-2	0.1 to 30 MHz	-22	dBµV
			30 to 130 MHz	-7	
			130 MHz to 1GHz	-12	
			SAE EMI Level	1	-

6.3.11 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the ANSI/JEDEC standard.

Table 47. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to ANSI/JEDEC JS-001	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to ANSI/ESD STM5.3.1.	C4	500	

1. Guaranteed by characterization results, not tested in production.

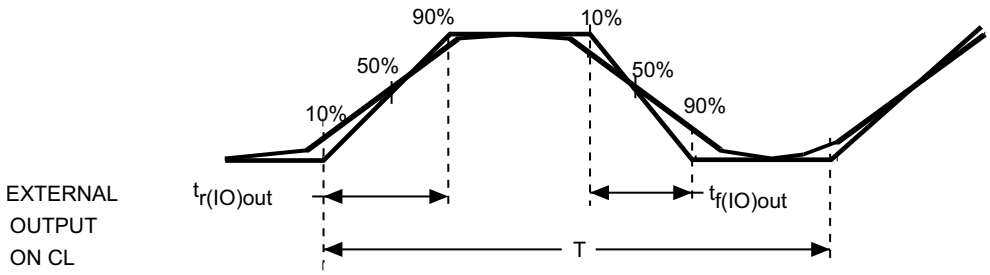
Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Figure 26. I/O AC characteristics definition



Maximum frequency is achieved if (t_r + t_f) ≤ (2/3)T and if the duty cycle is (45-55%) when loaded by CL specified in the table " *I/O AC characteristics*".

ai14131d

6.3.14 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} , except when it is internally driven low (see *Table 53*).

Unless otherwise specified, the parameters given in *Table 53* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 18*.

Table 53. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST input low level voltage	-	-	-	$0.3V_{DD}$	V
$V_{IH(NRST)}$(1)	NRST input high level voltage	-	$0.39V_{DD}$+ 0.59	-	-	
$V_{OL(NRST)}$(1)	NRST output low level voltage	I_{OL} = 2 mA 2.7 V < V_{DD} < 3.6 V	-	-	0.4	
		I_{OL} = 1.5 mA 1.65 V < V_{DD} < 2.7 V	-	-		
$V_{hys(NRST)}$(1)	NRST Schmitt trigger voltage hysteresis	-	-	$10\%V_{DD}$(2)	-	mV
R_{PU}	Weak pull-up equivalent resistor(3)	V_{IN} = V_{SS}	30	45	60	kΩ
$V_{F(NRST)}$(1)	NRST input filtered pulse	-	-	-	50	ns
$V_{NF(NRST)}$(1)	NRST input not filtered pulse	-	350	-	-	ns

1. Guaranteed by design, not tested in production.
2. 200 mV minimum value
3. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is around 10%.

6.3.19 Communications interfaces

I²C interface characteristics

The I²C interface meets the timings requirements of the I²C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm) : with a bit rate up to 100 kbit/s
- Fast-mode (Fm) : with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+) : with a bit rate up to 1 Mbit/s.

The I²C timing requirements are guaranteed by design when the I²C peripheral is properly configured (refer to the reference manual for details) and when the I2CCLK frequency is greater than the minimum given in *Table 63*. The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not "true" open-drain. When configured as open-drain, the PMOS connected between the I/O pin and VDDIOx is disabled, but is still present. Only FTf I/O pins support Fm+ low level output current maximum requirement (refer to *Section 6.3.13: I/O port characteristics* for the I2C I/Os characteristics).

All I²C SDA and SCL I/Os embed an analog filter (see *Table 62* for the analog filter characteristics).

Table 62. I2C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	50(2)	100(3)	ns

1. Guaranteed by design, not tested in production.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered

Table 63. I2C frequency in all I2C modes

Symbol	Parameter	Condition		Min	Unit
f_{I2CCLK}	I2C clock frequency	Standard-mode		2	MHz
		Fast-mode		8	
		Fast-mode Plus	Analog filter ON, DNF = 0	18	
			Analog filter OFF, DNF = 1	16	

Table 66. SPI characteristics in voltage Range 2 (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	-	8	MHz
		Slave mode Transmitter $1.65<V_{DD}<3.6V$			8	
		Slave mode Transmitter $2.7<V_{DD}<3.6V$			8(2)	
$Duty_{(SCK)}$	Duty cycle of SPI clock frequency	Slave mode	30	50	70	%
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI presc = 2	4Tpclk	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI presc = 2	2Tpclk	-	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode	Tpclk-2	Tpclk	Tpclk+2	
$t_{su(MI)}$	Data input setup time	Master mode	3	-	-	
$t_{su(SI)}$		Slave mode	3	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	6	-	-	
$t_{h(SI)}$		Slave mode	2	-	-	
$t_{a(SO}$	Data output access time	Slave mode	18	-	52	
$t_{dis(SO)}$	Data output disable time	Slave mode	12	-	42	
$t_{v(SO)}$	Data output valid time	Slave mode	-	16	33	
		Master mode	-	4	6	
$t_{v(MO)}$	Data output hold time	Slave mode	11	-	-	
$t_{h(SO)}$		Master mode	3	-	-	

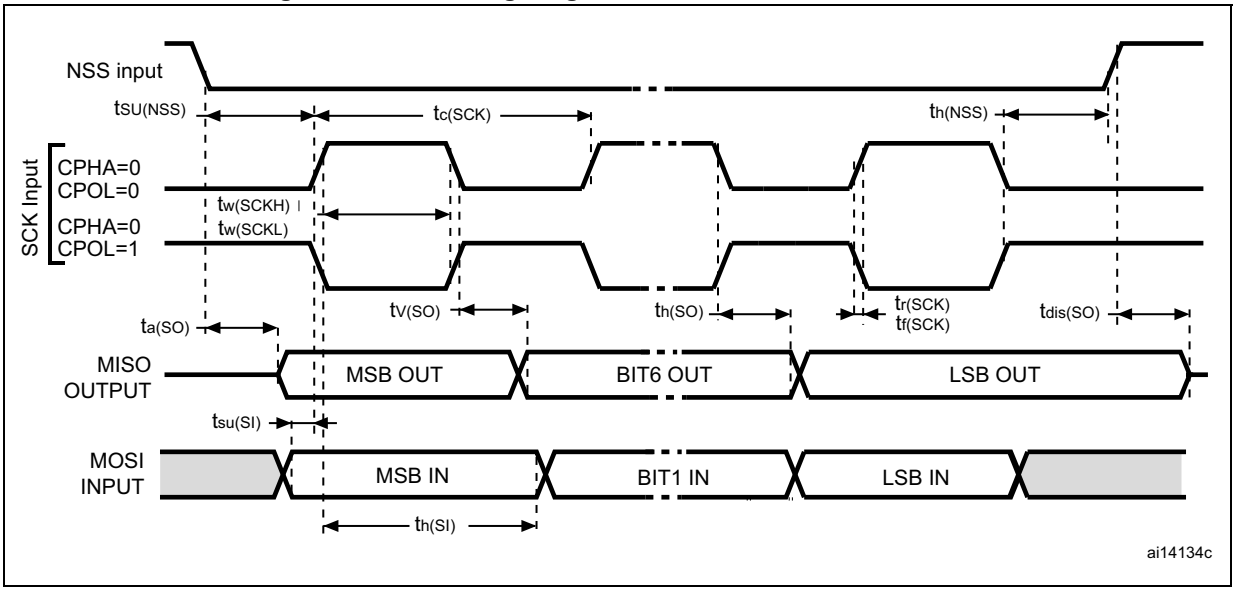
1. Guaranteed by characterization results, not tested in production.
2. The maximum SPI clock frequency in slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)}$ = 0 while $Duty_{(SCK)}$ = 50%.

Table 67. SPI characteristics in voltage Range 3 (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	-	2	MHz
		Slave mode			2(2)	
$Duty_{(SCK)}$	Duty cycle of SPI clock frequency	Slave mode	30	50	70	%
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI presc = 2	4Tpclk	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI presc = 2	2Tpclk	-	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode	Tpclk-2	Tpclk	Tpclk+2	
$t_{su(MI)}$	Data input setup time	Master mode	3	-	-	
$t_{su(SI)}$		Slave mode	3	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	16	-	-	
$t_{h(SI)}$		Slave mode	14	-	-	
$t_{a(SO}$	Data output access time	Slave mode	30	-	70	
$t_{dis(SO)}$	Data output disable time	Slave mode	40	-	80	
$t_{v(SO)}$	Data output valid time	Slave mode	-	26.5	47	
		Master mode	-	4	6	
$t_{v(MO)}$	Data output hold time	Slave mode	20	-	-	
$t_{h(SO)}$		Master mode	3	-	-	

1. Guaranteed by characterization results, not tested in production.
2. The maximum SPI clock frequency in slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)}$ = 0 while $Duty_{(SCK)}$ = 50%.

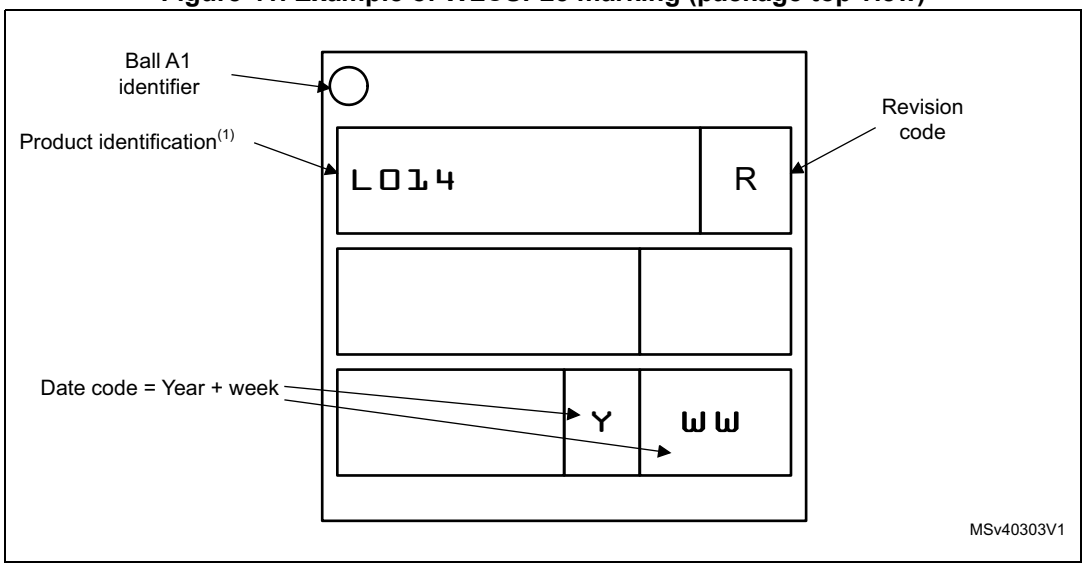
Figure 30. SPI timing diagram - slave mode and CPHA = 0



Device marking

The following figure gives an example of topside marking versus ball A1 position identifier location.

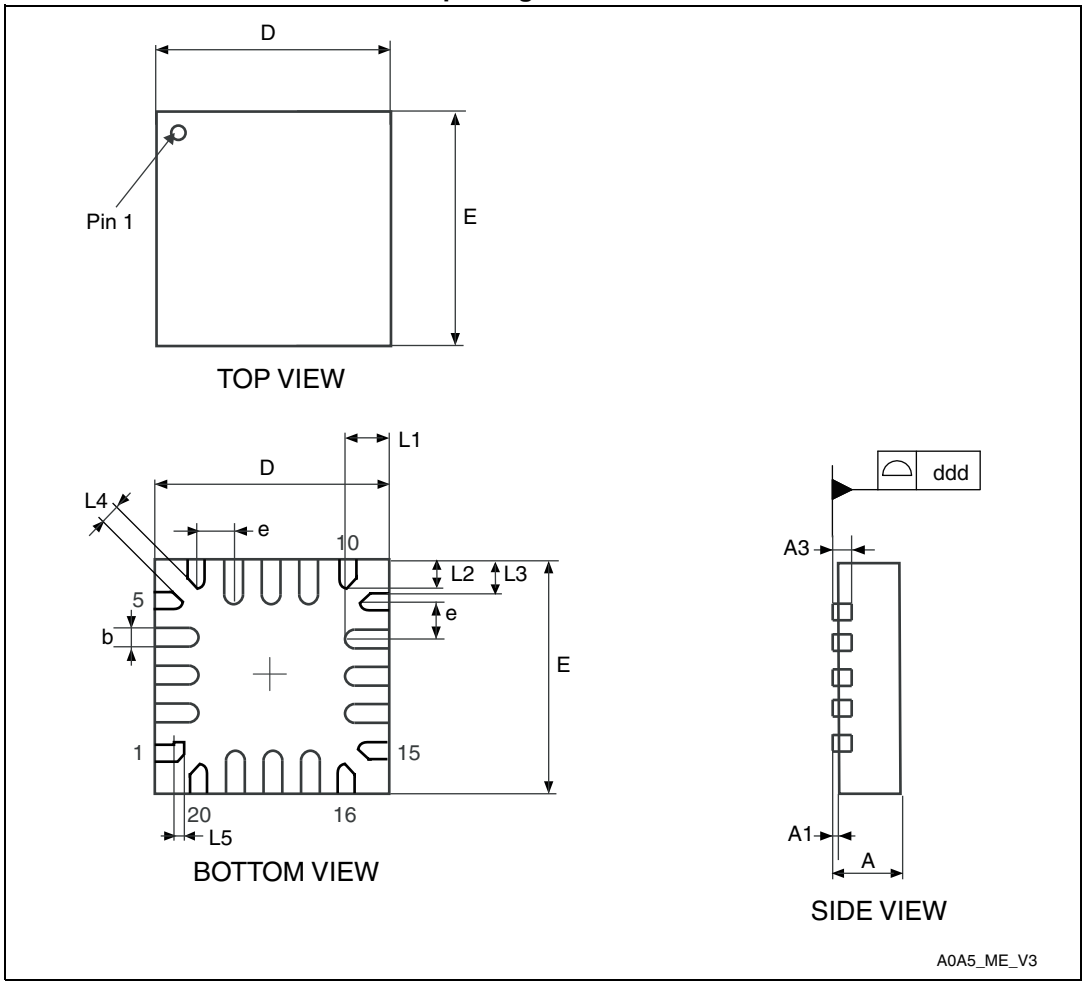
Figure 41. Example of WLCSP25 marking (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

7.5 UFQFPN20 package information

Figure 45. UFQFPN20 - 20-lead, 3x3 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline



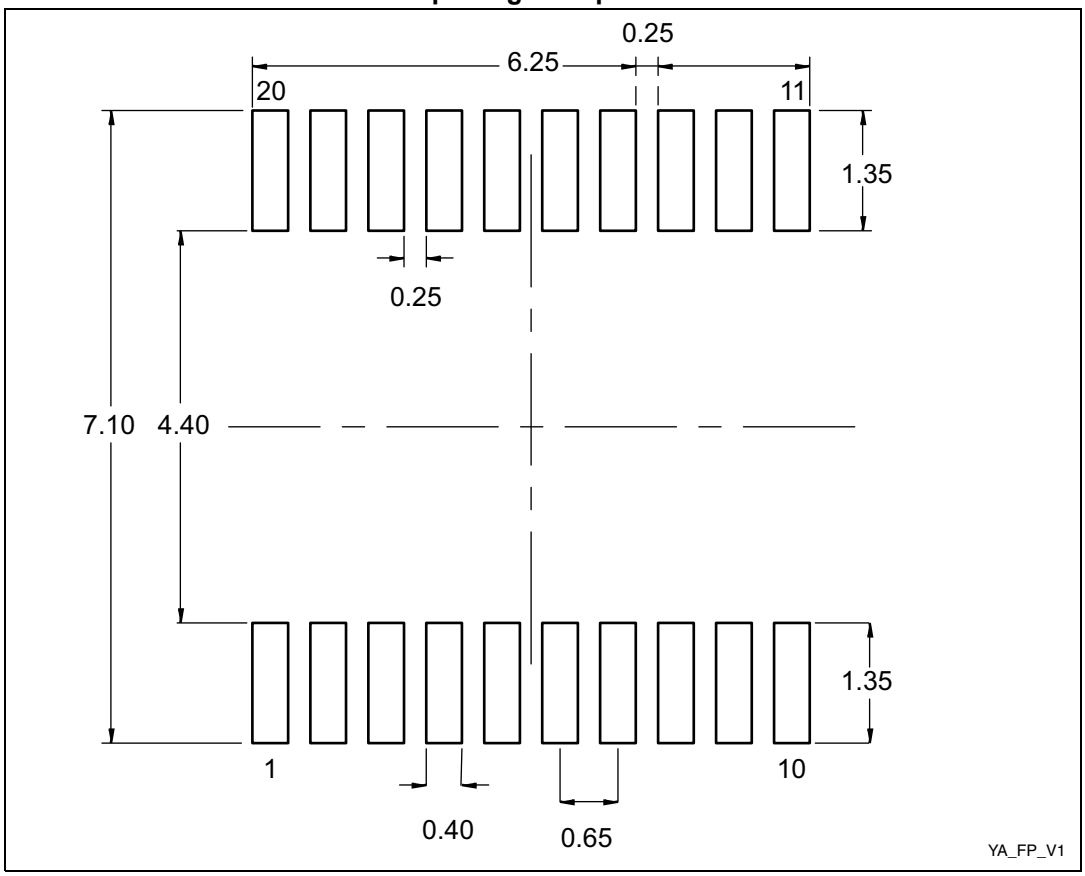
1. Drawing is not to scale.

Table 74. TSSOP20 – 20-lead thin shrink small outline, 6.5 x 4.4 mm, 0.65 mm pitch, package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
k	0°	-	8°	0°	-	8°
aaa	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to four decimal digits.

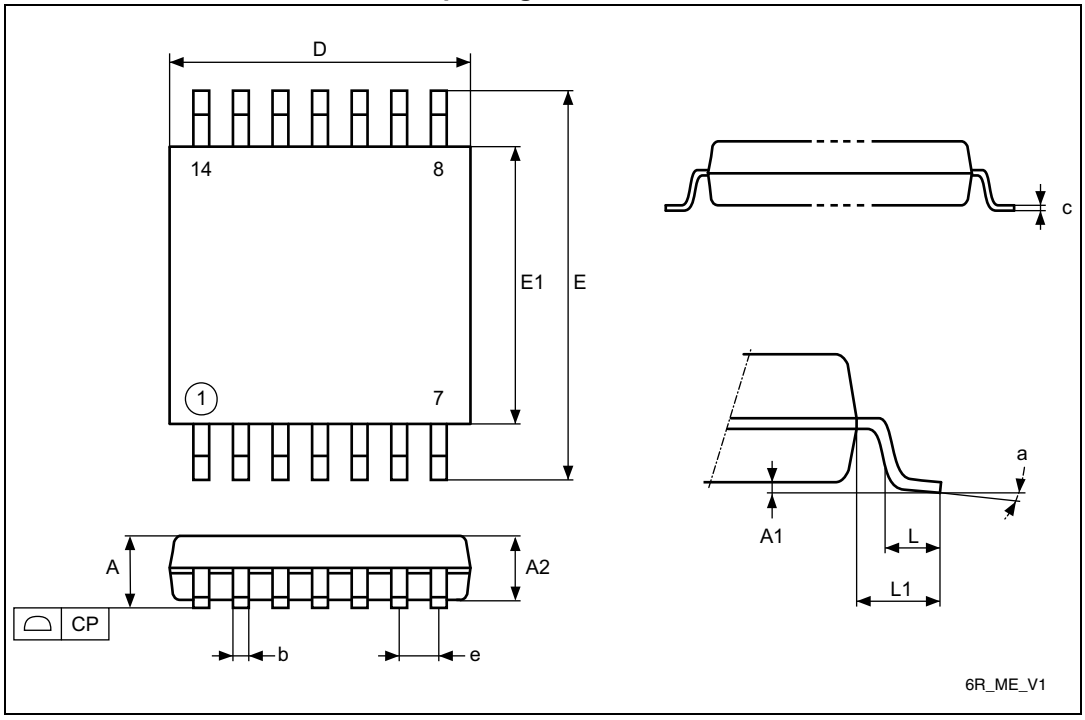
Figure 49. TSSOP20 – 20-lead thin shrink small outline, 6.5 x 4.4 mm, 0.65 mm pitch, package footprint



1. Dimensions are expressed in millimeters.

7.7 TSSOP14 package information

Figure 51.TSSOP14 – 14-lead thin shrink small outline, 5.0 x 4.4 mm, 0.65 mm pitch, package outline



1. Drawing is not to scale.

Table 75. TSSOP14 – 14-lead thin shrink small outline, 5.0 x 4.4 mm, 0.65 mm pitch, package mechanical data

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.200	-	-	0.0472
A1	0.050	-	0.150	0.0020	-	0.0059
A2	0.800	1.000	1.050	0.0315	0.0394	0.0413
b	0.190	-	0.300	0.0075	-	0.0118
c	0.090	-	0.200	0.0035	-	0.0079
CP	-	-	0.100	-	-	0.0039
D	4.900	5.000	5.100	0.1929	0.1969	0.2008
e	-	0.650	-	-	0.0256	-
E	6.200	6.400	6.600	0.2441	0.2520	0.2598
E1	4.300	4.400	4.500	0.1693	0.1732	0.1772
L	0.500	0.600	0.750	0.0197	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
a	0°	-	8°	0°	-	8°

8 Part numbering

Table 77. STM32L011x3/4 ordering information scheme

Example: STM32 L 011 K 4 T 6 D xxx

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

L = Low power

Device subfamily

011 = Access line

Pin count

K = 32 pins

G = 28 pins

E = 25 pins

F = 20 pins

D = 14 pins

Flash memory size

3 = 8 Kbytes

4 = 16 Kbytes

Package

T = LQFP

U = UFQFPN

Y = WLCSP

P = TSSOP

Temperature range

6 = Industrial temperature range, –40 to 85 °C

7 = Industrial temperature range, –40 to 105 °C

3 = Industrial temperature range, –40 to 125 °C

Options

No character = V_{DD} range: 1.8 to 3.6 V and BOR enabled

D = V_{DD} range: 1.65 to 3.6 V and BOR disabled

Packing

TR = tape and reel

No character = tray or tube

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.