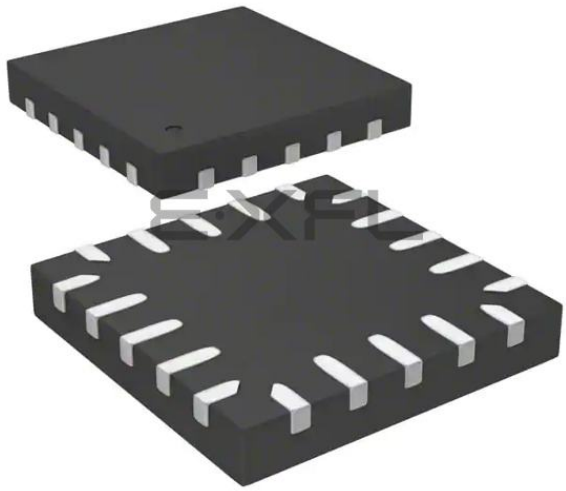

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	16
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 7x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-UFQFN
Supplier Device Package	20-UFQFPN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l011f3u6tr

Table 5. Functionalities depending on the working mode (from Run/active down to standby) (continued)[1][2]

IPs	Run/Active	Sleep	Low-power run	Low-power sleep	Stop		Standby	
						Wakeup capability		Wakeup capability
Programmable Voltage Detector (PVD)	O	O	O	O	O	O	-	-
Power-on/down reset (POR/PDR)	Y	Y	Y	Y	Y	Y	Y	Y
High Speed Internal (HSI)	O	O	-	-	[3]	-	-	-
High Speed External (HSE)	O	O	O	O	-	-	-	-
Low Speed Internal (LSI)	O	O	O	O	O	-	O	-
Low Speed External (LSE)	O	O	O	O	O	-	O	-
Multi-Speed Internal (MSI)	O	O	Y	Y	-	-	-	-
Inter-Connect Controller	Y	Y	Y	Y	Y	-	-	-
RTC	O	O	O	O	O	O	O	-
RTC Tamper	O	O	O	O	O	O	O	O
Auto WakeUp (AWU)	O	O	O	O	O	-	O	O
USART	O	O	O	O	O[4]	O	-	-
LPUART	O	O	O	O	O[4]	O	-	-
SPI	O	O	O	O	-		-	-
I2C	O	O	O	O	O[5]	O	-	-
ADC	O	O	-	-	-	-	-	-
Temperature sensor	O	O	O	O	O	-	-	-
Comparators	O	O	O	O	O	O	-	-
16-bit timers	O	O	O	O	-	-	-	-
LPTIM	O	O	O	O	O	O	-	-
IWDG	O	O	O	O	O	O	O	O
WWDG	O	O	O	O	-	-	-	-
SysTick Timer	O	O	O	O	-	-	-	-
GPIOs	O	O	O	O	O	O	-	2 pins

3.5 Clock management

The clock controller distributes the clocks coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness. It features:

- **Clock prescaler**

  To get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.

- **Safe clock switching**

  Clock sources can be changed safely on the fly in Run mode through a configuration register.

- **Clock management**

  To reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.

- **System clock source**

  Three different clock sources can be used to drive the master clock SYSCLK:

  – 0-32 MHz high-speed external (HSE bypass), that can supply a PLL
  – 16 MHz high-speed internal RC oscillator (HSI), trimmable by software, that can supply a PLL
  – Multispeed internal RC oscillator (MSI), trimmable by software, able to generate 7 frequencies (65 kHz, 131 kHz, 262 kHz, 524 kHz, 1.05 MHz, 2.1 MHz, 4.2 MHz). When a 32.768 kHz clock source is available in the system (LSE), the MSI frequency can be trimmed by software down to a ±0.5% accuracy.

- **Auxiliary clock source**

  Two ultra-low-power clock sources that can be used to drive the real-time clock:

  – 32.768 kHz low-speed external crystal (LSE)
  – 37 kHz low-speed internal RC (LSI), also used to drive the independent watchdog. The LSI clock can be measured using the high-speed internal RC oscillator for greater precision.

- **RTC clock sources**

  The LSI, LSE or HSE sources can be chosen to clock the RTC, whatever the system clock.

- **Startup clock**

  After reset, the microcontroller restarts by default with an internal 2 MHz clock (MSI). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.

- **Clock security system (CSS)**

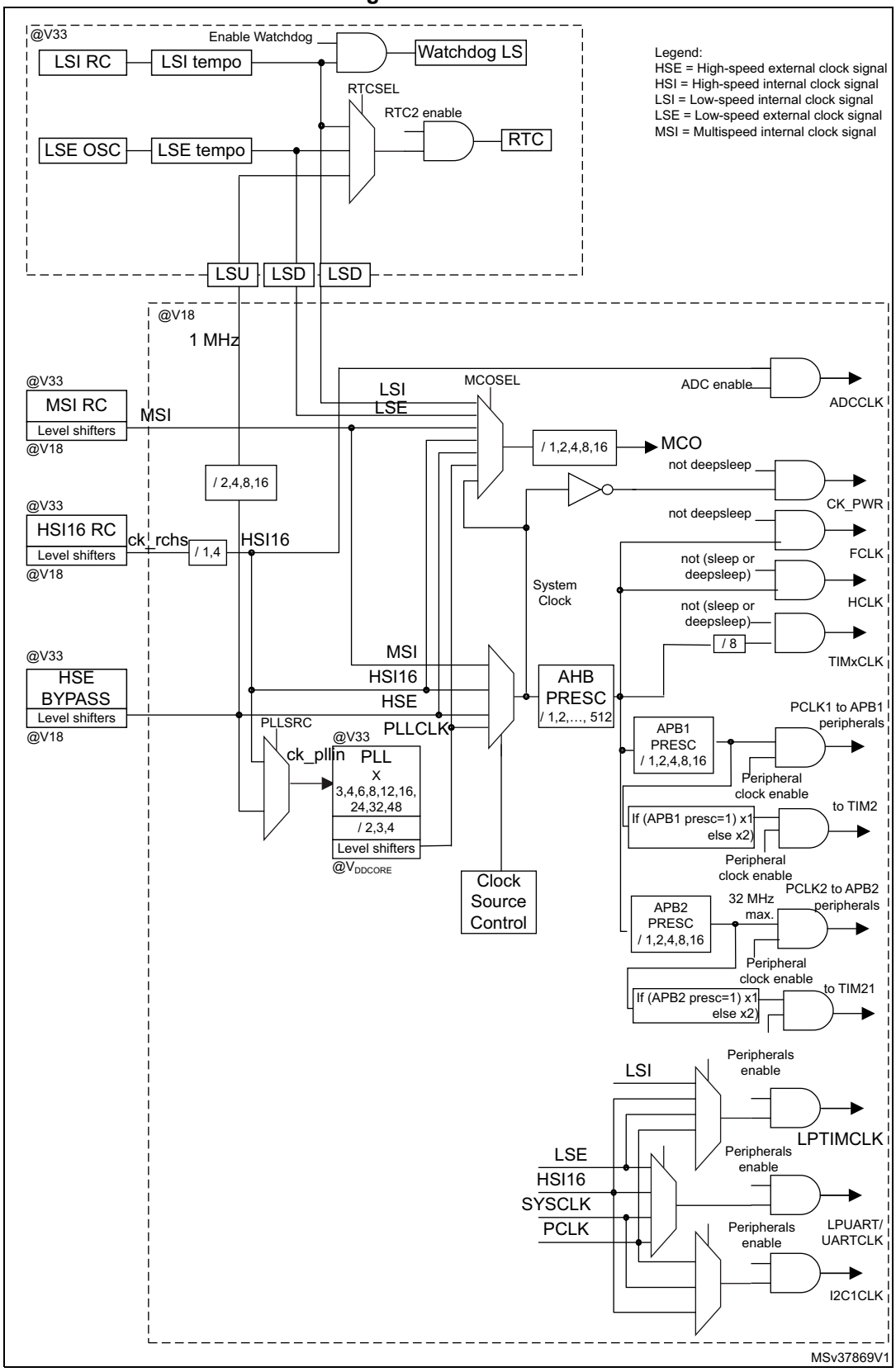
  This feature can be enabled by software. If an LSE clock failure occurs, it provides an interrupt or wakeup event which is generated assuming it has been previously enabled. This feature is not available on the HSE clock.

- **Clock-out capability (MCO: microcontroller clock output)**

  It outputs one of the internal clocks for external use by the application.

Several prescalers allow the configuration of the AHB frequency, each APB (APB1 and APB2) domains. The maximum frequency of the AHB and the APB domains is 32 MHz. See *Figure 2* for details on the clock tree.

Figure 2. Clock tree



3.14.4 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 37 kHz internal RC and, as it operates independently of the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes. The counter can be frozen in debug mode.

3.14.5 Window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.15 Communication interfaces

3.15.1 I^2C bus

One I^2C interface (I2C1) can operate in multimaster or slave modes. The I^2C interface can support Standard mode (Sm, up to 100 kbit/s), Fast mode (Fm, up to 400 kbit/s) and Fast Mode Plus (Fm+, up to 1 Mbit/s) with 20 mA output drive on some I/Os.

The I^2C interface supports 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (2 addresses, 1 with configurable mask). They also include programmable analog and digital noise filters.

Table 8. Comparison of I2C analog and digital filters

	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2C peripheral clocks
Benefits	Available in Stop mode	1. Extra filtering capability vs. standard requirements. 2. Stable length
Drawbacks	Variations depending on temperature, voltage, process	Wakeup from Stop on address match is not available when digital filter is enabled.

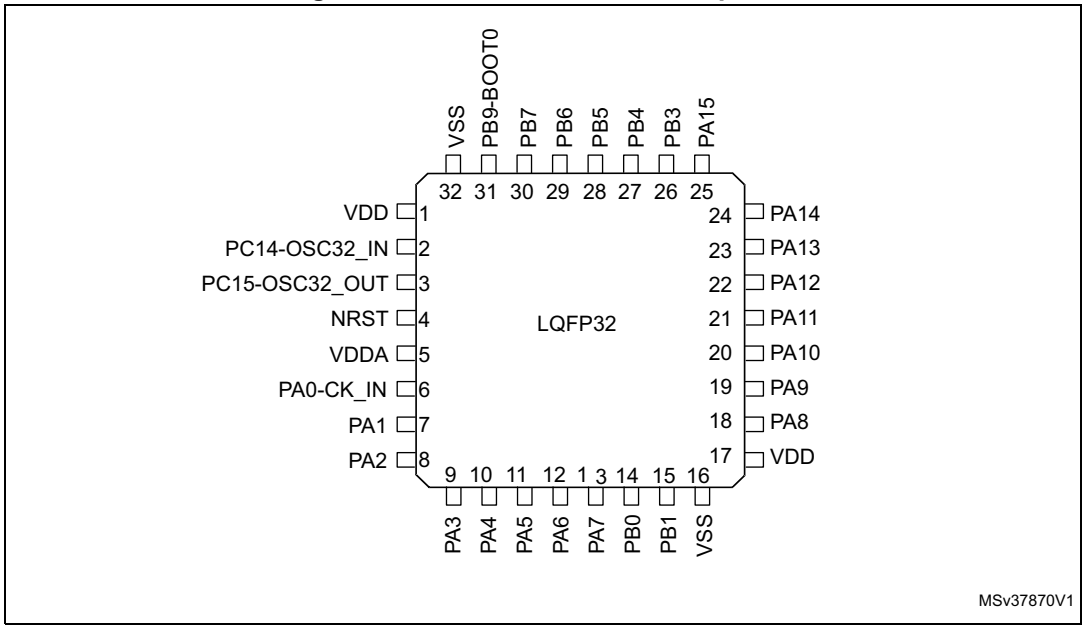
In addition, I2C1 provides hardware support for SMBus 2.0 and PMBus 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts verifications and ALERT protocol management. I2C1 also has a clock domain independent from the CPU clock, allowing the I2C1 to wake up the MCU from Stop mode on address match.

The I2C interface can be served by the DMA controller.

Refer to *Table 9* for the supported modes and features of I2C interface.

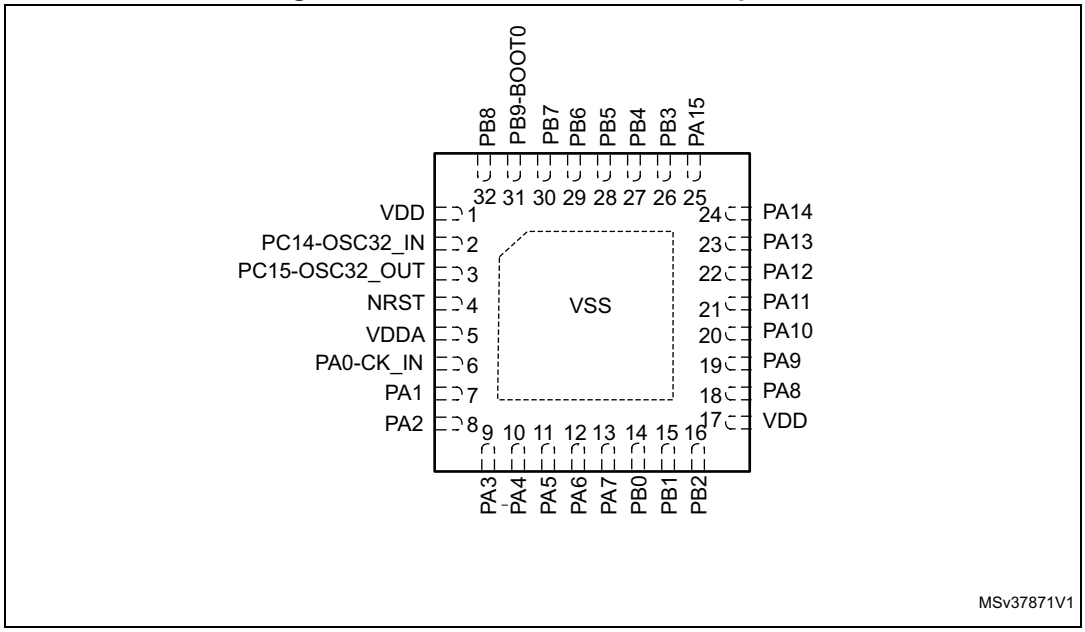
4 Pin descriptions

Figure 3. STM32L011x3/4 LQFP32 pinout



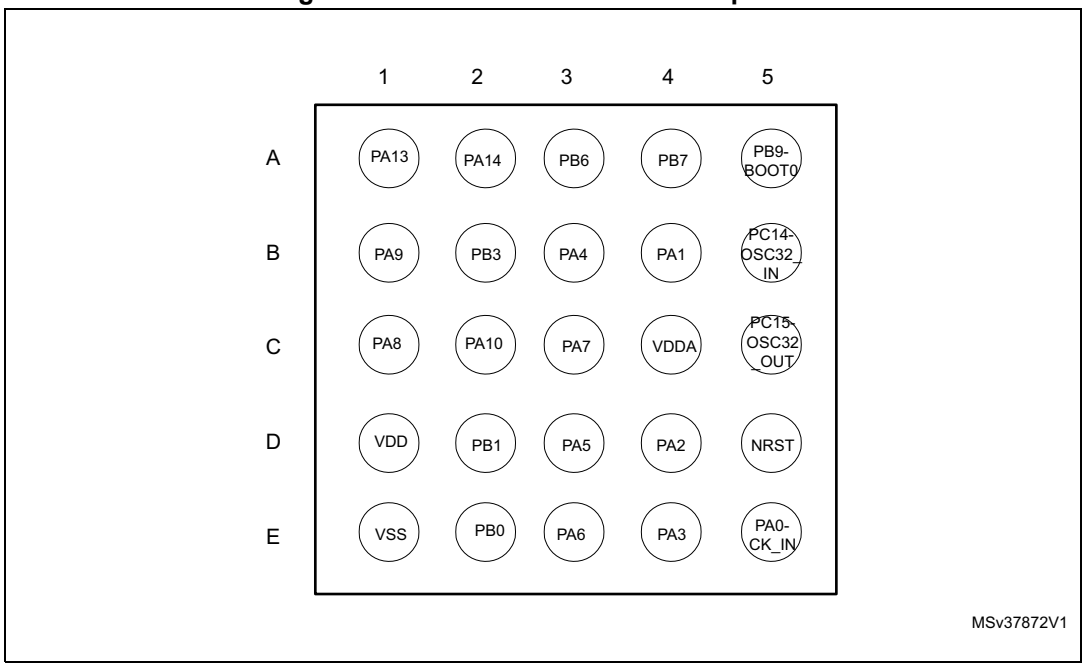
1. The above figure shows the package top view.

Figure 4. STM32L011x3/4 UFQFPN32 pinout



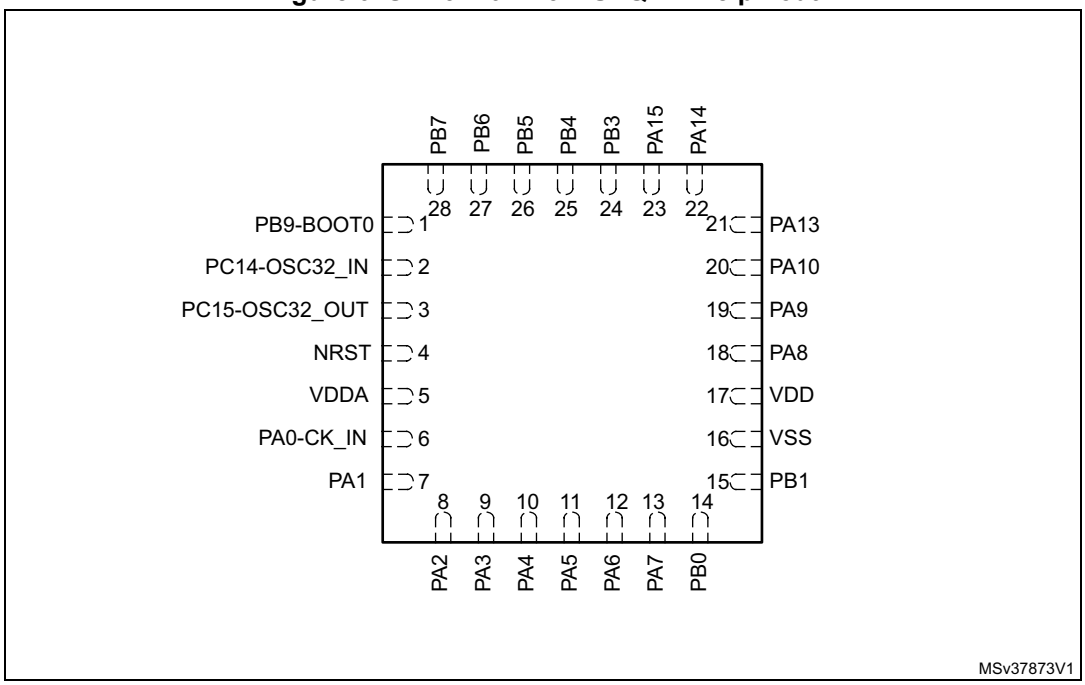
1. The above figure shows the package top view.

Figure 5. STM32L011x3/4 WLCSP25 pinout



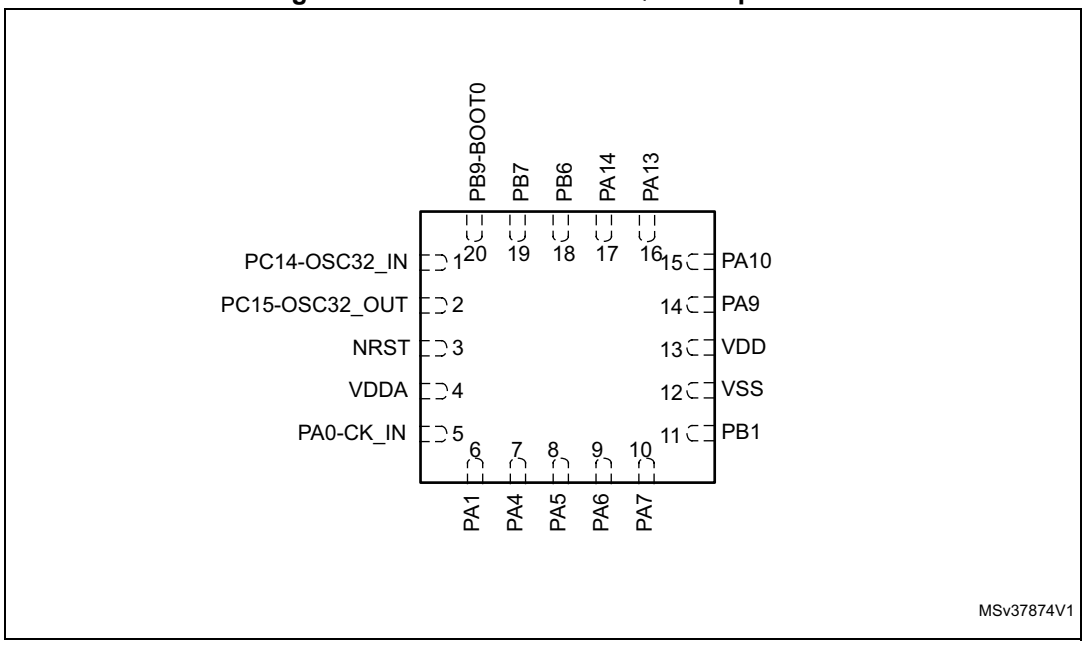
1. The above figure shows the package top view.

Figure 6. STM32L011x3/4 UFQFPN28 pinout



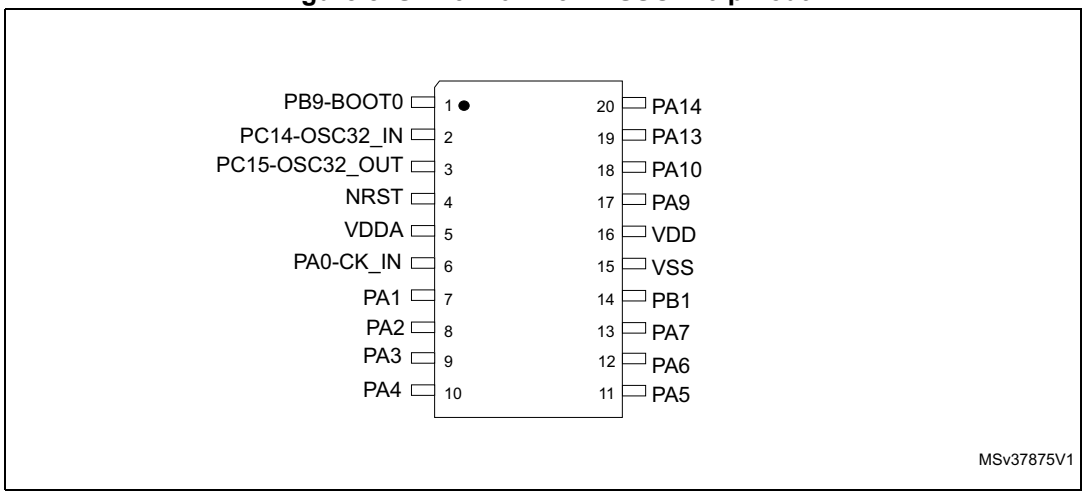
1. The above figure shows the package top view.

Figure 7. STM32L011x3/4 UFQFPN20 pinout



1. The above figure shows the package top view.

Figure 8. STM32L011x3/4 TSSOP20 pinout



1. The above figure shows the package top view.

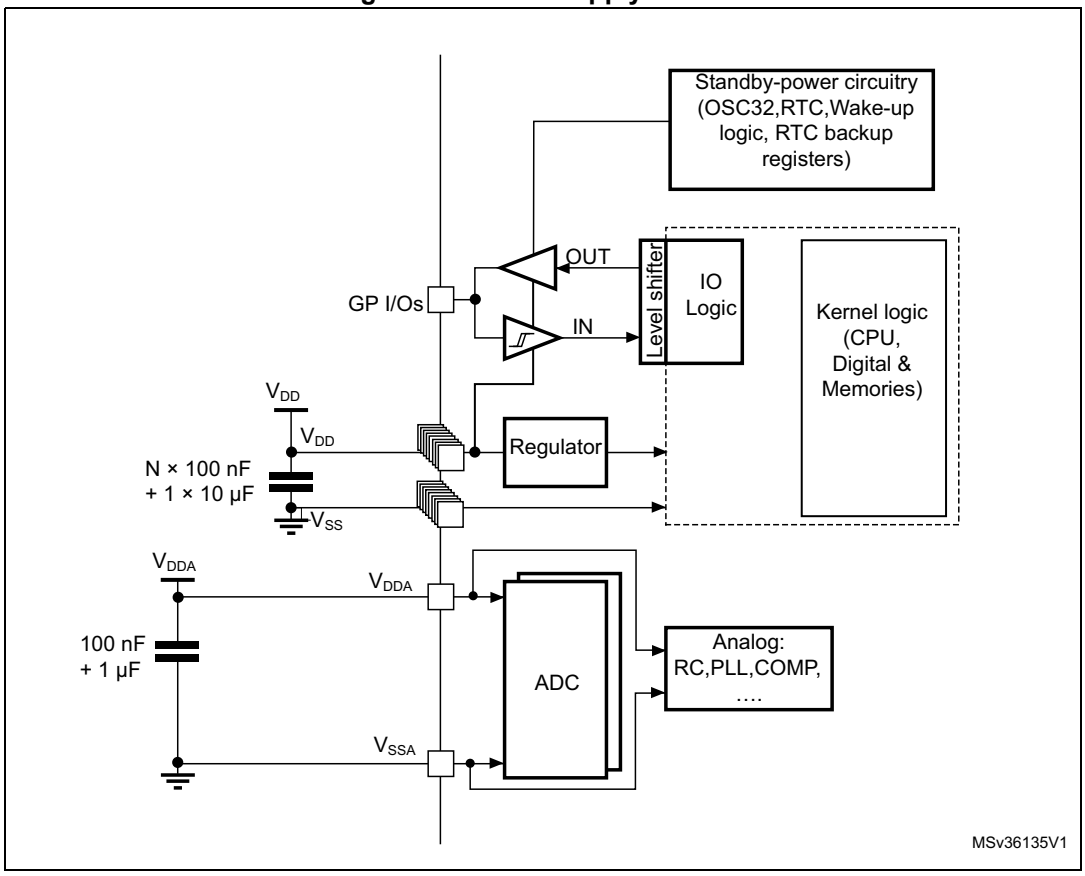
Table 13. Pin definitions (continued)

Pin number							Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
TSSOP14	UFQFPN20	TSSOP20	UFQFPN28	LQFP32	UFQFPN32[1]	WLCSP25					Alternate functions	Additional functions
-	-	-	26	28	28	-	PB5	I/O	FT	-	SPI1_MOSI, LPTIM1_IN1, I2C1_SMBA, TIM21_CH1	COMP2_INP
-	18	-	27	29	29	A3	PB6	I/O	FTf	-	USART2_TX, I2C1_SCL, LPTIM1_ETR, TIM2_CH3, LPUART1_TX	COMP2_INP
-	19	-	28	30	30	A4	PB7	I/O	FTf	-	USART2_RX, I2C1_SDA, LPTIM1_IN2, TIM2_CH4, LPUART1_RX	COMP2_INP, VREF_PVD_IN
1	20	1	1	31	31	A5	PB9-BOOT0	I	B	-	-	BOOT0 (Boot memory selection)
-	-	-	-	-	32	-	PB8	I/O	FTf	-	USART2_TX, EVENTOUT, I2C1_SCL, SPI1_NSS	-
-	-	-	-	32	-	-	VSS	S	-	(5)	-	-
-	-	-	-	1	1	-	VDD	S	-	(6)	-	-

1. V_{SS} pins are connected to the exposed pad (see *Figure 36: UFQFPN32, 5 x 5 mm, 32-pin package outline*).
2. Device reset input/internal reset output (active low).
3. Analog power supply.
4. On TSSOP14 package, V_{DDA} is internally connected to V_{DD}.
5. Digital and analog ground.
6. Digital power supply.

6.1.6 Power supply scheme

Figure 13. Power supply scheme



1. On TSSOP14 package, V_{DDA} is internally connected to V_{DD}.
2. V_{SSA} is internally connected to V_{SS} on all packages.

6.1.7 Current consumption measurement

Figure 14. Current consumption measurement scheme

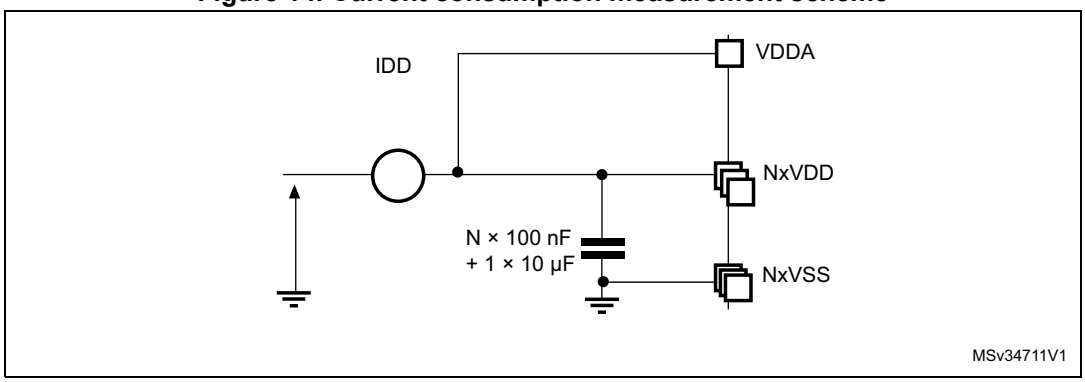


Table 19. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BOR3}	Brown-out reset threshold 3	Falling edge	2.45	2.55	2.6	V
		Rising edge	2.54	2.66	2.7	
V_{BOR4}	Brown-out reset threshold 4	Falling edge	2.68	2.8	2.85	
		Rising edge	2.78	2.9	2.95	
V_{PVD0}	Programmable voltage detector threshold 0	Falling edge	1.8	1.85	1.88	
		Rising edge	1.88	1.94	1.99	
V_{PVD1}	PVD threshold 1	Falling edge	1.98	2.04	2.09	
		Rising edge	2.08	2.14	2.18	
V_{PVD2}	PVD threshold 2	Falling edge	2.20	2.24	2.28	
		Rising edge	2.28	2.34	2.38	
V_{PVD3}	PVD threshold 3	Falling edge	2.39	2.44	2.48	
		Rising edge	2.47	2.54	2.58	
V_{PVD4}	PVD threshold 4	Falling edge	2.57	2.64	2.69	
		Rising edge	2.68	2.74	2.79	
V_{PVD5}	PVD threshold 5	Falling edge	2.77	2.83	2.88	
		Rising edge	2.87	2.94	2.99	
V_{PVD6}	PVD threshold 6	Falling edge	2.97	3.05	3.09	
		Rising edge	3.08	3.15	3.20	
V_{hyst}	Hysteresis voltage	BOR0 threshold	-	40	-	mV
		All BOR and PVD thresholds excepting BOR0	-	100	-	

1. Guaranteed by characterization results, not tested in production.
2. Valid for device version without BOR at power up. Please see option "D" in Ordering information scheme for more details.

4. Guaranteed by design, not tested in production.
5. Shortest sampling time can be determined in the application by multiple iterations.
6. To guarantee less than 1% VREF_OUT deviation.

6.3.4 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code. The current consumption is measured as described in *Figure 14: Current consumption measurement scheme*.

All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to Dhrystone 2.1 code if not specified otherwise.

The current consumption values are derived from the tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 18: General operating conditions* unless otherwise specified.

The MCU is placed under the following conditions:

- All I/O pins are configured in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time and prefetch is adjusted depending on f_{HCLK} frequency and voltage range to provide the best CPU performance unless otherwise specified.
- When the peripherals are enabled $f_{APB1} = f_{APB2} = f_{APB}$
- When PLL is ON, the PLL inputs are equal to HSI = 16 MHz (if internal clock is used) or HSE = 16 MHz (if HSE bypass mode is used)
- The HSE user clock is applied to CK_IN. It follows the characteristic specified in *Table 35: High-speed external user clock characteristics*
- For maximum current consumption $V_{DD} = V_{DDA} = 3.6$ V is applied to all supply pins
- For typical current consumption $V_{DD} = V_{DDA} = 3.0$ V is applied to all supply pins if not specified otherwise

Table 27. Current consumption in Low-power Run mode

Symbol	Parameter	Conditions			Typ	Max(1)	Unit
I_{DD} (LP Run)	Supply current in Low-power run mode	All peripherals OFF, code executed from RAM, Flash switched OFF, V_{DD} from 1.65 V to 3.6 V	MSI clock, 65 kHz f_{HCLK} = 32 kHz	T_A = -40 °C to 25 °C	5.7	8.1	µA
				T_A = 85 °C	6.5	9	
				T_A = 105 °C	8	13	
				T_A = 125 °C	11.5	22	
			MSI clock, 65 kHz f_{HCLK} = 65 kHz	T_A =-40 °C to 25 °C	8.7	11	
				T_A = 85 °C	9.5	12	
				T_A = 105 °C	11	15	
				T_A = 125 °C	15	24	
			MSI clock, 131 kHz f_{HCLK} = 131 kHz	T_A = -40 °C to 25 °C	17	19	
				T_A = 55 °C	17	19.5	
				T_A = 85 °C	17.5	20	
				T_A = 105 °C	19	22	
				T_A = 125 °C	22.5	31	
		All peripherals OFF, code executed from Flash, V_{DD} from 1.65 V to 3.6 V	MSI clock, 65 kHz f_{HCLK} = 32 kHz	T_A = -40 °C to 25 °C	18	22	
				T_A = 85 °C	20	24	
				T_A = 105 °C	22	27	
				T_A = 125 °C	26.5	37	
			MSI clock, 65 kHz f_{HCLK} = 65 kHz	T_A = -40 °C to 25 °C	22	25	
				T_A = 85 °C	24	27	
				T_A = 105 °C	26	30	
				T_A = 125 °C	30.5	39	
			MSI clock, 131 kHz f_{HCLK} = 131 kHz	T_A = -40 °C to 25 °C	32	34	
				T_A = 55 °C	32.5	35	
				T_A = 85 °C	34	37	
				T_A = 105 °C	36	39	
				T_A = 125 °C	40	47	

1. Guaranteed by characterization results at 125 °C, not tested in production, unless otherwise specified.

Figure 17. I_{DD} vs V_{DD}, at T_A= -40/25/55/ 85/105/125 °C, Low-power run mode, code running from RAM, Range 3, MSI (Range 0) at 64 KHz, 0 WS

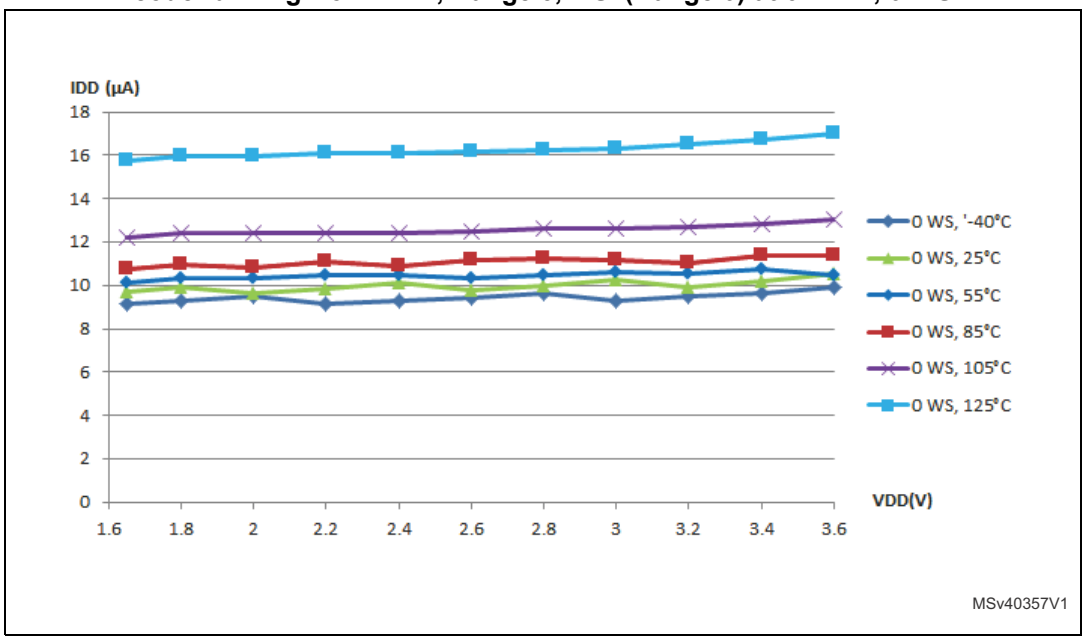


Table 28. Current consumption in Low-power Sleep mode

Symbol	Parameter	Conditions			Typ	Max(1)	Unit
I_{DD} (LP Sleep)	Supply current in Low-power sleep mode	All peripherals OFF, V_{DD} from 1.65 V to 3.6 V	MSI clock, 65 kHz f_{HCLK} = 32 kHz Flash OFF	T_A = -40 °C to 25 °C	2.5(2)	-	µA
			MSI clock, 65 kHz f_{HCLK} = 32 kHz Flash ON	T_A = -40 °C to 25 °C	13	19	
				T_A = 85 °C	15.5	20	
				T_A = 105 °C	17.5	22	
				T_A = 125 °C	21	29	
			MSI clock, 65 kHz f_{HCLK} = 65 kHz, Flash ON	T_A = -40 °C to 25 °C	13.5	19	
				T_A = 85 °C	16	20	
				T_A = 105 °C	18	22	
				T_A = 125 °C	21.5	29	
			MSI clock, 131 kHz f_{HCLK} = 131 kHz, Flash ON	T_A = -40 °C to 25 °C	15.5	21	
				T_A = 55 °C	17	22	
				T_A = 85 °C	18	23	
				T_A = 105 °C	19.5	24	
				T_A = 125 °C	23.5	31	

1. Guaranteed by characterization results at 125 °C, not tested in production, unless otherwise specified.
2. As the CPU is in Sleep mode, the difference between the current consumption with Flash memory ON and OFF (nearly 12 µA) is the same whatever the clock frequency.

6.3.17 Comparators

Table 59. Comparator 1 characteristics

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
V_{DDA}	Analog supply voltage	-	1.65		3.6	V
R_{400K}	R_{400K} value	-	-	400	-	kΩ
R_{10K}	R_{10K} value	-	-	10	-	
V_{IN}	Comparator 1 input voltage range	-	0.6	-	V_{DDA}	V
t_{START}	Comparator startup time	-	-	7	10	µs
td	Propagation delay(2)	-	-	3	10	
V_{offset}	Comparator offset(3)	-	-	±3	±10	mV
$d_{Voffset}/dt$	Comparator offset variation in worst voltage stress conditions(3)	V_{DDA} = 3.6 V V_{IN+} = 0 V V_{IN-} = V_{REFINT} T_A = 25 °C	0	1.5	10	mV/1000 h
I_{COMP1}	Current consumption(4)	-	-	160	260	nA

1. Guaranteed by characterization, not tested in production.
2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.
3. In TSSOP14 package, where V_{DDA} pin is shared with V_{DD} pin, I/O toggling should be minimized to reach the values given in the above table. I/O toggling with loaded I/O pins can generate ripple on V_{DD}/V_{DDA} and degrade the comparator performance.
4. Comparator consumption only. Internal reference voltage not included.

Table 60. Comparator 2 characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
V_{DDA}	Analog supply voltage	-	1.65	-	3.6	V
V_{IN}	Comparator 2 input voltage range	-	0	-	V_{DDA}	V
t_{START}	Comparator startup time	Fast mode	-	15	20	µs
		Slow mode	-	20	25	
$t_{d\ slow}$	Propagation delay(2) in slow mode	1.65 V ≤ V_{DDA} ≤ 2.7 V	-	1.8	3.5	
		2.7 V ≤ V_{DDA} ≤ 3.6 V	-	2.5	6	
$t_{d\ fast}$	Propagation delay(2) in fast mode	1.65 V ≤ V_{DDA} ≤ 2.7 V	-	0.8	2	
		2.7 V ≤ V_{DDA} ≤ 3.6 V	-	1.2	4	
V_{offset}	Comparator offset error(3)		-	±4	±20	mV
dThreshold/dt	Threshold voltage temperature coefficient	V_{DDA} = 3.3V T_A = 0 to 50 °C V- = V_{REFINT}, 3/4 V_{REFINT}, 1/2 V_{REFINT}, 1/4 V_{REFINT}.	-	15	30	ppm /°C

Table 66. SPI characteristics in voltage Range 2 (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	-	8	MHz
		Slave mode Transmitter $1.65<V_{DD}<3.6V$			8	
		Slave mode Transmitter $2.7<V_{DD}<3.6V$			8(2)	
$Duty_{(SCK)}$	Duty cycle of SPI clock frequency	Slave mode	30	50	70	%
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI presc = 2	4Tpclk	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI presc = 2	2Tpclk	-	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode	Tpclk-2	Tpclk	Tpclk+2	
$t_{su(MI)}$	Data input setup time	Master mode	3	-	-	
$t_{su(SI)}$		Slave mode	3	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	6	-	-	
$t_{h(SI)}$		Slave mode	2	-	-	
$t_{a(SO}$	Data output access time	Slave mode	18	-	52	
$t_{dis(SO)}$	Data output disable time	Slave mode	12	-	42	
$t_{v(SO)}$	Data output valid time	Slave mode	-	16	33	
		Master mode	-	4	6	
$t_{v(MO)}$	Data output hold time	Slave mode	11	-	-	
$t_{h(SO)}$		Master mode	3	-	-	

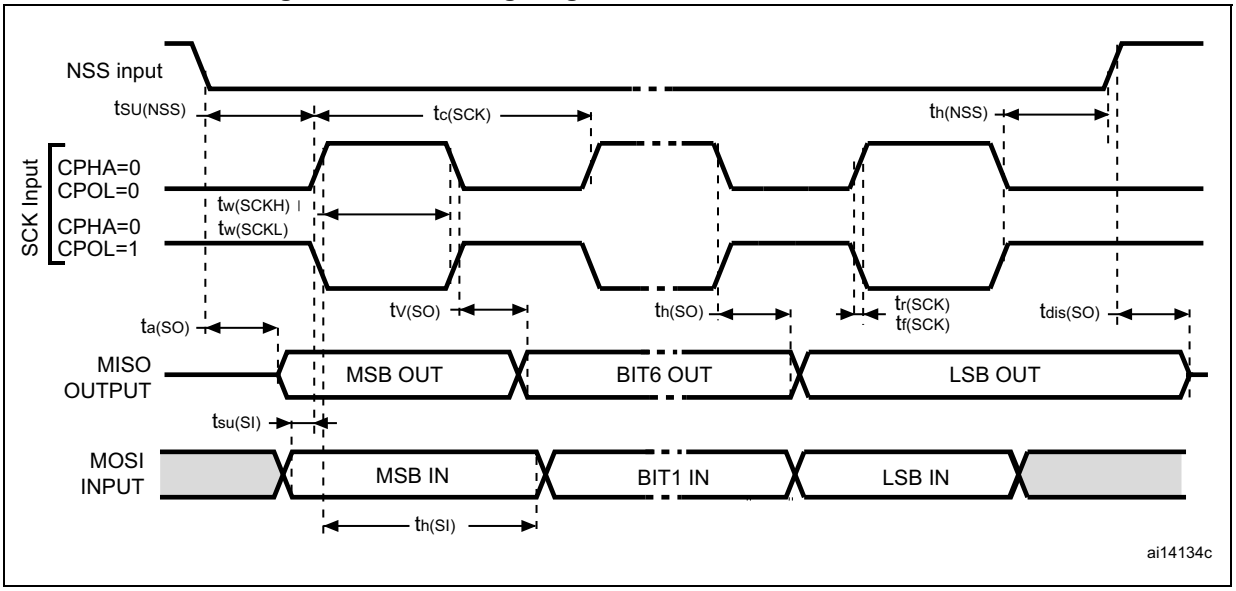
1. Guaranteed by characterization results, not tested in production.
2. The maximum SPI clock frequency in slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)}$ = 0 while $Duty_{(SCK)}$ = 50%.

Table 67. SPI characteristics in voltage Range 3 (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	-	2	MHz
		Slave mode			2(2)	
$Duty_{(SCK)}$	Duty cycle of SPI clock frequency	Slave mode	30	50	70	%
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI presc = 2	4Tpclk	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI presc = 2	2Tpclk	-	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode	Tpclk-2	Tpclk	Tpclk+2	
$t_{su(MI)}$	Data input setup time	Master mode	3	-	-	
$t_{su(SI)}$		Slave mode	3	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	16	-	-	
$t_{h(SI)}$		Slave mode	14	-	-	
$t_{a(SO}$	Data output access time	Slave mode	30	-	70	
$t_{dis(SO)}$	Data output disable time	Slave mode	40	-	80	
$t_{v(SO)}$	Data output valid time	Slave mode	-	26.5	47	
		Master mode	-	4	6	
$t_{v(MO)}$	Data output hold time	Slave mode	20	-	-	
$t_{h(SO)}$		Master mode	3	-	-	

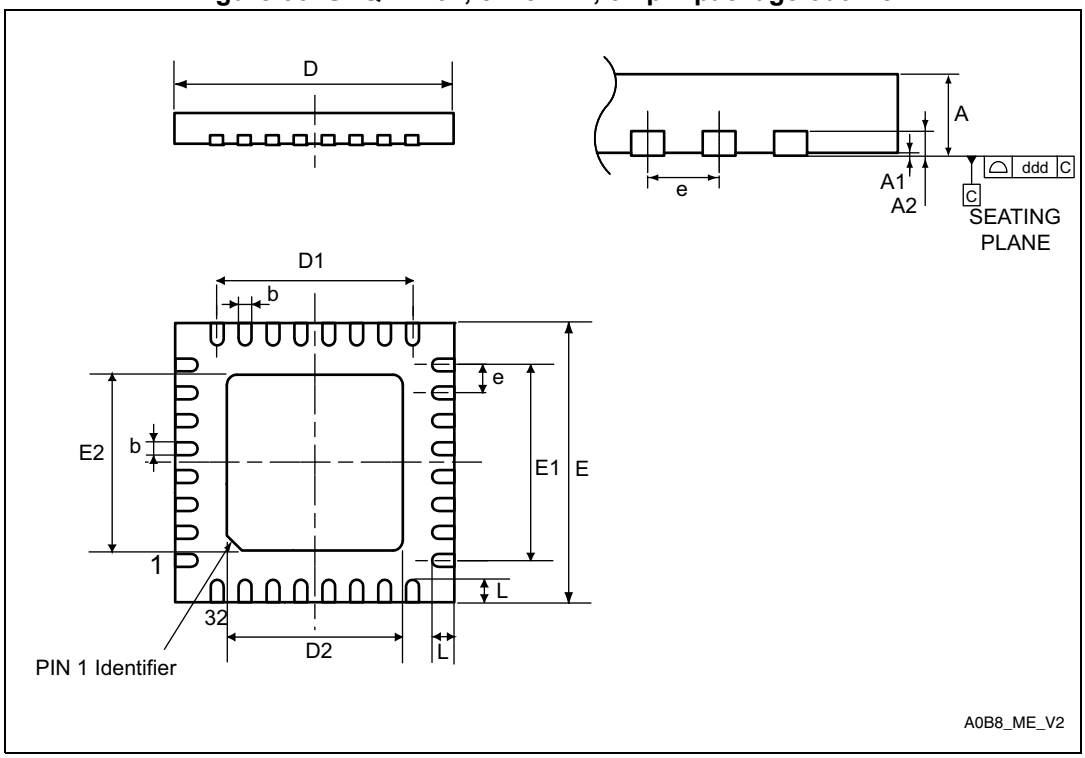
1. Guaranteed by characterization results, not tested in production.
2. The maximum SPI clock frequency in slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)}$ = 0 while $Duty_{(SCK)}$ = 50%.

Figure 30. SPI timing diagram - slave mode and CPHA = 0



7.2 UFQFPN32 package information

Figure 36. UFQFPN32, 5 x 5 mm, 32-pin package outline



1. Drawing is not to scale.

Table 69. UFQFPN32, 5 x 5 mm, 32-pin package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
A3	-	0.200	-	-	0.0079	-
b	0.180	0.250	0.300	0.0071	0.0098	0.0118
D	4.900	5.000	5.100	0.1929	0.1969	0.2008
D2	3.200	3.450	3.700	0.1260	0.1358	0.1457
E	4.900	5.000	5.100	0.1929	0.1969	0.2008
E2	3.200	3.450	3.700	0.1260	0.1358	0.1457
e	-	0.500	-	-	0.0197	-
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
ddd	-	-	0.080	-	-	0.0031

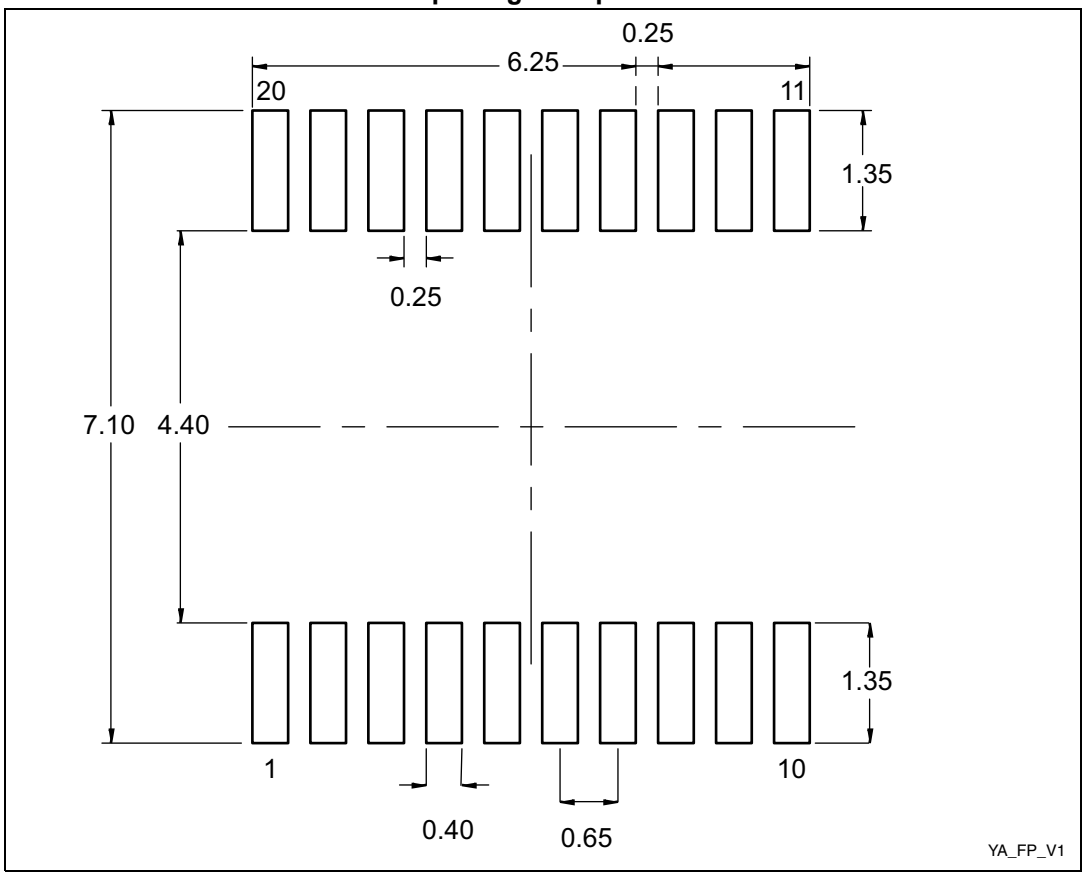
1. Values in inches are converted from mm and rounded to 4 decimal digits.

Table 74. TSSOP20 – 20-lead thin shrink small outline, 6.5 x 4.4 mm, 0.65 mm pitch, package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
k	0°	-	8°	0°	-	8°
aaa	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to four decimal digits.

Figure 49. TSSOP20 – 20-lead thin shrink small outline, 6.5 x 4.4 mm, 0.65 mm pitch, package footprint



1. Dimensions are expressed in millimeters.

9 Revision history

Table 78. Document revision history

Date	Revision	Changes
07-Dec-2015	1	Initial release.
11-Feb-2016	2	*Features*: modified current consumption in run mode, Cortex®-M0+ core frequency range and total number of timers. Updated ADC conversion consumption on cover page. Updated UFQFPN28 pinout: *Figure 6: STM32L011x3/4 UFQFPN28 pinout* and *Table 13: Pin definitions*. Updated *Table 55: RAIN max for fADC = 16 MHz*. Modified TS_CAL2 description in *Table 57: Temperature sensor calibration values*.
18-Mar-2016	3	Changed minimum comparator supply voltage to 1.65 V on cover page. Added baudrate allowing to wake up the MCU from Stop mode in *Section 3.15.3: Low-power universal asynchronous receiver transmitter (LPUART)*. Added number of fast and standard channels in *Section 3.10: Analog-to-digital converter (ADC)*. Updated *Table 16: Current characteristics* to add the total output current for STM32L011GxUx. Changed V_{DDA} minimum value to 1.65 V.in *Table 18: General operating conditions*. Updated *Table 26: Current consumption in Sleep mode*, *Table 27: Current consumption in Low-power Run mode*, *Table 28: Current consumption in Low-power Sleep mode* and *Table 30: Typical and maximum current consumptions in Standby mode*. *Section 6.3.15: 12-bit ADC characteristics*: – *Table 54: ADC characteristics*: Distinction made between V_{DDA} for fast and standard channels; added note *1.* Updated condition for f_{TRIG} measurement. Added note *4.* related to R_{ADC} and removed measurement condition. Updated t_S and t_{CONV}. – Updated equation 1 description. – Updated *Table 55: RAIN max for fADC = 16 MHz* for f_{ADC} = 16 MHz and distinction made between fast and standard channels. – Updated measurement condition in *Table 56: ADC accuracy*. Added *Table 64: USART/LPUART characteristics*.