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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I ² C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	28
Program Memory Size	16KB (16K × 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-UFQFPN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l011k4u3tr

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

2.2 Ultra-low-power device continuum

The ultra-low-power family offers a large choice of core and features, from 8-bit proprietary core up to ARM[®] Cortex[®]-M4, including ARM[®] Cortex[®]-M3 and ARM[®] Cortex[®]-M0+. The STM32Lx series are the best choice to answer your needs in terms of ultra-low-power features. The STM32 Ultra-low-power series are the best solution for applications such as gas/water meter, keyboard/mouse or fitness and healthcare application. Several built-in features like LCD drivers, dual-bank memory, low-power Run mode, operational amplifiers, 128-bit AES, DAC, crystal-less USB and many other definitely help you building a highly cost optimized application by reducing BOM cost. STMicroelectronics, as a reliable and long-term manufacturer, ensures as much as possible pin-to-pin compatibility between all STM8Lx and STM32Lx on one hand, and between all STM32Lx and STM32Fx on the other hand. Thanks to this unprecedented scalability, your legacy application can be upgraded to respond to the latest market feature and efficiency requirements.



			Low- Low-		Low-	Low-		Stop		Standby	
IPs	Run/Active	Sleep	power run	power sleep		Wakeup capability		Wakeup capability			
Programmable Voltage Detector (PVD)	0	0	О	Ο	0	0	-	-			
Power-on/down reset (POR/PDR)	Y	Y	Y	Y	Y	Y	Y	Y			
High Speed Internal (HSI)	0	0	-	-	(3)	-	-	-			
High Speed External (HSE)	0	0	0	0	-	-	-	-			
Low Speed Internal (LSI)	0	0	0	0	0	-	0	-			
Low Speed External (LSE)	0	0	0	0	0	-	0	-			
Multi-Speed Internal (MSI)	0	0	Y	Y	-	-	-	-			
Inter-Connect Controller	Y	Y	Y	Y	Y	-	-	-			
RTC	0	0	0	0	0	0	0	-			
RTC Tamper	0	0	0	0	0	0	0	0			
Auto WakeUp (AWU)	0	О	0	0	0	-	0	0			
USART	0	0	0	0	O ⁽⁴⁾	0	-	-			
LPUART	0	0	0	0	O ⁽⁴⁾	0	-	-			
SPI	0	0	0	0	-		-	-			
I2C	0	0	0	0	O ⁽⁵⁾	0	-	-			
ADC	0	0	-	-	-	-	-	-			
Temperature sensor	0	О	0	0	0	-	-	-			
Comparators	0	0	0	0	0	0	-	-			
16-bit timers	0	0	0	0	-	-	-	-			
LPTIM	0	0	0	0	0	0	-	-			
IWDG	0	0	0	0	0	0	0	0			
WWDG	0	0	0	0	-	-	-	-			
SysTick Timer	0	0	0	0	-	-	-	-			
GPIOs	0	0	0	0	0	0	-	2 pins			

Table 5. Functionalities depending on the working mode (from Run/active down to standby) (continued)⁽¹⁾⁽²⁾



Interconnect source	Interconnect destination	Interconnect action	Run	Sleep	Low- power run	Low- power sleep	Stop
TIMx	TIMx	Timer triggered by other timer	Y	Y	Y	Y	-
PTC	TIM21	Timer triggered by Auto wake-up	Y	Y	Y	Y	-
RIC	LPTIM1	Timer triggered by RTC event	Y	Y	Y	Y	Y
All clock source	TIMx	Clock source used as input channel for RC measurement and trimming	Y	Y	Y	Y	-
	TIMx	Timer input channel and trigger	Y	Y	Y	Y	-
GPIO	LPTIM1	Timer input channel and trigger	Y	Y	Y	Y	Y
	ADC	Conversion trigger	Y	Y	Y	Y	-

Table 6. STM32L011x3/4 peripherals interconnect matrix (continued)

3.3 ARM[®] Cortex[®]-M0+ core

The Cortex-M0+ processor is an entry-level 32-bit ARM Cortex processor designed for a broad range of embedded applications. It offers significant benefits to developers, including:

- a simple architecture that is easy to learn and program
- ultra-low power, energy-efficient operation
- excellent code density
- deterministic, high-performance interrupt handling
- upward compatibility with Cortex-M processor family
- platform security robustness.

The Cortex-M0+ processor is built on a highly area and power optimized 32-bit processor core, with a 2-stage pipeline von Neumann architecture. The processor delivers exceptional energy efficiency through a small but powerful instruction set and extensively optimized design, providing high-end processing hardware including a single-cycle multiplier.

The Cortex-M0+ processor provides the exceptional performance expected of a modern 32bit architecture, with a higher code density than other 8-bit and 16-bit microcontrollers.

Owing to its embedded ARM core, the STM32L011x3/4 are compatible with all ARM tools and software.



Five BOR thresholds are available through option bytes, starting from 1.8 V to 3 V. To reduce the power consumption in Stop mode, it is possible to automatically switch off the internal reference voltage (V_{REFINT}) in Stop mode. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR} , without the need for any external reset circuit.

Note: The start-up time at power-on is typically 3.3 ms when BOR is active at power-up, the startup time at power-on can be decreased down to 1 ms typically for devices with BOR inactive at power-up.

The devices feature an embedded programmable voltage detector (PVD) that monitors the $V_{DD/VDDA}$ power supply and compares it to the V_{PVD} threshold. This PVD offers 7 different levels between 1.85 V and 3.05 V, chosen by software, with a step around 200 mV. An interrupt can be generated when $V_{DD/VDDA}$ drops below the V_{PVD} threshold and/or when $V_{DD/VDDA}$ is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.4.3 Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR) and power down.

- MR is used in Run mode (nominal regulation)
- LPR is used in the Low-power run, Low-power sleep and Stop modes
- Power down is used in Standby mode. The regulator output is high impedance, the kernel circuitry is powered down, inducing zero consumption but the contents of the registers and RAM are lost except for the standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE crystal 32 KHz oscillator, RCC_CSR).

3.4.4 Boot modes

At startup, BOOT0 pin and nBOOT0, nBOOT1 and nBOOT_SEL option bits are used to select one of three boot options:

- Boot from Flash memory
- Boot from System memory
- Boot from embedded RAM

The boot loader is located in System memory. It is used to reprogram the Flash memory by using SPI1 (PA4, PA7, PA13 and PA14 on TSSOP14 package or PA4, PA5, PA6 and PA7 on other packages) or USART2 (PA2, PA3 and PA9, PA10). See STM32[™] microcontroller system memory boot mode AN2606 for details.



I2C features ⁽¹⁾	I2C1
7-bit addressing mode	Х
10-bit addressing mode	Х
Standard mode (up to 100 kbit/s)	Х
Fast mode (up to 400 kbit/s)	Х
Fast Mode Plus with 20 mA output drive I/Os (up to 1 Mbit/s)	X ⁽²⁾
Independent clock	Х
SMBus	Х
Wakeup from STOP	Х

Tabla O	STM221 044-2/4	120	implementation
Table 3.	311WJZLU11XJ/4	10	implementation

1. X = supported.

2. See Table 13: Pin definitions on page 37 for the list of I/Os that feature Fast Mode Plus capability

3.15.2 Universal synchronous/asynchronous receiver transmitter (USART)

The USART interface (USART2) is able to communicate at speeds of up to 4 Mbit/s.

It provides hardware management of the CTS, RTS and RS485 driver enable (DE) signals, multiprocessor communication mode and single-wire half-duplex communication mode. USART2 also supports Smartcard communication (ISO 7816, T=0 protocol) and IrDA SIR ENDEC.

USART2 interface can be served by the DMA controller.

Table 10 for the supported modes and features of USART interface.

USART modes/features ⁽¹⁾	USART2
Hardware flow control for modem	Х
Continuous communication using DMA	Х
Multiprocessor communication	Х
Synchronous mode	-
Smartcard mode	Х
Single-wire half-duplex communication	Х
IrDA SIR ENDEC block	Х
LIN mode	-
Dual clock domain and wakeup from Stop mode	-
Receiver timeout interrupt	-
Modbus communication	-
Auto baud rate detection (4 modes)	-
Driver Enable	Х

Table 10. USART implementation

1. X = supported.



3.17 Serial wire debug port (SW-DP)

An ARM SW-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.



6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A = 25$ °C and $T_A = T_Amax$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean $\pm 3\sigma$).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.6 V (for the 1.65 V \leq V_{DD} \leq 3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean $\pm 2\sigma$).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 11*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 12*.





Symbol	Parameter	Conditions	Min	Мах	Unit
		Maximum power dissipation (range 6)	-40	85	
TA	Temperature range	Maximum power dissipation (range 7)	-40	105	
		Maximum power dissipation (range 3)	-40	125	°C
	Junction temperature range (range 6)	-40 °C \leq T _A \leq 85 °	-40	105	
TJ	Junction temperature range (range 7)	-40 °C \leq T _A \leq 105 °C	-40	125	
	Junction temperature range (range 3)	-40 °C \leq T _A \leq 125 °C	-40	130	

 Table 18. General operating conditions (continued)

1. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and normal operation.

2. To sustain a voltage higher than V_{DD} +0.3V, the internal pull-up/pull-down resistors must be disabled.

If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_J max (see Table 17: Thermal characteristics on page 47).

6.3.2 Embedded reset and power control block characteristics

The parameters given in the following table are derived from the tests performed under the ambient temperature condition summarized in *Table 18*.

Symbol	Parameter	Conditions	Min	Тур	Мах	Unit	
(1)	V rise time rate	BOR detector enabled	0	-	8		
		BOR detector disabled	0	-	1000		
VDD` '	V fall time rate	BOR detector enabled	20	-	~	μ5/ν	
		BOR detector disabled	0	-	1000		
T _{RSTTEMPO} ⁽¹⁾	Poset temporization	V _{DD} rising, BOR enabled	-	2	3.3	ms	
	Reset temporization	V _{DD} rising, BOR disabled ⁽²⁾	0.4	0.7	1.6		
	Power on/power down reset	Falling edge	1	1.5	1.65		
♥ POR/PDR	threshold	Rising edge	1.3	1.5	1.65		
N/ s	Brown out reset threshold 0	Falling edge	1.67	1.7	1.74		
VBOR0		Rising edge	1.69	1.76	1.8	V	
V	Prown out report throshold 1	Falling edge	1.87	1.93	1.97	v	
VBOR1		Rising edge	1.96	2.03	2.07		
V _{BOR2}	Prown out report throshold 2	Falling edge	2.22	2.30	2.35		
		Rising edge	2.31	2.41	2.44		

Table 19. Embedded reset and power control block characteristics



		Typical consumption, V_{DD} = 3.0 V, T _A = 25 °C					
Per	ipheral	Range 1, V _{CORE} =1.8 V VOS[1:0] = 01	Range 2, V _{CORE} =1.5 V VOS[1:0] = 10	Range 3, V _{CORE} =1.2 V VOS[1:0] = 11	Low-power sleep and run	Unit	
	WWDG	2.5	2	1.6	2		
	LPUART1	8.3	7.2	5.4	7.2		
APB1	I2C1	11	8.2	6.8	8.9	µA/MHz	
	LPTIM1	14	11	8.7	11	(f _{HCLK})	
	TIM2	10.5	8.5	6.4	8.5		
	USART2	8.5	6.8	5.4	7.1		
	ADC1 ⁽²⁾	5.0	3.9	3.3	4		
	SPI1	4.5	3.5	2.9	3.6	μΑ/ΜΗz (f _{HCLK})	
APB2	TIM21	6.8	6.1	4.5	5.6		
, BE	DBGMCU	1.7	1.7	1.1	1.4		
	SYSCFG/ COMP	2.5	2.4	1.6	2.3		
Cortex-	GPIOA	7.6	6.3	4.9	6.5		
M0+ core	GPIOB	5.1	4.1	3.2	4	µA/MHz	
I/O port	GPIOC	1.1	0.7	0.6	0.8	VIICLK/	
	CRC	1.5	1.1	1	1.2		
	FLASH ⁽³⁾	10	8.5	7	8.5		
АНВ	DMA1	5.3	4.2	3.5	4.8	µA/MHz	
All enabled	ł	96	80	62	88	VHULK/	
PWR		2.1	1.9	1.4	1.8	µA/MHz (f _{HCLK})	

 Table 32. Peripheral current consumption in run or Sleep mode⁽¹⁾

 Data based on differential I_{DD} measurement between all peripherals OFF an one peripheral with clock enabled, in the following conditions: f_{HCLK} = 32 MHz (range 1), f_{HCLK} = 16 MHz (range 2), f_{HCLK} = 4 MHz (range 3), f_{HCLK} = 64kHz (Low-power run/sleep), f_{APB1} = f_{HCLK}, f_{APB2} = f_{HCLK}, default prescaler value for each peripheral. The CPU is in Sleep mode in both cases. No I/O pins toggling. Not tested in production.

2. HSI oscillator is OFF for this measure.

 These values correspond to the Flash memory dynamic current consumption. The Flash memory static consumption (Flash memory ON) equals 12 μA and does not depend on the frequency. The Flash memory consumption is already taken into account in all the supply current consumption tables (Flash memory ON cases).



Flash memory and data EEPROM

Symbol	Parameter	Conditions	Min	Тур	Max ⁽¹⁾	Unit
V_{DD}	Operating voltage Read / Write / Erase	-	1.65	-	3.6	V
+	Programming time for	Erasing	-	3.28	3.94	me
^{lprog} word or half-page		Programming	-	3.28	3.94	1115
	Average current during the whole programming / erase operation		-	500	700	μA
I _{DD}	Maximum current (peak) during the whole programming / erase operation	T _A = 25 °C, V _{DD} = 3.6 V	-	1.5	2.5	mA

Table 43. Flash memory and data EEPROM characteristics

1. Guaranteed by design, not tested in production.

Quarteral	Demonster	O a maliti a ma	Value	11
Symbol	Parameter	Conditions	Min ⁽¹⁾	Unit
	Cycling (erase / write) Program memory	$T_{\rm c} = -40^{\circ}$ C to 105 °C	10	
N	Cycling (erase / write) EEPROM data memory	$T_{\rm A} = -40$ C to 103 C	100	kovoles
NCYC'	Cycling (erase / write) Program memory	$T_{1} = -40^{\circ}$ C to 125 °C	0.2	kcycles
	Cycling (erase / write) EEPROM data memory	$T_{A} = -40 \ \text{C} \ \text{to} \ 123 \ \text{C}$	2	
	Data retention (program memory) after 10 kcycles at T _A = 85 °C	T = +85 °C	30	
	Data retention (EEPROM data memory) after 100 kcycles at $T_A = 85 \text{ °C}$	TRET - 105 C	30	
+ (2)	Data retention (program memory) after 10 kcycles at T _A = 105 °C	T - 1405 °C	- 10	years
^t RET ⁽²⁾	Data retention (EEPROM data memory) after 100 kcycles at $T_A = 105$ °C	TRET - TIUS C		
	Data retention (program memory) after 200 cycles at T _A = 125 °C	T - +125 °C		
	Data retention (EEPROM data memory) after 2 kcycles at T_A = 125 °C	1 RET - 123 C		

Table 44. Flash memor	y and data EEPROM endurance and retention

1. Guaranteed by characterization results, not tested in production.

2. Characterization is done according to JEDEC JESD22-A117.



Symbol	Parameter	Conditions	Class				
LU	Static latch-up class	$T_A = +125 \text{ °C conforming to JESD78A}$	II level A				

Table 48. Electrical sensitivities

6.3.12 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of -5μ A/+0 μ A range), or other functional failure (for example reset occurrence oscillator frequency deviation).

The test results are given in the Table 49.

		Functional s	usceptibility	
Symbol Description		Negative injection	Positive injection	Unit
	Injected current on BOOT0	-0	NA	
I _{INJ}	Injected current on all FT pins	-5 ⁽¹⁾	NA	mA
	Injected current on any other pin	-5 ⁽¹⁾	+5	

Table 49. I/O current injection susceptibility

1. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.





Figure 27. Recommended NRST pin protection

1. The reset network protects the device against parasitic resets.

 The user must ensure that the level on the NRST pin can go below the V_{IL(NRST)} max level specified in Table 53. Otherwise the reset will not be taken into account by the device.

6.3.15 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 54* are values derived from tests performed under ambient temperature, f_{PCLK} frequency and V_{DDA} supply voltage conditions summarized in *Table 18: General operating conditions*.

Note: It is recommended to perform a calibration after each power-up.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V	Analog supply voltage for	Fast channel	1.65	-	3.6	V
V DDA	ADC ON	Standard channels	1.75 ⁽¹⁾	-	3.6	v
	Current consumption of the	1.14 Msps	-	200	-	
	ADC on V _{DDA}	10 ksps	-	40	-	
'DDA (ADC)	Current consumption of the	1.14 Msps	-	70	-	μΑ
	ADC on V _{DD} ⁽²⁾	10 ksps	-	1	-	
		Voltage scaling Range 1	0.14	-	16	
f _{ADC} ADC clock frequency	Voltage scaling Range 2	0.14	-	8	MHz	
		Voltage scaling Range 3	0.14	-	4	
f _S ⁽³⁾	Sampling rate	-	0.05	-	1.14	MHz
f _{TRIG} ⁽³⁾	External trigger frequency	f _{ADC} = 16 MHz, 16-bit resolution	-	-	941	kHz
		-	-	-	17	1/f _{ADC}
V _{AIN}	Conversion voltage range	-	0	-	V _{DDA}	V
R _{AIN} ⁽³⁾	External input impedance	See <i>Equation 1</i> and <i>Table 55</i> for details	-	-	50	kΩ
R _{ADC} ⁽³⁾⁽⁴⁾	Sampling switch resistance	-	-	-	1	kΩ
C _{ADC} ⁽³⁾	Internal sample and hold capacitor	-	-	-	8	pF

Table 54. ADC characteristics



Electrical characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
ET	Total unadjusted error		-	3	5	
EO	Offset error		-	2	2.5	
EG	Gain error		-	2	2.5	LSB
EL	Integral linearity error		-	1.5	2.5	
ED	Differential linearity error		-	1	1.7	
	Effective number of bits	$1.65 V < V_{DDA} < 3.6 V_{range}$	9.5	10.5	-	
ENOB	Effective number of bits (16-bit mode oversampling with ratio =256) ⁽⁵⁾	1/2/3, TSSOP14 package	10.7	11.6	-	bits
SINAD	Signal-to-noise distortion		59	65	-	
	Signal-to-noise ratio		59	65	-	
SNR	Signal-to-noise ratio (16-bit mode oversampling with ratio =256) ⁽⁵⁾		66	73	-	dB
THD	Total harmonic distortion]	-	-75	-63	

Table 56. ADC $accuracy^{(1)(2)(3)(4)}$

1. ADC DC accuracy values are measured after internal calibration.

 ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for I_{INJ(PIN)} and ΣI_{INJ(PIN)} in Section 6.3.12 does not affect the ADC

Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in Section 6.3.12 does not affect the ADC accuracy.

- 3. Better performance may be achieved in restricted V_{DDA} , frequency and temperature ranges.
- 4. In TSSOP14 package, where V_{DDA} pin is shared with V_{DD} pin, I/O toggling should be minimized to reach the values given in the above table. I/O toggling with loaded I/O pins can generate ripple on V_{DD}/V_{DDA} and degrade the ADC accuracy.
- 5. This number is obtained by the test board without additional noise, resulting in non-optimized value for oversampling mode.

Figure 28. ADC accuracy characteristics



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Figure 29. Typical connection diagram using the ADC

- 1. Refer to Table 54: ADC characteristics for the values of RAIN, RADC and CADC.
- C_{parasitic} represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high C_{parasitic} value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

6.3.16 Temperature sensor characteristics

Table 57. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL2	TS ADC raw data acquired at temperature of 130 °C \pm 5 °C, V _{DDA} = 3 V \pm 10 mV	0x1FF8 007E - 0x1FF8 007F

	•				
Symbol	Parameter	Min	Тур	Мах	Unit
T _L ⁽¹⁾	V _{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope ⁽¹⁾	Average slope	1.48	1.61	1.75	mV/°C
V ₁₃₀	Voltage at 130°C ±5°C ⁽²⁾	640	670	700	mV
I _{DDA(TEMP)} ⁽³⁾	Current consumption	-	3.4	6	μA
t _{START} ⁽³⁾	Startup time	-	-	10	
T _{S_temp} ⁽⁴⁾⁽³⁾	ADC sampling time when reading the temperature	10	-	-	μs

Table 58. Temperature sensor characteristics

1. Guaranteed by characterization results, not tested in production.

2. Measured at V_{DD} = 3 V \pm 10 mV. V30 ADC conversion result is stored in the TS_CAL1 byte.

3. Guaranteed by design, not tested in production.

4. Shortest sampling time can be determined in the application by multiple iterations.



Symbol	Parameter	Conditions	Min	Тур	Max	Unit
		Master mode			8	
f _{SCK}	SPI clock frequency	Slave mode Transmitter 1.65 <v<sub>DD<3.6V</v<sub>	-	-	8	MHz
(SCK)		Slave mode Transmitter 2.7 <v<sub>DD<3.6V</v<sub>			8 ⁽²⁾	
Duty _(SCK)	Duty cycle of SPI clock frequency	Slave mode	30	50	70	%
t _{su(NSS)}	NSS setup time	Slave mode, SPI presc = 2	4Tpclk	-	-	
t _{h(NSS)}	NSS hold time	Slave mode, SPI presc = 2	2Tpclk	-	-	
t _{w(SCKH)} t _{w(SCKL)}	SCK high and low time	Master mode	Tpclk-2	Tpclk	Tpclk+2	
t _{su(MI)}	Data input actus tima	Master mode	3	-	-	
t _{su(SI)}	Data input setup time	Slave mode	3	-	-	
t _{h(MI)}	Data input hold time	Master mode	6	-	-	
t _{h(SI)}	Data input hold time	Slave mode	2	-	-	ns
t _{a(SO}	Data output access time	Slave mode	18	-	52	
t _{dis(SO)}	Data output disable time	Slave mode	12	-	42	
turee	Data output valid time	Slave mode	-	16	33	
•v(SO)		Master mode	-	4	6	
t _{v(MO)}	Data output hold time	Slave mode	11	-	-	1
t _{h(SO)}	Data output noid time	Master mode	3	-	-	1

-					_	~ (1)
lable 66.	SPI	characteristics	ın	voltage	Range	2 \	•,

1. Guaranteed by characterization results, not tested in production.

2. The maximum SPI clock frequency in slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)} = 0$ while Duty_(SCK) = 50%.



Symbol	Parameter	Conditions	Min	Тур	Max	Unit
f _{scк}		Master mode			2	
1/t _{c(SCK)}	SPI Clock liequency	Slave mode	-	-	2 ⁽²⁾	
Duty _(SCK)	Duty cycle of SPI clock frequency	Slave mode	30	50	70	%
t _{su(NSS)}	NSS setup time	Slave mode, SPI presc = 2	4Tpclk	-	-	
t _{h(NSS)}	NSS hold time	Slave mode, SPI presc = 2	2Tpclk	-	-	
t _{w(SCKH)} t _{w(SCKL)}	SCK high and low time	Master mode	Tpclk-2	Tpclk	Tpclk+2	
t _{su(MI)}	Data input actur timo	Master mode	3	-	-	
t _{su(SI)}	Data input setup time	Slave mode	3	-	-	
t _{h(MI)}	Data input hold time	Master mode	16	-	-	
t _{h(SI)}		Slave mode	14	-	-	ns
t _{a(SO}	Data output access time	Slave mode	30	-	70	
t _{dis(SO)}	Data output disable time	Slave mode	40	-	80	
t (ee)	Data output valid time	Slave mode	-	26.5	47	
v(SO)		Master mode	-	4	6	
t _{v(MO)}	Dete autout hald time	Slave mode	20	-	-	1
t _{h(SO)}		Master mode	3	-	-	1

Table 67	SPI cl	haractoristics	in	voltano	Rango	z (1)	
Table 07.	SFIC	laracteristics	ш	vonage	капуе	S` '	

1. Guaranteed by characterization results, not tested in production.

2. The maximum SPI clock frequency in slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)} = 0$ while Duty_(SCK) = 50%.



Figure 30. SPI timing diagram - slave mode and CPHA = 0

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Figure 37. UFQFPN32 recommended footprint

1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking versus pin 1 position identifier location.



Figure 38. Example of UFQFPN32 marking (package top view)

 Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.



Table 70. WLCSP25 - 25-ball, 2.133 x 2.070 mm, 0.4 mm pitch wafer level chip scale package mechanical data (continued)

G	-	0.235	-	-	0.0093	-
aaa	-	-	0.100	-	-	0.0039
bbb	-	-	0.100	-	-	0.0039
CCC	-	-	0.100	-	-	0.0039
ddd	-	-	0.050	-	-	0.0020
eee	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

2. Back side coating.

3. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

Figure 40. WLCSP25 - 25-ball, 2.133 x 2.070 mm, 0.4 mm pitch wafer level chip scale package recommended footprint



WLCSP25_A05M_FP_V1

Table 71. WLCSP25 recommended PCB design rules (0.4 mm pitch)

Dimension	Recommended values
Pitch	0.4 mm
Dpad	0.225 mm
Dsm	0.290 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.250 mm
Stencil thickness	0.100 mm





Figure 43. UFQFPN28 recommended footprint

1. Dimensions are expressed in millimeters.

UFQFPN28 device marking

The following figure gives an example of topside marking versus pin 1 position identifier location.



Figure 44. Example of UFQFPN28 marking (package top view)

 Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.



puokago moonamoa data						
Symbol	millimeters			inches ⁽¹⁾		
	Min	Тур	Мах	Min	Тур	Max
А	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
A3	-	0.152	-	-	0.060	-
D	-	3.000	-	-	0.1181	-
E	-	3.000	-	-	0.1181	-
L1	0.500	0.550	0.600	0.0197	0.0217	0.0236
L2	0.300	0.350	0.400	0.0118	0.0138	0.0157
L3	-	0.375	-	-	0.0148	-
L4	-	0.200	-	-	0.0079	-
L5	-	0.150	-	-	0.0059	-
b	0.180	0.250	0.300	0.0071	0.0098	0.0118
е	-	0.500	-	-	0.0197	-
ddd	-	-	0.050	-	-	0.0020

Table 73. UFQFPN20 - 20-lead, 3x3 mm, 0.5 mm pitch, ultra thin fine pitch quad flatpackage mechanical data

1. Values in inches are converted from mm and rounded to 4 decimal digits.





1. Dimensions are expressed in millimeters.

