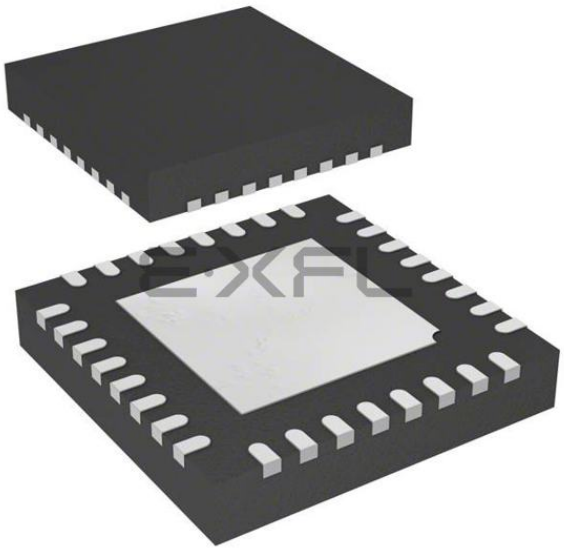

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0+ |
| Core Size | 32-Bit Single-Core |
| Speed | 32MHz |
| Connectivity | I²C, IrDA, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, POR, PWM, WDT |
| Number of I/O | 28 |
| Program Memory Size | 16KB (16K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 512 x 8 |
| RAM Size | 2K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.65V ~ 3.6V |
| Data Converters | A/D 10x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 32-UFQFN Exposed Pad |
| Supplier Device Package | 32-UFQFPN (5x5) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l011k4u6 |

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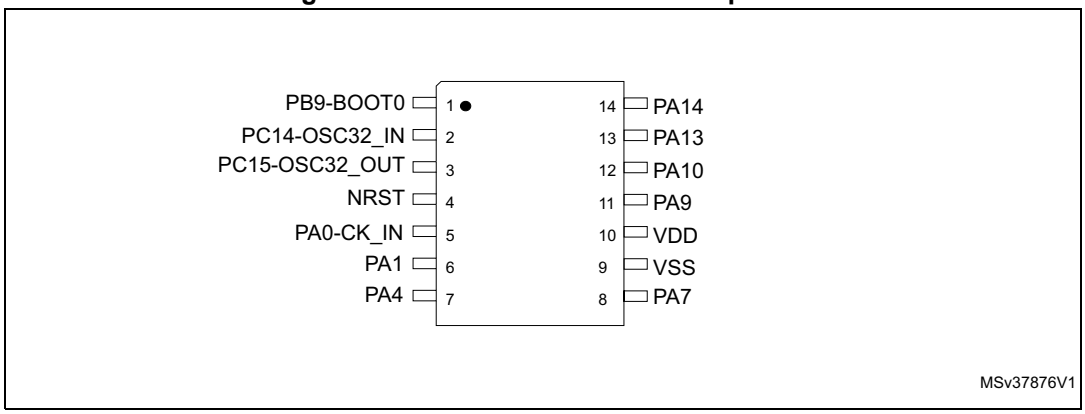
## 2.2 Ultra-low-power device continuum

The ultra-low-power family offers a large choice of core and features, from 8-bit proprietary core up to ARM® Cortex®-M4, including ARM® Cortex®-M3 and ARM® Cortex®-M0+. The STM32Lx series are the best choice to answer your needs in terms of ultra-low-power features. The STM32 Ultra-low-power series are the best solution for applications such as gas/water meter, keyboard/mouse or fitness and healthcare application. Several built-in features like LCD drivers, dual-bank memory, low-power Run mode, operational amplifiers, 128-bit AES, DAC, crystal-less USB and many other definitely help you building a highly cost optimized application by reducing BOM cost. STMicroelectronics, as a reliable and long-term manufacturer, ensures as much as possible pin-to-pin compatibility between all STM8Lx and STM32Lx on one hand, and between all STM32Lx and STM32Fx on the other hand. Thanks to this unprecedented scalability, your legacy application can be upgraded to respond to the latest market feature and efficiency requirements.

**Figure 9. STM32L011x3/4 TSSOP14 pinout**




1. The above figure shows the package top view.

**Table 12. Legend/abbreviations used in the pinout table**

| Name | | Abbreviation | Definition |
|---|---|---|---|
| Pin name | | Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name | |
| Pin type | | S | Supply pin |
| | | I | Input only pin |
| | | I/O | Input / output pin |
| I/O structure | | FT | 5 V tolerant I/O |
| | | FTf | 5 V tolerant I/O, FM+ capable |
| | | TTa | 3.3 V tolerant I/O directly connected to the ADC |
| | | TC | Standard 3.3V I/O |
| | | B | Dedicated BOOT0 pin |
| | | RST | Bidirectional reset pin with embedded weak pull-up resistor |
| Notes | | Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset. | |
| Pin functions | Alternate functions | Functions selected through GPIOx_AFR registers | |
| | Additional functions | Functions directly selected/enabled through peripheral registers | |

Table 13. Pin definitions (continued)

| Pin number | | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Pin functions | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TSSOP14 | UFQFPN20 | TSSOP20 | UFQFPN28 | LQFP32 | UFQFPN32[1] | WLCSP25 | | | | | Alternate functions | Additional functions |
| - | 8 | 11 | 11 | 11 | 11 | D3 | PA5 | I/O | TTa | - | SPI1_SCK, LPTIM1_IN2, TIM2_ETR, TIM2_CH1 | COMP1_INM, COMP2_INM, ADC_IN5 |
| - | 9 | 12 | 12 | 12 | 12 | E3 | PA6 | I/O | FT | - | SPI1_MISO, LPTIM1_ETR, LPUART1_CTS, EVENTOUT, COMP1_OUT | ADC_IN6 |
| 8 | 10 | 13 | 13 | 13 | 13 | C3 | PA7 | I/O | FT | - | SPI1_MOSI, LPTIM1_OUT, USART2_CTS, TIM21_ETR, EVENTOUT, COMP2_OUT | COMP2_INP, ADC_IN7 |
| - | - | - | 14 | 14 | 14 | E2 | PB0 | I/O | FT | - | EVENTOUT, SPI1_MISO, TIM2_CH2, USART2_RTS, TIM2_CH3 | ADC_IN8, VREF_OUT |
| - | 11 | 14 | 15 | 15 | 15 | D2 | PB1 | I/O | FT | - | USART2_CK, SPI1_MOSI, LPTIM1_IN1, LPUART1_RTS, TIM2_CH4 | ADC_IN9, VREF_OUT |
| - | - | - | - | - | 16 | - | PB2 | I/O | FT | - | LPTIM1_OUT | - |
| 9 | 12 | 15 | 16 | 16 | - | E1 | VSS | S | - | (5) | - | - |
| 10 | 13 | 16 | 17 | 17 | 17 | D1 | VDD | S | - | (6) | - | - |
| - | - | - | 18 | 18 | 18 | C1 | PA8 | I/O | FT | - | MCO, LPTIM1_IN1, EVENTOUT, USART2_CK, TIM2_CH1 | - |
| 11 | 14 | 17 | 19 | 19 | 19 | B1 | PA9 | I/O | FTf | - | MCO, I2C1_SCL, LPTIM1_OUT, USART2_TX, TIM21_CH2, COMP1_OUT | - |

Table 13. Pin definitions (continued)

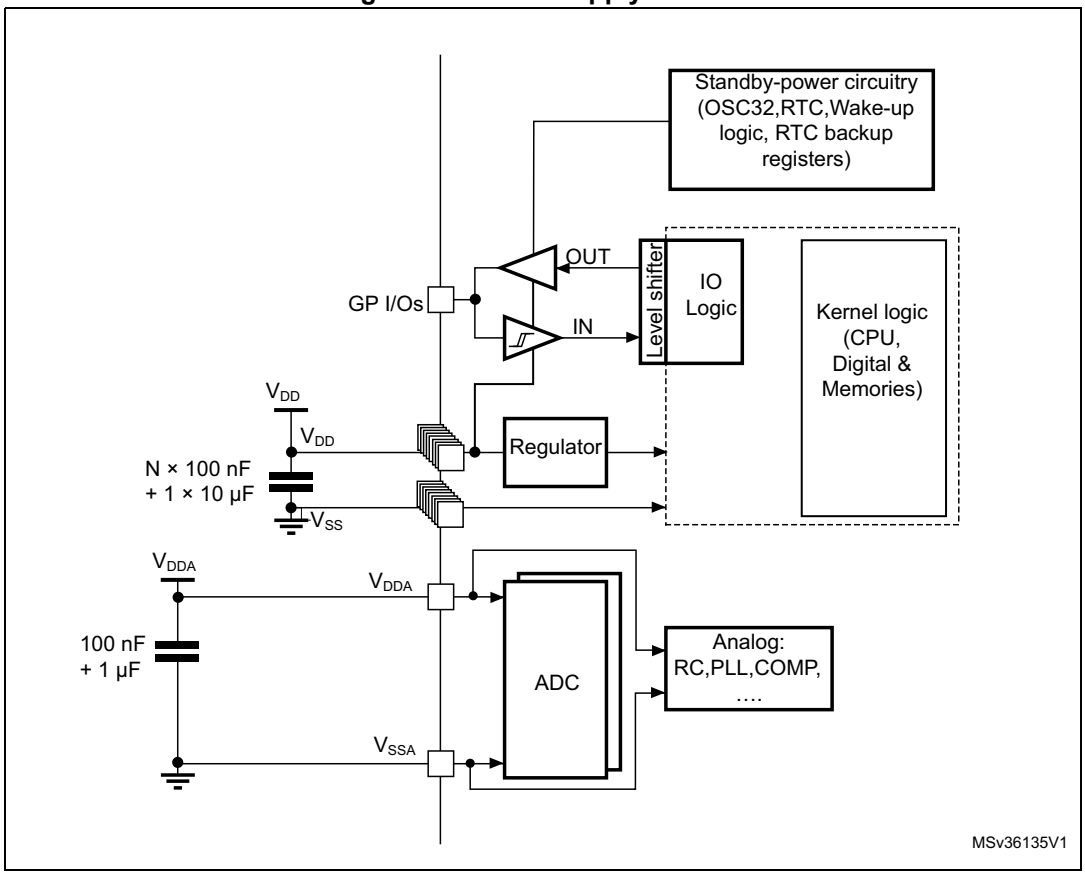
| Pin number | | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Pin functions | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TSSOP14 | UFQFPN20 | TSSOP20 | UFQFPN28 | LQFP32 | UFQFPN32[1] | WLCSP25 | | | | | Alternate functions | Additional functions |
| 12 | 15 | 18 | 20 | 20 | 20 | C2 | PA10 | I/O | FTf | - | TIM21_CH1, I2C1_SDA, RTC_REFIN, USART2_RX, TIM2_CH3, COMP1_OUT | - |
| - | - | - | - | 21 | 21 | - | PA11 | I/O | FT | - | SPI1_MISO, LPTIM1_OUT, EVENTOUT, USART2_CTS, TIM21_CH2, COMP1_OUT | - |
| - | - | - | - | 22 | 22 | - | PA12 | I/O | FT | - | SPI1_MOSI, EVENTOUT, USART2_RTS, COMP2_OUT | - |
| 13 | 16 | 19 | 21 | 23 | 23 | A1 | PA13 | I/O | FTf | - | SWDIO, LPTIM1_ETR, I2C1_SDA, SPI1_SCK, LPUART1_RX, COMP1_OUT | - |
| 14 | 17 | 20 | 22 | 24 | 24 | A2 | PA14 | I/O | FT | - | SWCLK, LPTIM1_OUT, I2C1_SMBA, USART2_TX, SPI1_MISO, LPUART1_TX, COMP2_OUT | - |
| - | - | - | 23 | 25 | 25 | - | PA15 | I/O | FT | - | SPI1_NSS, TIM2_ETR, EVENTOUT, USART2_RX, TIM2_CH1 | - |
| - | - | - | 24 | 26 | 26 | B2 | PB3 | I/O | FT | - | SPI1_SCK, TIM2_CH2, EVENTOUT | COMP2_INM |
| - | - | - | 25 | 27 | 27 | - | PB4 | I/O | FT | - | SPI1_MISO, EVENTOUT | COMP2_INP |

Table 14. Alternate functions (continued)

| Ports | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 |
|---|---|---|---|---|---|---|---|---|---|
| | | SPI1/USART2/ TIM21/ EVENTOUT/ SYS_AF | SPI1/I2C1/ LPTIM | LPUART1/ LPTIM/TIM2/ EVENTOUT/ SYS_AF | I2C1/LPTIM/ EVENTOUT | I2C1/USART2/LPUART1/ EVENTOUT | SPI1/TIM2/21 | LPUART1/EVEVENTOUT | COMP1/2 |
| Port B | PB0 | EVENTOUT | SPI1_MISO | TIM2_CH2 | - | USART2_RTS | TIM2_CH3 | - | - |
| | PB1 | USART2_CK | SPI1_MOSI | LPTIM1_IN1 | - | LPUART1_RTS | TIM2_CH4 | - | - |
| | PB2 | - | - | LPTIM1_OUT | - | - | - | - | - |
| | PB3 | SPI1_SCK | - | TIM2_CH2 | - | EVENTOUT | - | - | - |
| | PB4 | SPI1_MISO | - | EVENTOUT | - | - | - | - | - |
| | PB5 | SPI1_MOSI | - | LPTIM1_IN1 | I2C1_SMBA | - | TIM21_CH1 | - | - |
| | PB6 | USART2_TX | I2C1_SCL | LPTIM1_ETR | - | - | TIM2_CH3 | LPUART1_TX | - |
| | PB7 | USART2_RX | I2C1_SDA | LPTIM1_IN2 | - | - | TIM2_CH4 | LPUART1_RX | - |
| | PB8 | USART2_TX | - | EVENTOUT | - | I2C1_SCL | SPI1_NSS | - | - |
| | PB9 | - | - | - | - | - | - | - | - |
| Port C | PC14 | - | - | - | - | - | - | - | - |
| | PC15 | - | - | - | - | - | - | - | - |

### 6.1.6 Power supply scheme

**Figure 13. Power supply scheme**




1. On TSSOP14 package, $V_{DDA}$ is internally connected to $V_{DD}$.
2. $V_{SSA}$ is internally connected to $V_{SS}$ on all packages.

### 6.1.7 Current consumption measurement

**Figure 14. Current consumption measurement scheme**

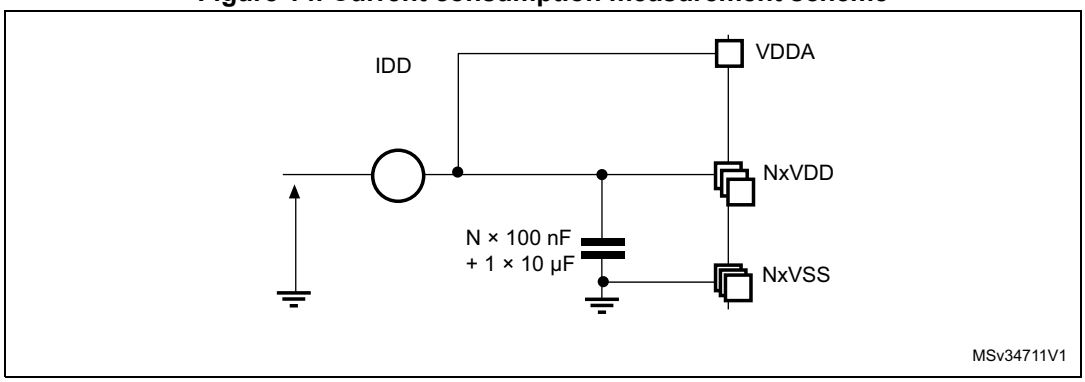


**Table 16. Current characteristics**

| Symbol | Ratings | Max. | Unit |
|---|---|---|---|
| $\Sigma I_{VDD}$ (2) | Total current into sum of all $V_{DD}$ power lines (source)(1) | 105 | mA |
| $\Sigma I_{VSS}$ (2) | Total current out of sum of all $V_{SS}$ ground lines (sink)(1) | 105 | |
| $I_{VDD(PIN)}$ | Maximum current into each $V_{DD}$ power pin (source)(1) | 100 | |
| $I_{VSS(PIN)}$ | Maximum current out of each $V_{SS}$ ground pin (sink)(1) | 100 | |
| $I_{IO}$ | Output current sunk by any I/O and control pin except FTf pins | 16 | |
| | Output current sunk by FTf pins | 22 | |
| | Output current sourced by any I/O and control pin | -16 | |
| $\Sigma I_{IO(PIN)}$ (3) | Total output current sunk by sum of all IOs and control pins(4) | 45 | |
| | Total output current sourced by sum of all IOs and control pins | -45 | |
| $\Sigma I_{IO(PIN)}$ | Total output current sunk by sum of all IOs and control pins(2) | 90 | |
| | Total output current sourced by sum of all IOs and control pins(2) | -90 | |
| $I_{INJ(PIN)}$ | Injected current on FT, FFf, RST and B pins | -5/+0(5) | |
| | Injected current on TC pin | ± 5(6) | |
| $\Sigma I_{INJ(PIN)}$ | Total injected current (sum of all I/O and control pins)(7) | ± 25 | |

1. All main power ($V_{DD}$, $V_{DDA}$) and ground ($V_{SS}$, $V_{SSA}$) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
3. These values apply only to STM32L011GxUx part number (UFQFPN28 package).
4. This current consumption must be correctly distributed over all I/Os and control pins. In particular, it must be located the closest possible to the couple of supply and ground, and distributed on both sides.
5. Positive current injection is not possible on these I/Os. A negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 15* for maximum allowed input voltage values.
6. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 15: Voltage characteristics* for the maximum allowed input voltage values.
7. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

**Table 17. Thermal characteristics**

| Symbol | Ratings | Value | Unit |
|---|---|---|---|
| $T_{STG}$ | Storage temperature range | –65 to +150 | °C |
| $T_J$ | Maximum junction temperature | 150 | °C |

4. Guaranteed by design, not tested in production.
5. Shortest sampling time can be determined in the application by multiple iterations.
6. To guarantee less than 1% VREF_OUT deviation.

### 6.3.4 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code. The current consumption is measured as described in *Figure 14: Current consumption measurement scheme*.

All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to Dhrystone 2.1 code if not specified otherwise.

The current consumption values are derived from the tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 18: General operating conditions* unless otherwise specified.

The MCU is placed under the following conditions:

- All I/O pins are configured in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time and prefetch is adjusted depending on $f_{HCLK}$ frequency and voltage range to provide the best CPU performance unless otherwise specified.
- When the peripherals are enabled $f_{APB1} = f_{APB2} = f_{APB}$
- When PLL is ON, the PLL inputs are equal to HSI = 16 MHz (if internal clock is used) or HSE = 16 MHz (if HSE bypass mode is used)
- The HSE user clock is applied to CK_IN. It follows the characteristic specified in *Table 35: High-speed external user clock characteristics*
- For maximum current consumption $V_{DD} = V_{DDA} = 3.6$ V is applied to all supply pins
- For typical current consumption $V_{DD} = V_{DDA} = 3.0$ V is applied to all supply pins if not specified otherwise

**Table 22. Current consumption in Run mode, code with data processing running from Flash**

| Symbol | Parameter | Conditions | | $f_{HCLK}$ | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|---|
| $I_{DD}$ (Run from Flash) | Supply current in Run mode, code executed from Flash | $f_{HSE} = f_{HCLK}$ up to 16 MHz included, $f_{HSE} = f_{HCLK}/2$ above 16 MHz (PLL ON)(2) | Range 3, $V_{CORE}$=1.2 V VOS[1:0]=11 | 1 MHz | 140 | 180 | µA |
| | | | | 2 MHz | 245 | 290 | |
| | | | | 4 MHz | 460 | 540 | |
| | | | Range 2, $V_{CORE}$=1.5 V, VOS[1:0]=10, | 4 MHz | 0.56 | 0.65 | mA |
| | | | | 8 MHz | 1.1 | 1.3 | |
| | | | | 16 MHz | 2.1 | 2.4 | |
| | | | Range 1, $V_{CORE}$=1.8 V, VOS[1:0]=01 | 8 MHz | 1.3 | 1.6 | |
| | | | | 16 MHz | 2.6 | 3 | |
| | | | | 32 MHz | 5.3 | 6.5 | |
| | | MSI clock | Range 3, $V_{CORE}$=1.2 V, VOS[1:0]=11 | 65 kHz | 34.5 | 54 | µA |
| | | | | 524 kHz | 86 | 120 | |
| | | | | 4.2 MHz | 505 | 560 | |
| | | HSI clock | Range 2, $V_{CORE}$=1.5 V, VOS[1:0]=10, | 16 MHz | 2.2 | 2.6 | mA |
| | | | Range 1, $V_{CORE}$=1.8 V, VOS[1:0]=01 | 32 MHz | 5.4 | 5.9 | |

1. Guaranteed by characterization results at 125 °C, not tested in production, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

**Table 23. Current consumption in Run mode vs code type, code with data processing running from Flash**

| Symbol | Parameter | Conditions | | | $f_{HCLK}$ | Typ | Unit |
|---|---|---|---|---|---|---|---|
| $I_{DD}$ (Run from Flash) | Supply current in Run mode, code executed from Flash | $f_{HSE} = f_{HCLK}$ up to 16 MHz included, $f_{HSE} = f_{HCLK}/2$ above 16 MHz (PLL ON)(1) | Range 3, $V_{CORE}$=1.2 V, VOS[1:0]=11 | Dhrystone | 4 MHz | 460 | µA |
| | | | | CoreMark | | 440 | |
| | | | | Fibonacci | | 330 | |
| | | | | while(1) | | 305 | |
| | | | | while(1), prefetch OFF | | 320 | |
| | | | Range 1, VOS[1:0]=01, $V_{CORE}$=1.8 V | Dhrystone | 32 MHz | 5.4 | mA |
| | | | | CoreMark | | 4.9 | |
| | | | | Fibonacci | | 5 | |
| | | | | while(1) | | 4.35 | |
| | | | | while(1), prefetch OFF | | 3.7 | |

1. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

**Figure 15. $I_{DD}$ vs $V_{DD}$, at $T_A$= 25 °C, Run mode, code running from Flash memory, Range 2, 16 MHz HSE, 1WS**

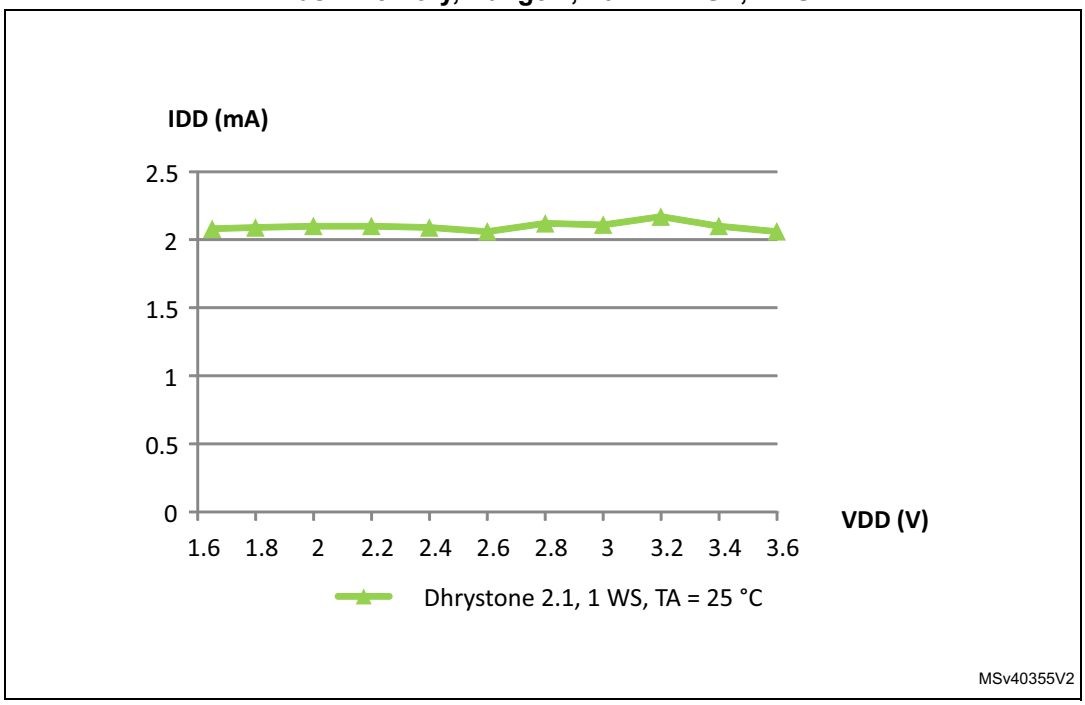



**Figure 16. $I_{DD}$ vs $V_{DD}$, at $T_A$= 25 °C, Run mode, code running from Flash memory, Range 2, HSI16, 1WS**

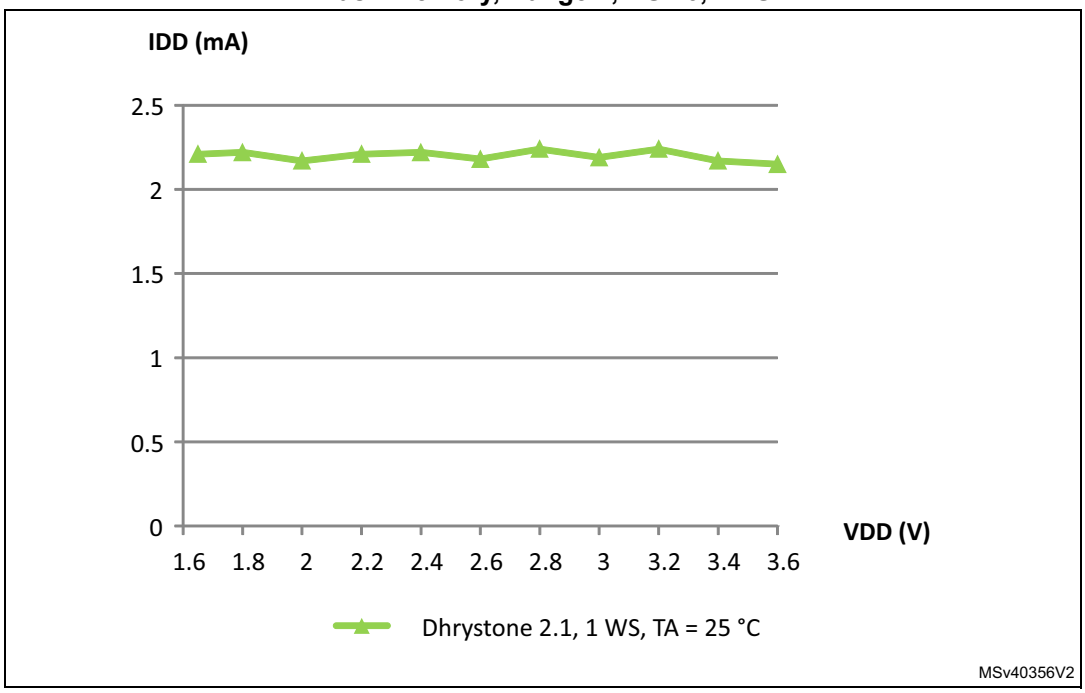


**Figure 17. $I_{DD}$ vs $V_{DD}$, at $T_A$= -40/25/55/ 85/105/125 °C, Low-power run mode, code running from RAM, Range 3, MSI (Range 0) at 64 KHz, 0 WS**

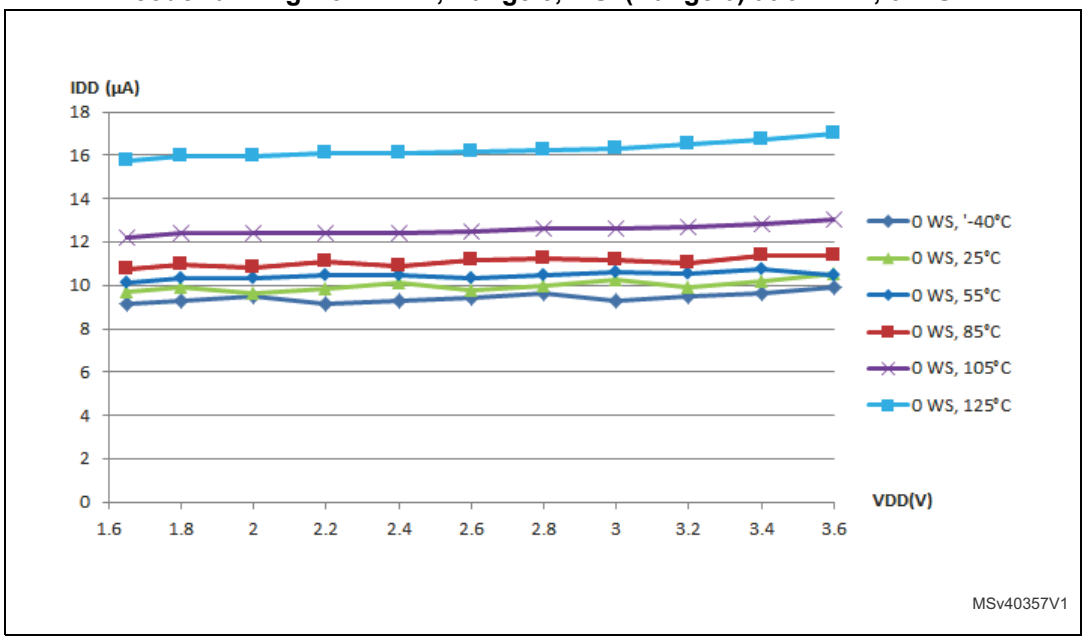



**Table 28. Current consumption in Low-power Sleep mode**

| Symbol | Parameter | Conditions | | | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|---|
| $I_{DD}$ (LP Sleep) | Supply current in Low-power sleep mode | All peripherals OFF, $V_{DD}$ from 1.65 V to 3.6 V | MSI clock, 65 kHz $f_{HCLK}$ = 32 kHz Flash OFF | $T_A$ = -40 °C to 25 °C | 2.5(2) | - | µA |
| | | | MSI clock, 65 kHz $f_{HCLK}$ = 32 kHz Flash ON | $T_A$ = -40 °C to 25 °C | 13 | 19 | |
| | | | | $T_A$ = 85 °C | 15.5 | 20 | |
| | | | | $T_A$ = 105 °C | 17.5 | 22 | |
| | | | | $T_A$ = 125 °C | 21 | 29 | |
| | | | MSI clock, 65 kHz $f_{HCLK}$ = 65 kHz, Flash ON | $T_A$ = -40 °C to 25 °C | 13.5 | 19 | |
| | | | | $T_A$ = 85 °C | 16 | 20 | |
| | | | | $T_A$ = 105 °C | 18 | 22 | |
| | | | | $T_A$ = 125 °C | 21.5 | 29 | |
| | | | MSI clock, 131 kHz $f_{HCLK}$ = 131 kHz, Flash ON | $T_A$ = -40 °C to 25 °C | 15.5 | 21 | |
| | | | | $T_A$ = 55 °C | 17 | 22 | |
| | | | | $T_A$ = 85 °C | 18 | 23 | |
| | | | | $T_A$ = 105 °C | 19.5 | 24 | |
| | | | | $T_A$ = 125 °C | 23.5 | 31 | |

1. Guaranteed by characterization results at 125 °C, not tested in production, unless otherwise specified.
2. As the CPU is in Sleep mode, the difference between the current consumption with Flash memory ON and OFF (nearly 12 µA) is the same whatever the clock frequency.

**Table 48. Electrical sensitivities**

| Symbol | Parameter | Conditions | Class |
|---|---|---|---|
| LU | Static latch-up class | $T_A$ = +125 °C conforming to JESD78A | II level A |

## 6.3.12 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below $V_{SS}$ or above $V_{DD}$ (for standard pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

### Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range), or other functional failure (for example reset occurrence oscillator frequency deviation).

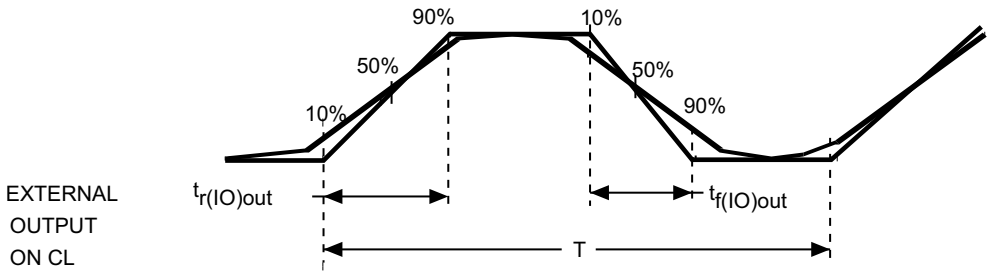
The test results are given in the *Table 49*.

**Table 49. I/O current injection susceptibility**

| Symbol | Description | Functional susceptibility | | Unit |
|---|---|---|---|---|
| | | Negative injection | Positive injection | |
| $I_{INJ}$ | Injected current on BOOT0 | -0 | NA | mA |
| | Injected current on all FT pins | -5 (1) | NA | |
| | Injected current on any other pin | -5 (1) | +5 | |

1. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

**Figure 26. I/O AC characteristics definition**




Maximum frequency is achieved if ($t_r$ + $t_f$) ≤ (2/3)T and if the duty cycle is (45-55%) when loaded by CL specified in the table " *I/O AC characteristics*".

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## 6.3.14 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, $R_{PU}$ , except when it is internally driven low (see *Table 53*).

Unless otherwise specified, the parameters given in *Table 53* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 18*.

**Table 53. NRST pin characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL(NRST)}$(1) | NRST input low level voltage | - | - | - | $0.3V_{DD}$ | V |
| $V_{IH(NRST)}$(1) | NRST input high level voltage | - | $0.39V_{DD}$+ 0.59 | - | - | |
| $V_{OL(NRST)}$(1) | NRST output low level voltage | $I_{OL}$ = 2 mA 2.7 V < $V_{DD}$ < 3.6 V | - | - | 0.4 | |
| | | $I_{OL}$ = 1.5 mA 1.65 V < $V_{DD}$ < 2.7 V | - | - | | |
| $V_{hys(NRST)}$(1) | NRST Schmitt trigger voltage hysteresis | - | - | $10\%V_{DD}$(2) | - | mV |
| $R_{PU}$ | Weak pull-up equivalent resistor(3) | $V_{IN}$ = $V_{SS}$ | 30 | 45 | 60 | kΩ |
| $V_{F(NRST)}$(1) | NRST input filtered pulse | - | - | - | 50 | ns |
| $V_{NF(NRST)}$(1) | NRST input not filtered pulse | - | 350 | - | - | ns |

1. Guaranteed by design, not tested in production.
2. 200 mV minimum value
3. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is around 10%.

## 6.3.19 Communications interfaces

### I²C interface characteristics

The I²C interface meets the timings requirements of the I²C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm) : with a bit rate up to 100 kbit/s
- Fast-mode (Fm) : with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+) : with a bit rate up to 1 Mbit/s.

The I²C timing requirements are guaranteed by design when the I²C peripheral is properly configured (refer to the reference manual for details) and when the I2CCLK frequency is greater than the minimum given in *Table 63*. The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not "true" open-drain. When configured as open-drain, the PMOS connected between the I/O pin and VDDIOx is disabled, but is still present. Only FTf I/O pins support Fm+ low level output current maximum requirement (refer to *Section 6.3.13: I/O port characteristics* for the I2C I/Os characteristics).

All I²C SDA and SCL I/Os embed an analog filter (see *Table 62* for the analog filter characteristics).

**Table 62. I2C analog filter characteristics(1)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{AF}$ | Maximum pulse width of spikes that are suppressed by the analog filter | 50(2) | 100(3) | ns |

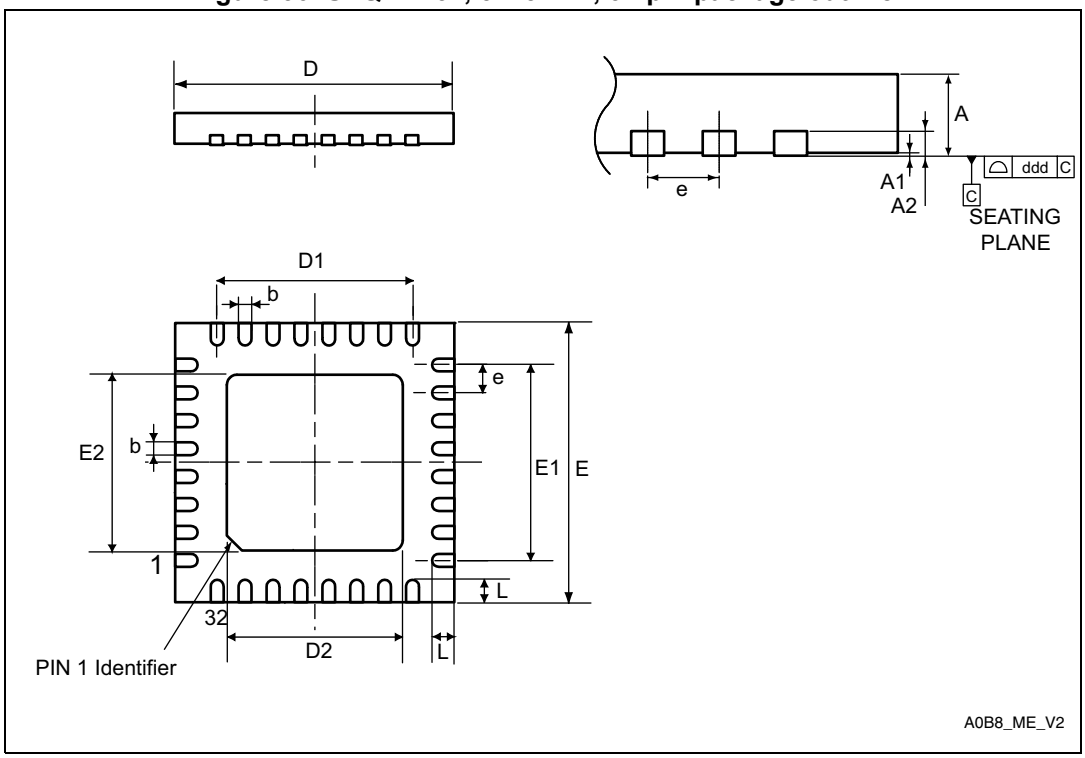
1. Guaranteed by design, not tested in production.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered

**Table 63. I2C frequency in all I2C modes**

| Symbol | Parameter | Condition | | Min | Unit |
|---|---|---|---|---|---|
| $f_{I2CCLK}$ | I2C clock frequency | Standard-mode | | 2 | MHz |
| | | Fast-mode | | 8 | |
| | | Fast-mode Plus | Analog filter ON, DNF = 0 | 18 | |
| | | | Analog filter OFF, DNF = 1 | 16 | |

## 7.2 UFQFPN32 package information

**Figure 36. UFQFPN32, 5 x 5 mm, 32-pin package outline**




1. Drawing is not to scale.

**Table 69. UFQFPN32, 5 x 5 mm, 32-pin package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.500 | 0.550 | 0.600 | 0.0197 | 0.0217 | 0.0236 |
| A1 | 0.000 | 0.020 | 0.050 | 0.0000 | 0.0008 | 0.0020 |
| A3 | - | 0.200 | - | - | 0.0079 | - |
| b | 0.180 | 0.250 | 0.300 | 0.0071 | 0.0098 | 0.0118 |
| D | 4.900 | 5.000 | 5.100 | 0.1929 | 0.1969 | 0.2008 |
| D2 | 3.200 | 3.450 | 3.700 | 0.1260 | 0.1358 | 0.1457 |
| E | 4.900 | 5.000 | 5.100 | 0.1929 | 0.1969 | 0.2008 |
| E2 | 3.200 | 3.450 | 3.700 | 0.1260 | 0.1358 | 0.1457 |
| e | - | 0.500 | - | - | 0.0197 | - |
| L | 0.300 | 0.400 | 0.500 | 0.0118 | 0.0157 | 0.0197 |
| ddd | - | - | 0.080 | - | - | 0.0031 |

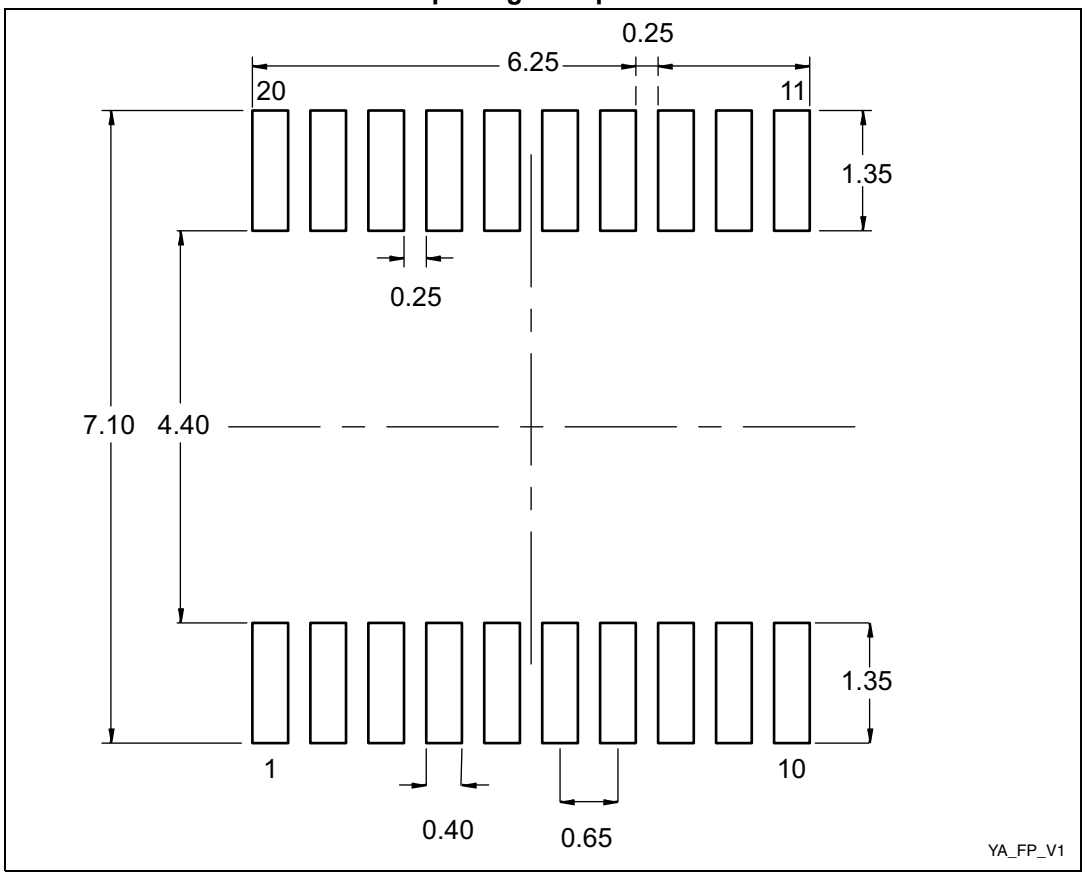
1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Table 74. TSSOP20 – 20-lead thin shrink small outline, 6.5 x 4.4 mm, 0.65 mm pitch, package mechanical data (continued)**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| k | 0° | - | 8° | 0° | - | 8° |
| aaa | - | - | 0.100 | - | - | 0.0039 |

1. Values in inches are converted from mm and rounded to four decimal digits.

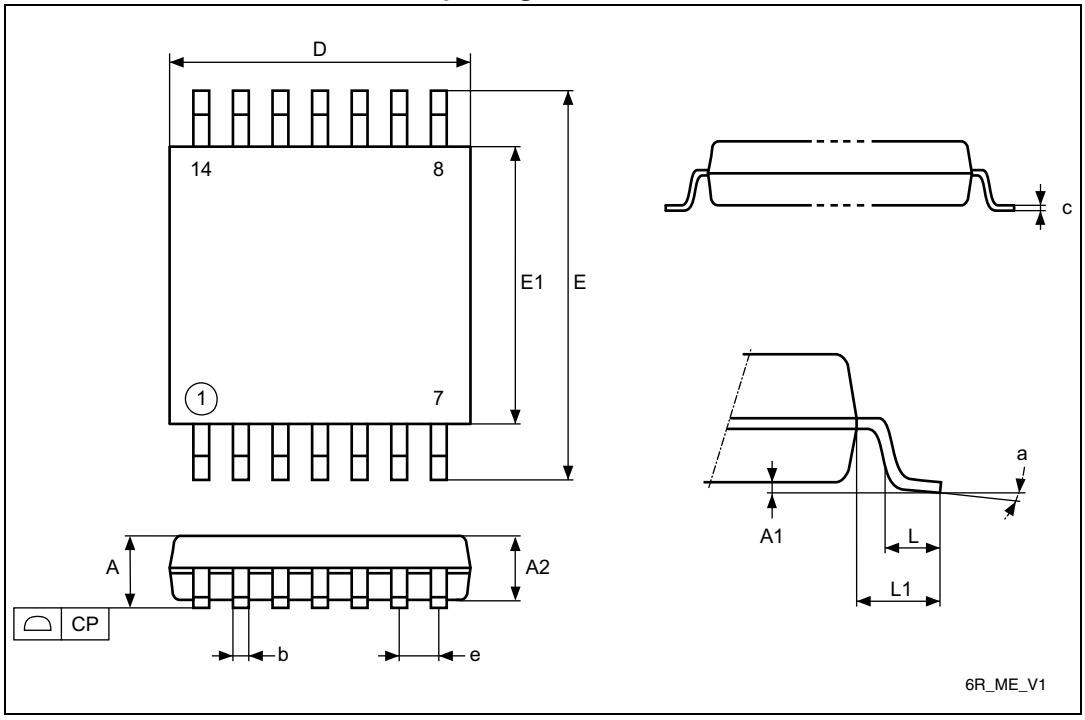
**Figure 49. TSSOP20 – 20-lead thin shrink small outline, 6.5 x 4.4 mm, 0.65 mm pitch, package footprint**




1. Dimensions are expressed in millimeters.

## 7.7 TSSOP14 package information

**Figure 51.TSSOP14 – 14-lead thin shrink small outline, 5.0 x 4.4 mm, 0.65 mm pitch, package outline**




1. Drawing is not to scale.

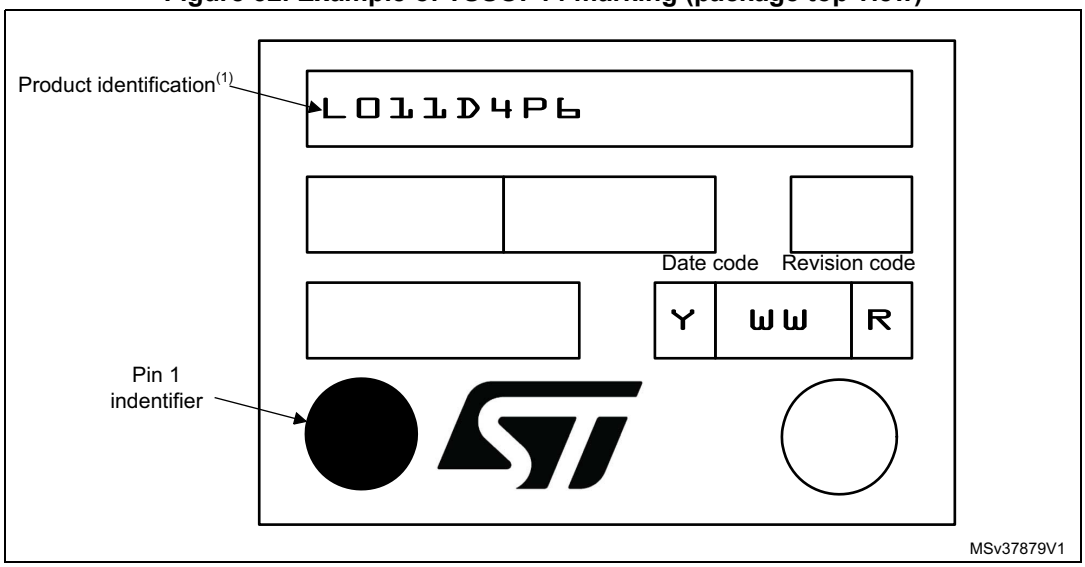
**Table 75. TSSOP14 – 14-lead thin shrink small outline, 5.0 x 4.4 mm, 0.65 mm pitch, package mechanical data**

| Symbol | millimeters | | | inches | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.200 | - | - | 0.0472 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 0.800 | 1.000 | 1.050 | 0.0315 | 0.0394 | 0.0413 |
| b | 0.190 | - | 0.300 | 0.0075 | - | 0.0118 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| CP | - | - | 0.100 | - | - | 0.0039 |
| D | 4.900 | 5.000 | 5.100 | 0.1929 | 0.1969 | 0.2008 |
| e | - | 0.650 | - | - | 0.0256 | - |
| E | 6.200 | 6.400 | 6.600 | 0.2441 | 0.2520 | 0.2598 |
| E1 | 4.300 | 4.400 | 4.500 | 0.1693 | 0.1732 | 0.1772 |
| L | 0.500 | 0.600 | 0.750 | 0.0197 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| a | 0° | - | 8° | 0° | - | 8° |

### TSSOP14 device marking

The following figure gives an example of topside marking versus pin 1 position identifier location.

**Figure 52. Example of TSSOP14 marking (package top view)**




1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

## 7.8 Thermal characteristics

The maximum chip-junction temperature, $T_J$ max, in degrees Celsius, may be calculated using the following equation:

$T_J$ max = $T_A$ max + ($P_D$ max × $\Theta_{JA}$)

Where:

- $T_A$ max is the maximum ambient temperature in °C,
- $\Theta_{JA}$ is the package junction-to-ambient thermal resistance, in °C/W,
- $P_D$ max is the sum of $P_{INT}$ max and $P_{I/O}$ max ($P_D$ max = $P_{INT}$ max + $P_{I/O}$max),
- $P_{INT}$ max is the product of $I_{DD}$ and $V_{DD}$, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$P_{I/O}$ max = $\Sigma$ ($V_{OL}$ × $I_{OL}$) + $\Sigma$(($V_{DD}$ – $V_{OH}$) × $I_{OH}$),

taking into account the actual $V_{OL}$ / $I_{OL}$ and $V_{OH}$ / $I_{OH}$ of the I/Os at low and high level in the application.