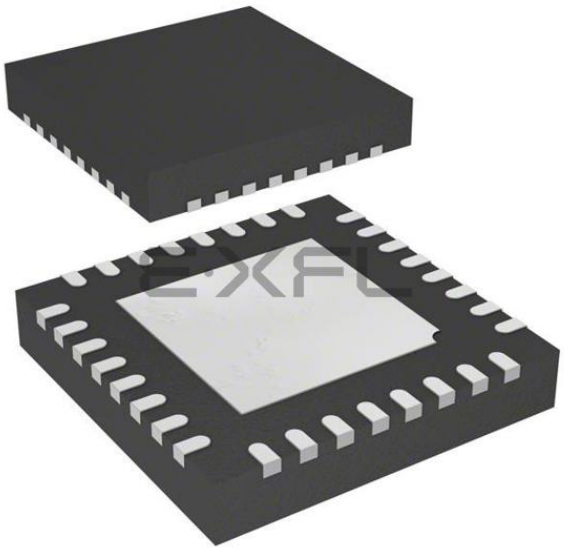

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	28
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-UFQFPN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l011k4u6tr

Figure 1. STM32L011x3/4 block diagram

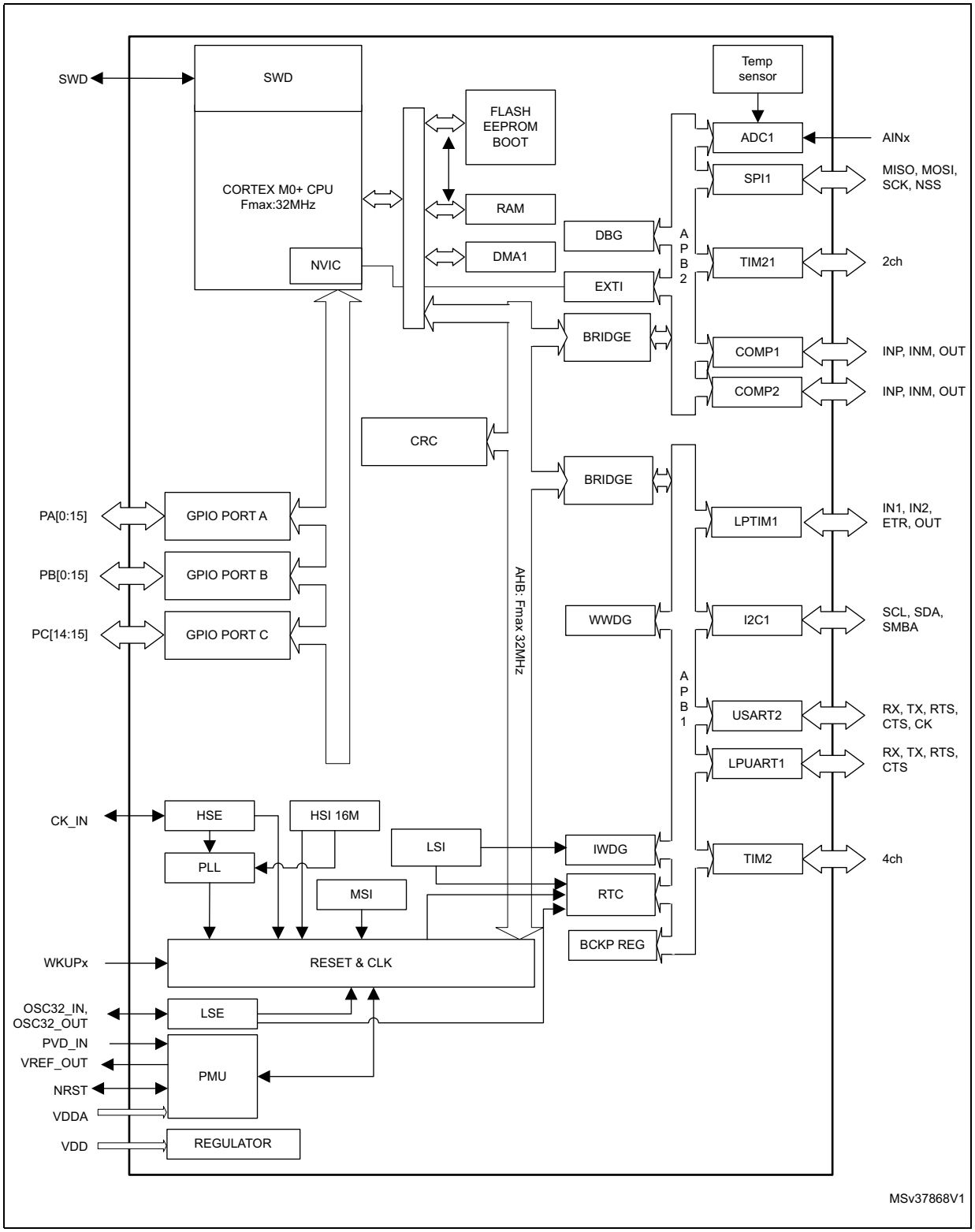


Table 5. Functionalities depending on the working mode (from Run/active down to standby) (continued)[1][2]

IPs	Run/Active	Sleep	Low-power run	Low-power sleep	Stop		Standby	
						Wakeup capability		Wakeup capability
Programmable Voltage Detector (PVD)	O	O	O	O	O	O	-	-
Power-on/down reset (POR/PDR)	Y	Y	Y	Y	Y	Y	Y	Y
High Speed Internal (HSI)	O	O	-	-	[3]	-	-	-
High Speed External (HSE)	O	O	O	O	-	-	-	-
Low Speed Internal (LSI)	O	O	O	O	O	-	O	-
Low Speed External (LSE)	O	O	O	O	O	-	O	-
Multi-Speed Internal (MSI)	O	O	Y	Y	-	-	-	-
Inter-Connect Controller	Y	Y	Y	Y	Y	-	-	-
RTC	O	O	O	O	O	O	O	-
RTC Tamper	O	O	O	O	O	O	O	O
Auto WakeUp (AWU)	O	O	O	O	O	-	O	O
USART	O	O	O	O	O[4]	O	-	-
LPUART	O	O	O	O	O[4]	O	-	-
SPI	O	O	O	O	-		-	-
I2C	O	O	O	O	O[5]	O	-	-
ADC	O	O	-	-	-	-	-	-
Temperature sensor	O	O	O	O	O	-	-	-
Comparators	O	O	O	O	O	O	-	-
16-bit timers	O	O	O	O	-	-	-	-
LPTIM	O	O	O	O	O	O	-	-
IWDG	O	O	O	O	O	O	O	O
WWDG	O	O	O	O	-	-	-	-
SysTick Timer	O	O	O	O	-	-	-	-
GPIOs	O	O	O	O	O	O	-	2 pins

Nested vectored interrupt controller (NVIC)

The ultra-low-power STM32L011x3/4 embed a nested vectored interrupt controller able to handle up to 32 maskable interrupt channels and 4 priority levels.

The Cortex-M0+ processor closely integrates a configurable Nested Vectored Interrupt Controller (NVIC), to deliver industry-leading interrupt performance. The NVIC:

- includes a Non-Maskable Interrupt (NMI)
- provides zero jitter interrupt option
- provides four interrupt priority levels

The tight integration of the processor core and NVIC provides fast execution of Interrupt Service Routines (ISRs), dramatically reducing the interrupt latency. This is achieved through the hardware stacking of registers, and the ability to abandon and restart load-multiple and store-multiple operations. Interrupt handlers do not require any assembler wrapper code, removing any code overhead from the ISRs. Tail-chaining optimization also significantly reduces the overhead when switching from one ISR to another.

To optimize low-power designs, the NVIC integrates with the sleep modes, that include a deep sleep function that enables the entire device to enter rapidly stop or standby mode.

This hardware block provides flexible interrupt management features with minimal interrupt latency.

3.4 Reset and supply management

3.4.1 Power supply schemes

- V_{DD} = 1.65 to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 1.65 to 3.6 V: external analog power supplies for ADC, reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively. On TSSOP14 package, V_{DDA} is internally connected to V_{DD}.

3.4.2 Power supply supervisor

The devices feature an integrated ZEROPOWER power-on reset (POR)/power-down reset (PDR) that can be coupled with a brownout reset (BOR) circuitry.

Two versions are available:

- The version with BOR activated at power-on operates between 1.8 V and 3.6 V.
- The other version without BOR operates between 1.65 V and 3.6 V.

After the V_{DD} threshold is reached (1.65 V or 1.8 V depending on the BOR which is active or not at power-on), the option byte loading process starts, either to confirm or modify default thresholds, or to disable the BOR permanently: in this case, the VDD min value becomes 1.65 V (whatever the version, BOR active or not, at power-on).

When BOR is active at power-on, it ensures proper operation starting from 1.8 V whatever the power ramp-up phase before it reaches 1.8 V. When BOR is not active at power-up, the power ramp-up should guarantee that 1.65 V is reached on V_{DD} at least 1 ms after it exits the POR area.

3.14.4 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 37 kHz internal RC and, as it operates independently of the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes. The counter can be frozen in debug mode.

3.14.5 Window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.15 Communication interfaces

3.15.1 I^2C bus

One I^2C interface (I2C1) can operate in multimaster or slave modes. The I^2C interface can support Standard mode (Sm, up to 100 kbit/s), Fast mode (Fm, up to 400 kbit/s) and Fast Mode Plus (Fm+, up to 1 Mbit/s) with 20 mA output drive on some I/Os.

The I^2C interface supports 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (2 addresses, 1 with configurable mask). They also include programmable analog and digital noise filters.

Table 8. Comparison of I2C analog and digital filters

	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2C peripheral clocks
Benefits	Available in Stop mode	1. Extra filtering capability vs. standard requirements. 2. Stable length
Drawbacks	Variations depending on temperature, voltage, process	Wakeup from Stop on address match is not available when digital filter is enabled.

In addition, I2C1 provides hardware support for SMBus 2.0 and PMBus 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts verifications and ALERT protocol management. I2C1 also has a clock domain independent from the CPU clock, allowing the I2C1 to wake up the MCU from Stop mode on address match.

The I2C interface can be served by the DMA controller.

Refer to *Table 9* for the supported modes and features of I2C interface.

Table 9. STM32L011x3/4 I²C implementation

I2C features[1]	I2C1
7-bit addressing mode	X
10-bit addressing mode	X
Standard mode (up to 100 kbit/s)	X
Fast mode (up to 400 kbit/s)	X
Fast Mode Plus with 20 mA output drive I/Os (up to 1 Mbit/s)	X[2]
Independent clock	X
SMBus	X
Wakeup from STOP	X

1. X = supported.
2. See *Table 13: Pin definitions on page 37* for the list of I/Os that feature Fast Mode Plus capability

3.15.2 Universal synchronous/asynchronous receiver transmitter (USART)

The USART interface (USART2) is able to communicate at speeds of up to 4 Mbit/s.

It provides hardware management of the CTS, RTS and RS485 driver enable (DE) signals, multiprocessor communication mode and single-wire half-duplex communication mode. USART2 also supports Smartcard communication (ISO 7816, T=0 protocol) and IrDA SIR ENDEC.

USART2 interface can be served by the DMA controller.

Table 10 for the supported modes and features of USART interface.

Table 10. USART implementation

USART modes/features[1]	USART2
Hardware flow control for modem	X
Continuous communication using DMA	X
Multiprocessor communication	X
Synchronous mode	-
Smartcard mode	X
Single-wire half-duplex communication	X
IrDA SIR ENDEC block	X
LIN mode	-
Dual clock domain and wakeup from Stop mode	-
Receiver timeout interrupt	-
Modbus communication	-
Auto baud rate detection (4 modes)	-
Driver Enable	X

1. X = supported.

Table 13. Pin definitions (continued)

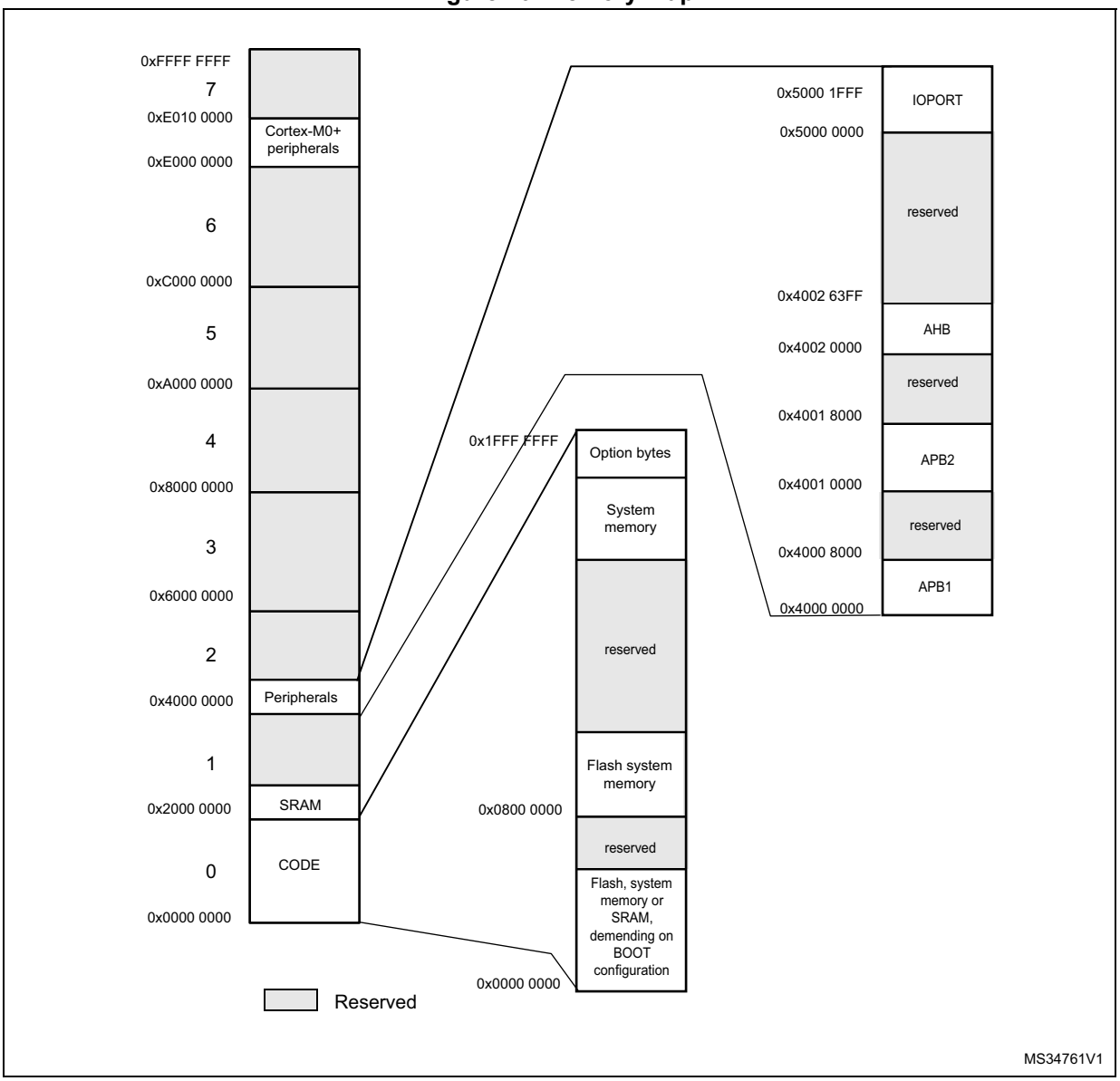
Pin number							Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
TSSOP14	UFQFPN20	TSSOP20	UFQFPN28	LQFP32	UFQFPN32[1]	WLCSP25					Alternate functions	Additional functions
12	15	18	20	20	20	C2	PA10	I/O	FTf	-	TIM21_CH1, I2C1_SDA, RTC_REFIN, USART2_RX, TIM2_CH3, COMP1_OUT	-
-	-	-	-	21	21	-	PA11	I/O	FT	-	SPI1_MISO, LPTIM1_OUT, EVENTOUT, USART2_CTS, TIM21_CH2, COMP1_OUT	-
-	-	-	-	22	22	-	PA12	I/O	FT	-	SPI1_MOSI, EVENTOUT, USART2_RTS, COMP2_OUT	-
13	16	19	21	23	23	A1	PA13	I/O	FTf	-	SWDIO, LPTIM1_ETR, I2C1_SDA, SPI1_SCK, LPUART1_RX, COMP1_OUT	-
14	17	20	22	24	24	A2	PA14	I/O	FT	-	SWCLK, LPTIM1_OUT, I2C1_SMBA, USART2_TX, SPI1_MISO, LPUART1_TX, COMP2_OUT	-
-	-	-	23	25	25	-	PA15	I/O	FT	-	SPI1_NSS, TIM2_ETR, EVENTOUT, USART2_RX, TIM2_CH1	-
-	-	-	24	26	26	B2	PB3	I/O	FT	-	SPI1_SCK, TIM2_CH2, EVENTOUT	COMP2_INM
-	-	-	25	27	27	-	PB4	I/O	FT	-	SPI1_MISO, EVENTOUT	COMP2_INP

Table 14. Alternate functions (continued)

Ports		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SPI1/USART2/ TIM21/ EVENTOUT/ SYS_AF	SPI1/I2C1/ LPTIM	LPUART1/ LPTIM/TIM2/ EVENTOUT/ SYS_AF	I2C1/LPTIM/ EVENTOUT	I2C1/USART2/LPUART1/ EVENTOUT	SPI1/TIM2/21	LPUART1/EVEVENTOUT	COMP1/2
Port B	PB0	EVENTOUT	SPI1_MISO	TIM2_CH2	-	USART2_RTS	TIM2_CH3	-	-
	PB1	USART2_CK	SPI1_MOSI	LPTIM1_IN1	-	LPUART1_RTS	TIM2_CH4	-	-
	PB2	-	-	LPTIM1_OUT	-	-	-	-	-
	PB3	SPI1_SCK	-	TIM2_CH2	-	EVENTOUT	-	-	-
	PB4	SPI1_MISO	-	EVENTOUT	-	-	-	-	-
	PB5	SPI1_MOSI	-	LPTIM1_IN1	I2C1_SMBA	-	TIM21_CH1	-	-
	PB6	USART2_TX	I2C1_SCL	LPTIM1_ETR	-	-	TIM2_CH3	LPUART1_TX	-
	PB7	USART2_RX	I2C1_SDA	LPTIM1_IN2	-	-	TIM2_CH4	LPUART1_RX	-
	PB8	USART2_TX	-	EVENTOUT	-	I2C1_SCL	SPI1_NSS	-	-
	PB9	-	-	-	-	-	-	-	-
Port C	PC14	-	-	-	-	-	-	-	-
	PC15	-	-	-	-	-	-	-	-

5 Memory mapping

Figure 10. Memory map



1. Refer to the STM32L011x3/4 reference manual for details on the Flash memory organization for each memory size.

Table 18. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
T_A	Temperature range	Maximum power dissipation (range 6)	–40	85	°C
		Maximum power dissipation (range 7)	–40	105	
		Maximum power dissipation (range 3)	–40	125	
T_J	Junction temperature range (range 6)	-40 °C ≤ T_A ≤ 85 °	–40	105	
	Junction temperature range (range 7)	-40 °C ≤ T_A ≤ 105 °C	–40	125	
	Junction temperature range (range 3)	-40 °C ≤ T_A ≤ 125 °C	–40	130	

1. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and normal operation.
2. To sustain a voltage higher than V_{DD}+0.3V, the internal pull-up/pull-down resistors must be disabled.
3. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_J max (see *Table 17: Thermal characteristics on page 47*).

6.3.2 Embedded reset and power control block characteristics

The parameters given in the following table are derived from the tests performed under the ambient temperature condition summarized in *Table 18*.

Table 19. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VDD}(1)	V_{DD} rise time rate	BOR detector enabled	0	-	∞	µs/V
		BOR detector disabled	0	-	1000	
	V_{DD} fall time rate	BOR detector enabled	20	-	∞	
		BOR detector disabled	0	-	1000	
$T_{RSTTEMPO}$(1)	Reset temporization	V_{DD} rising, BOR enabled	-	2	3.3	ms
		V_{DD} rising, BOR disabled(2)	0.4	0.7	1.6	
$V_{POR/PDR}$	Power on/power down reset threshold	Falling edge	1	1.5	1.65	V
		Rising edge	1.3	1.5	1.65	
V_{BOR0}	Brown-out reset threshold 0	Falling edge	1.67	1.7	1.74	
		Rising edge	1.69	1.76	1.8	
V_{BOR1}	Brown-out reset threshold 1	Falling edge	1.87	1.93	1.97	
		Rising edge	1.96	2.03	2.07	
V_{BOR2}	Brown-out reset threshold 2	Falling edge	2.22	2.30	2.35	
		Rising edge	2.31	2.41	2.44	

4. Guaranteed by design, not tested in production.
5. Shortest sampling time can be determined in the application by multiple iterations.
6. To guarantee less than 1% VREF_OUT deviation.

6.3.4 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code. The current consumption is measured as described in *Figure 14: Current consumption measurement scheme*.

All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to Dhrystone 2.1 code if not specified otherwise.

The current consumption values are derived from the tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 18: General operating conditions* unless otherwise specified.

The MCU is placed under the following conditions:

- All I/O pins are configured in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time and prefetch is adjusted depending on f_{HCLK} frequency and voltage range to provide the best CPU performance unless otherwise specified.
- When the peripherals are enabled $f_{APB1} = f_{APB2} = f_{APB}$
- When PLL is ON, the PLL inputs are equal to HSI = 16 MHz (if internal clock is used) or HSE = 16 MHz (if HSE bypass mode is used)
- The HSE user clock is applied to CK_IN. It follows the characteristic specified in *Table 35: High-speed external user clock characteristics*
- For maximum current consumption $V_{DD} = V_{DDA} = 3.6$ V is applied to all supply pins
- For typical current consumption $V_{DD} = V_{DDA} = 3.0$ V is applied to all supply pins if not specified otherwise

Table 26. Current consumption in Sleep mode

Symbol	Parameter	Conditions		f_{HCLK}	Typ	Max(1)	Unit
I_{DD} (Sleep)	Supply current in Sleep mode, Flash OFF	f_{HSE} = f_{HCLK} up to 16 MHz included, f_{HSE} = f_{HCLK}/2 above 16 MHz (PLL ON)(2)	Range 3, V_{CORE}=1.2 V, VOS[1:0]=11	1 MHz	36.5	70	µA
				2 MHz	58	95	
				4 MHz	100	150	
			Range 2, V_{CORE}=1.5 V, VOS[1:0]=10	4 MHz	125	170	
				8 MHz	230	300	
				16 MHz	450	540	
			Range 1, V_{CORE}=1.8 V, VOS[1:0]=01	8 MHz	275	350	
				16 MHz	555	650	
				32 MHz	1350	1600	
		MSI clock	Range 3, V_{CORE}=1.2 V, VOS[1:0]=11	65 kHz	15.5	32	
				524 kHz	26.5	55	
				4.2 MHz	115	160	
		HSI16 clock source (16 MHz)	Range 2, V_{CORE}=1.5 V, VOS[1:0]=10	16 MHz	585	670	
			Range 1, V_{CORE}=1.8 V, VOS[1:0]=01	32 MHz	1500	1700	
	Supply current in Sleep mode, Flash ON	f_{HSE} = f_{HCLK} up to 16 MHz included, f_{HSE} = f_{HCLK}/2 above 16 MHz (PLL ON)(2)	Range 3, V_{CORE}=1.2 V, VOS[1:0]=11	1 MHz	49	88	
				2 MHz	69	120	
				4 MHz	115	190	
			Range 2, CORE=1.5 V, VOS[1:0]=10	4 MHz	135	200	
				8 MHz	240	340	
				16 MHz	460	650	
			Range 1, V_{CORE}=1.8 V, VOS[1:0]=01	8 MHz	290	400	
				16 MHz	565	750	
				32 MHz	1350	1900	
		MSI clock	Range 3, V_{CORE}=1.2 V, VOS[1:0]=11	65 kHz	26.5	46	
				524 kHz	38.5	70	
				4.2 MHz	125	190	
		HSI16 clock source (16 MHz)	Range 2, V_{CORE}=1.5 V, VOS[1:0]=10	16 MHz	600	760	
			Range 1, V_{CORE}=1.8 V, VOS[1:0]=01	32 MHz	1500	1850	

1. Guaranteed by characterization results at 125 °C, not tested in production, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

Table 34. Low-power mode wakeup timings (continued)

Symbol	Parameter	Conditions	Typ	Max	Unit
t_{WUSTOP}	Wakeup from Stop mode, regulator in Run mode	$f_{HCLK} = f_{MSI}$ = 4.2 MHz	5.1	8	µs
		$f_{HCLK} = f_{HSI}$ = 16 MHz	5.1	7	
		$f_{HCLK} = f_{HSI}/4$ = 4 MHz	8.1	11	
	Wakeup from Stop mode, regulator in low-power mode	$f_{HCLK} = f_{MSI}$ = 4.2 MHz Voltage range 1	5	8	
		$f_{HCLK} = f_{MSI}$ = 4.2 MHz Voltage range 2	5	8	
		$f_{HCLK} = f_{MSI}$ = 4.2 MHz Voltage range 3	5	8	
		$f_{HCLK} = f_{MSI}$ = 2.1 MHz	7.4	13	
		$f_{HCLK} = f_{MSI}$ = 1.05 MHz	14	23	
		$f_{HCLK} = f_{MSI}$ = 524 kHz	28	38	
		$f_{HCLK} = f_{MSI}$ = 262 kHz	51	65	
		$f_{HCLK} = f_{MSI}$ = 131 kHz	99	120	
		$f_{HCLK} = f_{MSI}$ = 65 kHz	196	260	
		$f_{HCLK} = f_{HSI}$ = 16 MHz	5.1	7	
		$f_{HCLK} = f_{HSI}/4$ = 4 MHz	8.2	11	
	Wakeup from Stop mode, regulator in low-power mode, HSI kept running in Stop mode	$f_{HCLK} = f_{HSI}$ = 16 MHz	3.25	-	
	Wakeup from Stop mode, regulator in low-power mode, code running from RAM	$f_{HCLK} = f_{HSI}$ = 16 MHz	4.9	7	
		$f_{HCLK} = f_{HSI}/4$ = 4 MHz	7.9	10	
		$f_{HCLK} = f_{MSI}$ = 4.2 MHz	4.8	8	
$t_{WUSTDBY}$	Wakeup from Standby mode FWU bit = 1	$f_{HCLK} = f_{MSI}$ = 2.1 MHz	65	130	
	Wakeup from Standby mode FWU bit = 0	$f_{HCLK} = f_{MSI}$ = 2.1 MHz	2.2	3	ms

6.3.6 External clock source characteristics

High-speed external user clock generated from an external source

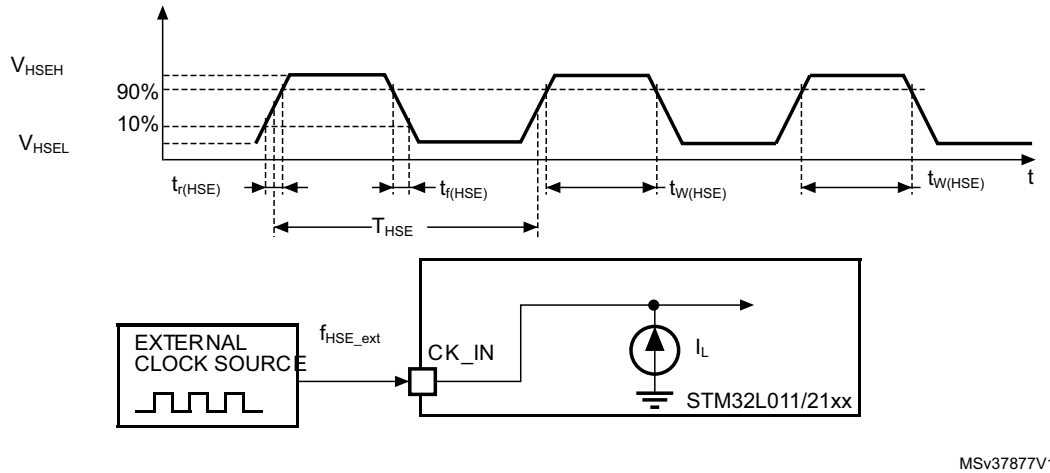
In bypass mode the input pin is a standard GPIO.The external clock signal has to respect the I/O characteristics in *Section 6.3.12*. However, the recommended clock input waveform is shown in *Figure 20*.

Table 35. High-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	CSS is ON or PLL is used	1	8	32	MHz
		CSS is OFF, PLL not used	0	8	32	MHz
V_{HSEH}	CK_IN input pin high level voltage	-	$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	CK_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSE)}$ $t_{w(HSE)}$	CK_IN high or low time		12	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	CK_IN rise or fall time		-	-	20	
$C_{in(HSE)}$	CK_IN input capacitance		-	2.6	-	pF
$DuCy_{(HSE)}$	Duty cycle		45	-	55	%
I_L	CK_IN Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	µA

1. Guaranteed by design, not tested in production.

Figure 20. High-speed external clock source AC timing diagram



time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

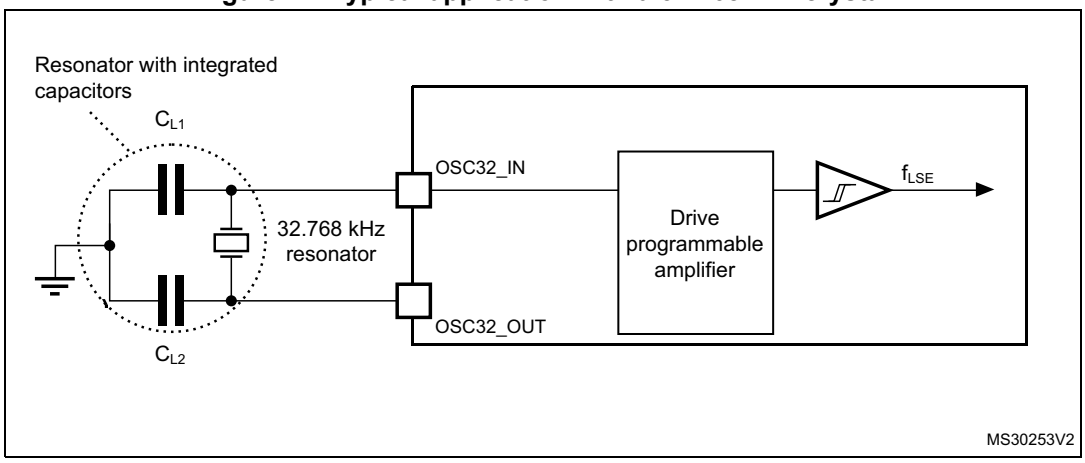
Table 37. LSE oscillator characteristics(1)

Symbol	Parameter	Conditions(2)	Min(2)	Typ	Max	Unit
f_{LSE}	LSE oscillator frequency		-	32.768	-	kHz
G_m	Maximum critical crystal transconductance	LSEDRV[1:0]=00 lower driving capability	-	-	0.5	µA/V
		LSEDRV[1:0]= 01 medium low driving capability	-	-	0.75	
		LSEDRV[1:0] = 10 medium high driving capability	-	-	1.7	
		LSEDRV[1:0]=11 higher driving capability	-	-	2.7	
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized	-	2	-	s

1. Guaranteed by design, not tested in production.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
3. Guaranteed by characterization results, not tested in production. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer. To increase speed, address a lower-drive quartz with a high- driver mode.

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website http://www.st.com.

Figure 22. Typical application with a 32.768 kHz crystal



Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.

Flash memory and data EEPROM

Table 43. Flash memory and data EEPROM characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
V_{DD}	Operating voltage Read / Write / Erase	-	1.65	-	3.6	V
t_{prog}	Programming time for word or half-page	Erasing	-	3.28	3.94	ms
		Programming	-	3.28	3.94	
I_{DD}	Average current during the whole programming / erase operation	T_A = 25 °C, V_{DD} = 3.6 V	-	500	700	µA
	Maximum current (peak) during the whole programming / erase operation		-	1.5	2.5	mA

1. Guaranteed by design, not tested in production.

Table 44. Flash memory and data EEPROM endurance and retention

Symbol	Parameter	Conditions	Value	Unit
			Min(1)	
N_{CYC}(2)	Cycling (erase / write) Program memory	T_A = -40°C to 105 °C	10	kcycles
	Cycling (erase / write) EEPROM data memory		100	
	Cycling (erase / write) Program memory	T_A = -40°C to 125 °C	0.2	
	Cycling (erase / write) EEPROM data memory		2	
t_{RET}(2)	Data retention (program memory) after 10 kcycles at T_A = 85 °C	T_{RET} = +85 °C	30	years
	Data retention (EEPROM data memory) after 100 kcycles at T_A = 85 °C		30	
	Data retention (program memory) after 10 kcycles at T_A = 105 °C	T_{RET} = +105 °C	10	
	Data retention (EEPROM data memory) after 100 kcycles at T_A = 105 °C			
	Data retention (program memory) after 200 cycles at T_A = 125 °C	T_{RET} = +125 °C		
	Data retention (EEPROM data memory) after 2 kcycles at T_A = 125 °C			

1. Guaranteed by characterization results, not tested in production.
2. Characterization is done according to JEDEC JESD22-A117.

6.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 45*. They are based on the EMS levels and classes defined in application note AN1709.

Table 45. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP32, T_A = +25 °C, f_{HCLK} = 32 MHz conforms to IEC 61000-4-2	3B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP32, T_A = +25 °C, f_{HCLK} = 32 MHz conforms to IEC 61000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

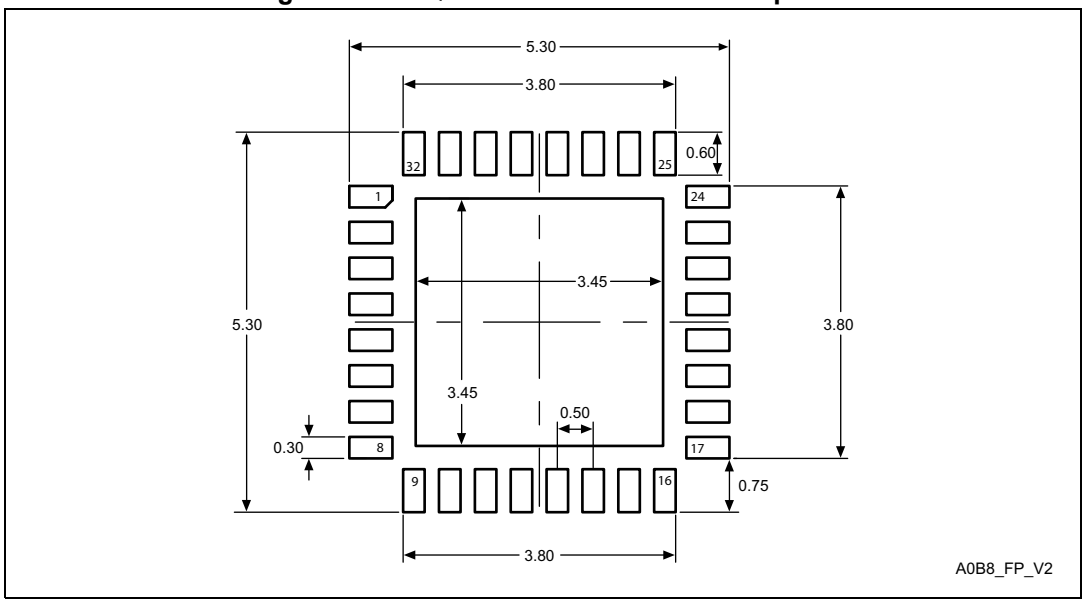
The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the oscillator pins for 1 second.

Figure 37. UFQFPN32 recommended footprint

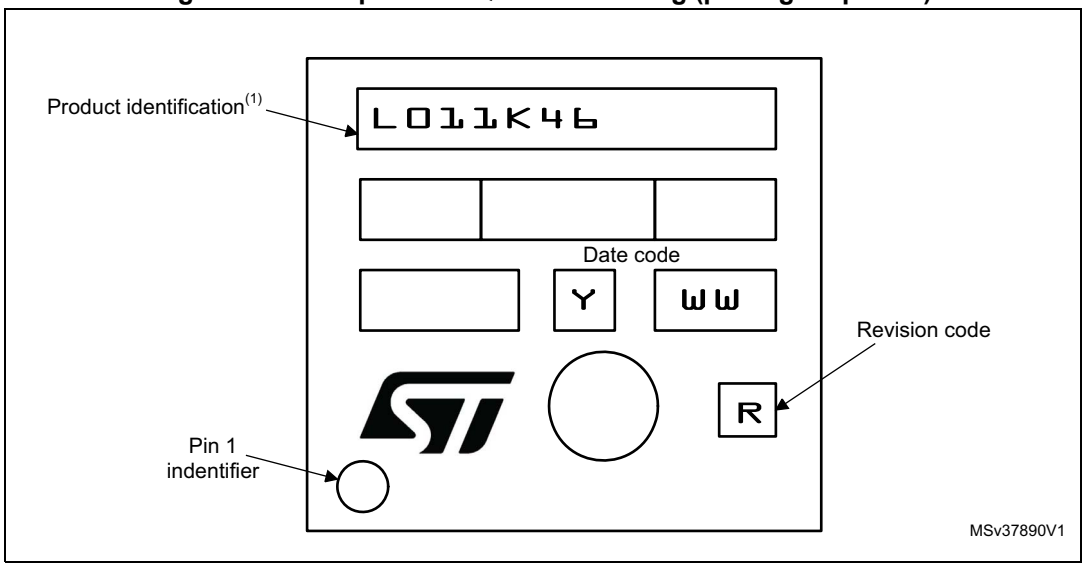


1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking versus pin 1 position identifier location.

Figure 38. Example of UFQFPN32 marking (package top view)

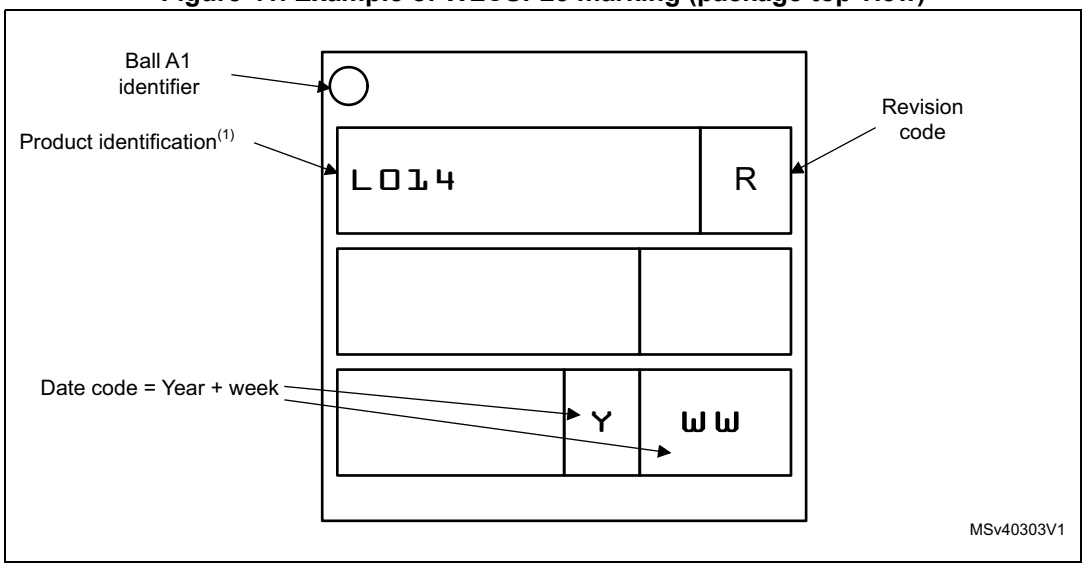


1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Device marking

The following figure gives an example of topside marking versus ball A1 position identifier location.

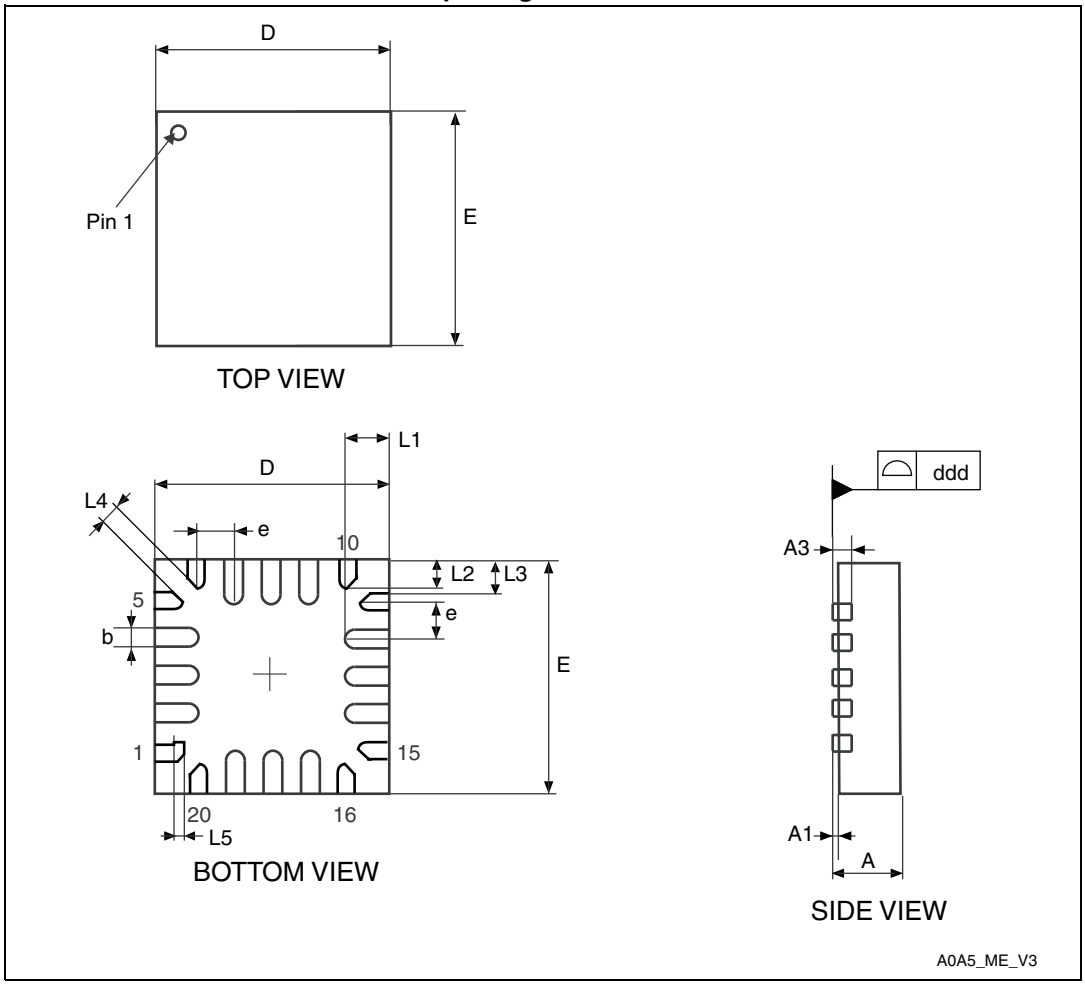
Figure 41. Example of WLCSP25 marking (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

7.5 UFQFPN20 package information

Figure 45. UFQFPN20 - 20-lead, 3x3 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline

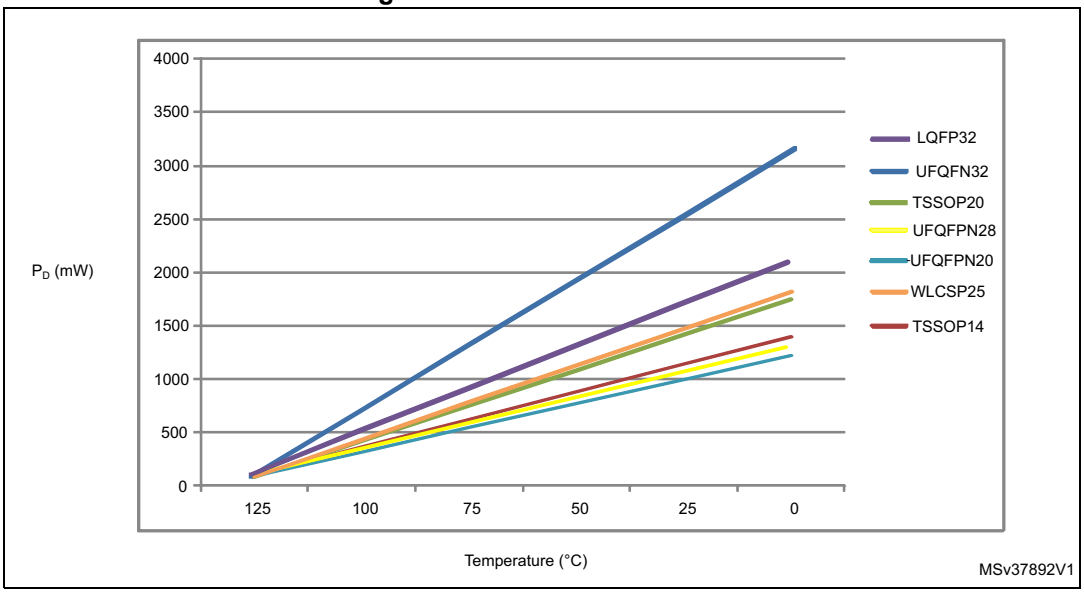


1. Drawing is not to scale.

Table 76. Thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP32 - 7 x 7 mm / 0.8 mm pitch	60	°C/W
	Thermal resistance junction-ambient UFQFPN32 - 5 x 5 mm / 0.5 mm pitch	39	
	Thermal resistance junction-ambient WLCSP25 - 2.133 x 2.070 mm, 0.4 mm pitch	70	
	Thermal resistance junction-ambient UFQFPN28 - 4 x 4 mm, 0.5 mm pitch	97	
	Thermal resistance junction-ambient UFQFPN20 - 3 x 3 mm, 0.5 mm pitch	102	
	Thermal resistance junction-ambient TSSOP20 - 169 mils	74	
	Thermal resistance junction-ambient TSSOP14 - 169 mils	95	

Figure 53. Thermal resistance



1. The above curves are valid for range 3.

7.8.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.