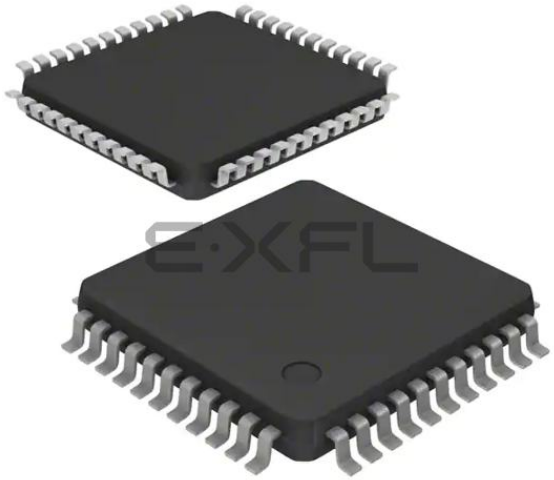
Zilog - Z8F1681AN024XK2246 Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	eZ8
Core Size	8-Bit
Speed	24MHz
Connectivity	DALI, DMX, I²C, LINbus, SPI, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 10x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f1681an024xk2246

1.4.8. Analog Comparators

The analog comparators compare the signal at an input pin or at other internal signal sources with either an internal programmable voltage reference, an internal fixed reference, the DAC output or a second input pin. The comparator outputs are used to either drive an output pin, the Event System, or to generate an interrupt. The comparators can function in all operating modes including Stop Mode.

1.4.9. Temperature Sensor

The temperature sensor produces an analog output proportional to the device temperature. The signal is sent either to the ADC or to the analog comparators. The temperature sensor can function in all operating modes including Stop Mode.

1.4.10. Low-Voltage Detector

The low-voltage detector generates an interrupt when the supply voltage drops below a user-programmable level.

1.4.11. USB 2.0

The Full-Speed Universal Serial Bus (USB 2.0) device provides eight endpoints supporting bulk, control, and interrupt transfers. It contains an integrated USB-PHY and a PLL for transmit clocking.

1.4.12. Enhanced SPI

The enhanced SPI is a full-duplex, buffered, synchronous character-oriented channel which supports a four-wire interface.

1.4.13. UART with LIN, DALI, and DMX

A full-duplex 9-bit UART provides serial, asynchronous communication, and supports the Local Interconnect Network (LIN) and Digital Addressable Lighting Interface (DALI) serial communications protocols as well as Asynchronous Serial Digital Data Transmission Standard for Controlling Lighting Equipment and Accessories (DMX). The UART supports 8-bit and 9-bit data modes, selectable parity, and an efficient bus transceiver Driver Enable signal for controlling a multi-transceiver bus, such as a RS-485. The LIN bus is a cost-efficient, single-master, multiple-slave organization which supports speed up to 20 kilobits. Manchester encoding is supported for the DALI protocol.

1.4.14. Master/Slave I^2C

The inter-integrated circuit (I^2C) controller makes the F6482 Series products compatible with the I^2C protocol. The I^2C controller consists of two bidirectional bus lines:

- Serial data (SDA) line

Table 8. Register File Address Map (Continued)

Address (Hex)	Register Description	Mnemonic	Reset (Hex)	Page #
FAF	DMA 3 Subdata	DMA3SD	00	400
FB0	DMA Control	DMACTL	00	401
Liquid Crystal Display (LCD)				
FB1	LCD Subaddress	LCDSA	00	518
FB2	LCD Subdata	LCDSD	XX	519
FB3	LCD Clock	LCDCLK	00	520
FB4	LCD Control 0	LCDCTL0	00	521
FB5	LCD Control 1	LCDCTL1	00	522
FB6	LCD Control 2	LCDCTL2	00	524
FB7	LCD Control 3	LCDCTL3	00	525
AES				
FB8	AES Data	AESDATA	XX	434
	AES Initialization Vector	AESIV	XX	435
FB9	AES Key	AESKEY	XX	435
FBA	AES Control	AESCTL	00	436
FBB	AES Status	AESSTAT	00	437
PORT J				
FBC	Port J Address	PJADDR	00	86
FBD	Port J Control	PJCTL	00	87
FBE	Port J Input Data	PJIN	XX	94
FBF	Port J Output Data	PJOUT	00	95
Interrupt Controller				
FC0	Interrupt Request 0	IRQ0	00	133
FC1	IRQ0 Enable High Bit	IRQ0ENH	00	137
FC2	IRQ0 Enable Low Bit	IRQ0ENL	00	138
FC3	Interrupt Request 1	IRQ1	00	134
FC4	IRQ1 Enable High Bit	IRQ1ENH	00	139
FC5	IRQ1 Enable Low Bit	IRQ1ENL	00	140
Interrupt Controller (Continued)				
FC6	Interrupt Request 2	IRQ2	00	135
FC7	IRQ2 Enable High Bit	IRQ2ENH	00	141
FC8	IRQ2 Enable Low Bit	IRQ2ENL	00	141

Bit	Description (Continued)
[4] LVD	**Low-Voltage Detection Enable** 0=LVD disabled. 1=LVD enabled (this applies even in Stop Mode).
[3] TEMP	**Temperature Sensor Enable** 0=Temperature Sensor disabled. 1=Temperature Sensor enabled (this applies even in Stop Mode if FRECOV=1).
[2] FRECOV	Fast Recovery 0=Fast Recovery disabled. 1=Fast Recovery enabled. Fast Recovery provides for the shortest Stop-Mode recovery latency at the expense of higher Stop Mode current consumption. See the Reset, Stop-Mode Recovery and Low-Voltage Detection chapter on page 38 to learn more. In addition, this bit must be set for certain peripherals to remain active during Stop Mode as described in this chapter.
[1] COMP0	**Comparator 0 Enable** 0=Comparator 0 is disabled. 1=Comparator 0 is enabled (this applies even in Stop Mode if FRECOV=1).
[0] COMP1	**Comparator 1 Enable** 0=Comparator 1 is disabled). 1=Comparator 1 is enabled (this applies even in Stop Mode if FRECOV=1).

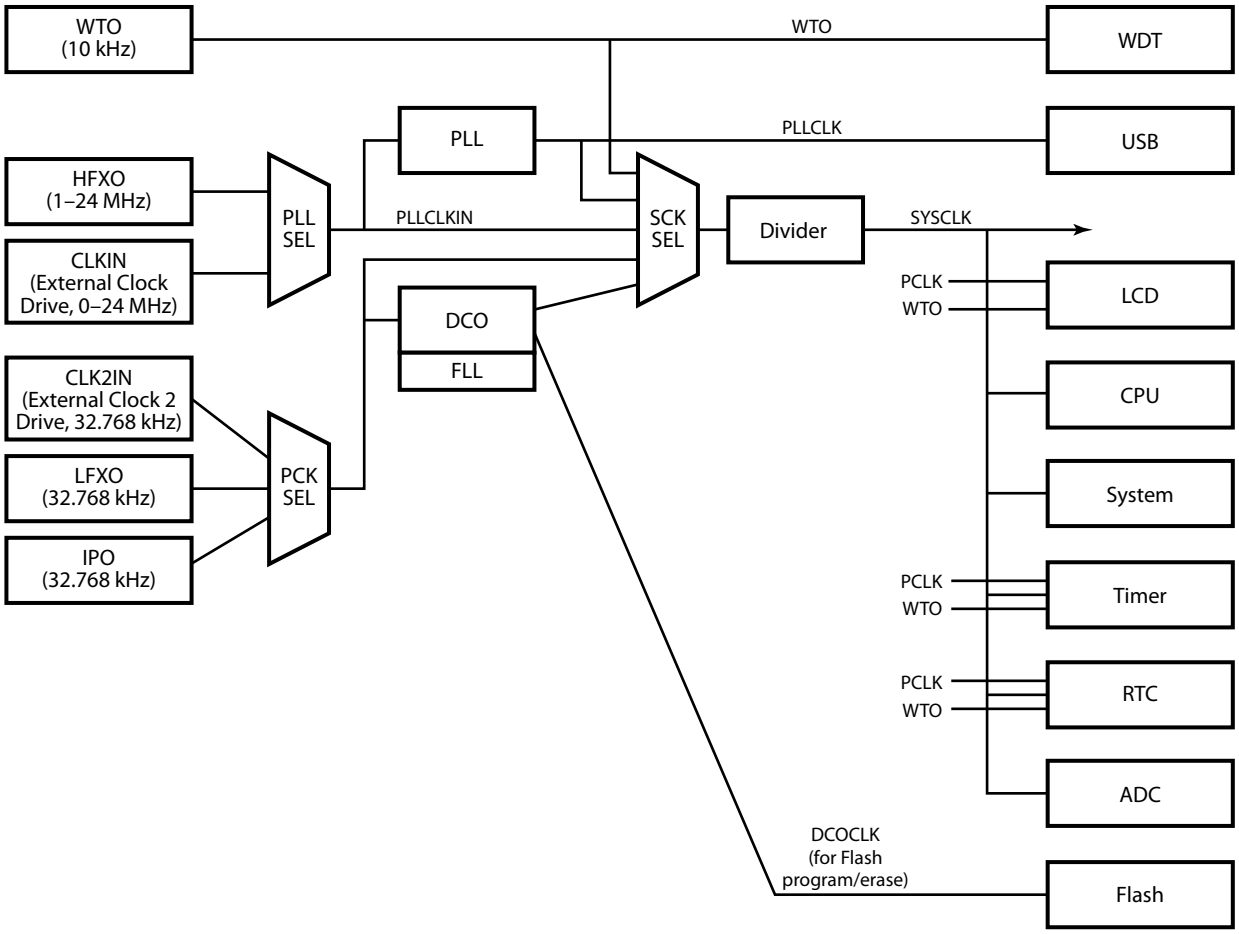

Figure 11. Clock System Block Diagram

8.2. Clock Selection

Clock sources can be selected for System Clock, Peripheral Clock, and PLL Clock.

8.2.1. System Clock Selection

The Clock System selects from the available clock sources. Table 35 details each clock source and its usage.

Bit	Description (Continued)
[3:2] HFXOBAND	**High Frequency Crystal Oscillator (HFXO) Frequency Band** 00: The HFXO or external clock drive is in the 1MHz to 8MHz frequency band. 01: The HFXO or external clock drive is in the > 8MHz to 16MHz frequency band. 10: The HFXO or external clock drive is in the > 16MHz to 24MHz frequency band. 11: Reserved.
[1]	**Reserved** This bit is reserved and must be programmed to 0.
[0] HFXOEN	**High Frequency Crystal Oscillator (HFXO) Enable** 0: HFXO is disabled. 1: HFXO is enabled. In Stop Mode, this bit is overridden such that the HFXO is disabled.

8.11.4. Clock Control 3 Register

The Clock Control 3 (CLKCTL3) Register, shown in Table 41, selects the FLL N-Divider High byte. Before writing CLKCTL3, the clock control registers must be unlocked as described in the Clock System Control Register Unlocking/Locking section on page 103.

Bit	Description (Continued)
[6] CHST	**Channel Status** This bit indicates if a channel Capture/Compare event occurred. This bit is the logical OR of the CHyEF bits in the MCTCHS1 Register. This bit is cleared when TEN=0. 0: No channel capture/compare event has occurred. 1: A channel capture/compare event has occurred. One or more of the CHDEF, CHCEF, CHBEF, and CHAEF bits in the MCTCHS1 Register are set.
[5] TCIEN	**Timer Count Interrupt Enable** This bit enables generation of timer count interrupt. A timer count interrupt is generated whenever the timer completes a count cycle: counting up to Reload Register value or counting down to zero depending on whether the time r mode is Count Modulo or Count up/down. 0: Timer Count Interrupt is disabled. 1: Timer Count Interrupt is enabled.
[4:3]	**Reserved** These bits are reserved and must be programmed to 00.
[2:0] TCLKS	**Timer Clock Source** 000: System Clock (prescaling enabled). 001: Reserved. 010: System Clock gated by active High Timer Input signal (Prescaling enabled). 011: System Clock gated by active Low Timer Input signal (Prescaling enabled). 100: Timer input rising edge (Prescaler disabled). 101: Timer input falling edge (Prescaler disabled). 110: Reserved. 111: Reserved.

Note: The input frequency of the timer input signal must not exceed one-fourth of the system clock frequency.

Chapter 14. UART-LDD

The Local Interconnect Network Universal Asynchronous Receiver/Transmitter (UART-LDD) is a full-duplex communication channel capable of handling asynchronous data transfers in standard UART applications and providing LIN, DALI, and DMX protocol support. The UART-LDD is a superset of the standard F6482 Series MCU UART, providing all of its standard features, LIN/DALI/DMX protocol support and a digital noise filter.

UART-LDD includes the following features:

- 8-bit asynchronous data transfer
- Selectable even- and odd-parity generation and checking
- Option of 1 or 2 stop bits
- Selectable Multiprocessor (9-bit) Mode with three configurable interrupt schemes
- Separate transmit and receive interrupts
- Framing, parity, overrun and break detection
- 16-bit baud rate generator (BRG) which can function as a general-purpose timer with interrupt
- Driver Enable output for external bus transceivers
- LIN protocol support for both Master and Slave modes:
  - Break generation and detection
  - Selectable slave autobaud
  - Check Tx vs. Rx data when sending
- DALI protocol support for both Master and Slave modes:
  - Biphase data encoding
  - Slave address matching
- DMX protocol support for both Master and Slave modes:
  - Slave address matching
  - Automatic break generation
- Configuring a digital-noise filter on the Receive Data line
- DMA support

15.3.3.2. Inter-IC Sound (I^2S) Mode

This mode is selected by setting the SSMD field of the Mode Register to 010. The PHASE and CLKPOL bits of the Control Register must be cleared to 0 and the ESPIEN1 bit must be set=1 (ESPIEN0 can be either 1 or 0). If the ESPI is being used to both send and receive I^2S data, the TDRE interrupt should be serviced before the RDRF interrupt. Figure 41 shows I^2S Mode, with $\overline{SS}$ alternating between consecutive frames. Each audio frame consists of a fixed number of bits, typically a multiple of 8 bits such as 16.

The SSV indicates whether the corresponding bytes are left or right channel data. The SSV value must be updated when servicing the TDRE interrupt/request for the first byte in a left or write channel frame. This update can be made by performing a byte write to update SSV, followed by a byte Write to the Data Register. The $\overline{SS}$ signal will lead the data by one SCK period.

A DMA can be used to transfer audio data, but software must toggle the SSV bit in sync with the first data byte of each left/right channel word.

A transaction is terminated when the master has no more data to transmit. After the last bit is transferred, SCK will stop, and $\overline{SS}$ and SSV will return to their default states. A transmit underrun error will occur at this point.

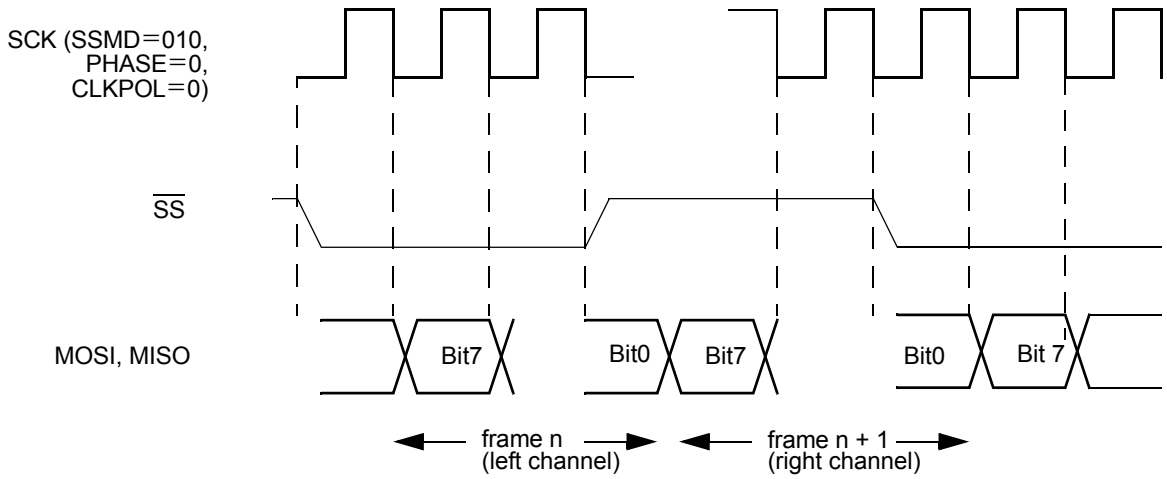

Figure 41. I^2S Mode (SSMD=010), Multiple Frames

15.3.4. SPI Protocol Configuration

This section describes how to configure the ESPI block for the SPI protocol. In the SPI protocol, the master sources the SCK and asserts Slave Select signals to one or more slaves. The Slave Select signals are typically active Low.

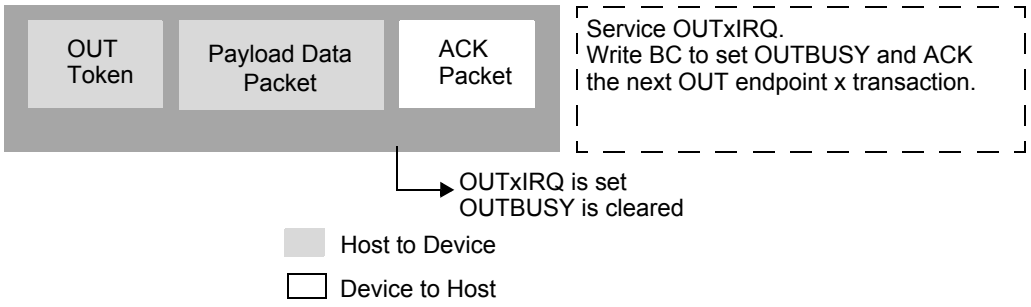

Figure 59. Bulk OUT Transfer Example

Table 168. USB Module Response to Host upon Receiving an OUT Token

Error in OUT Token	OUTBUSY	OUTSTALL	USB Module Response to Host
No	0	0	NAK
No	0	1	STALL
No	1	0	ACK
No	1	1	STALL
Yes	–	–	No Response

17.2.5.3. Function Address

The USB Module copies the function address which was sent by the host into the USB Function Address Subregister (FNADDR). Upon reset, the USB Module function address is cleared to be the default address of 00h, and this address is used until completing a SET_ADDRESS request from the host. The USB Module responds only when the packet function address matches the function address assigned to the USB Module.

17.2.6. Endpoint Pairing

Endpoints 2 and 3 may be paired to allow double buffering. When pairing is enabled, software may access one endpoint memory buffer of the pair while the USB host accesses the other buffer via the USB Module.

IN endpoints 2 and 3 are paired by setting PRIN23 in the USBPAIR Subregister. When IN endpoints 2 and 3 are paired, the IN endpoint 2 subregisters govern control of the paired endpoints; software should access only the IN endpoint 2 buffer space. The USB Module manages readdressing, as required, to utilize the IN endpoint 3 buffer space. Software is not required to configure the IN endpoint 3 control bits and registers. When paired, soft-

17.3.9. USB IN Endpoint 1–3 Start Address Subregisters

The USB IN Endpoint 1–3 Start Address subregisters, shown in Table 178, in conjunction with the USBISTADDR Register shown in Table 177 and the USBISPADDR Register shown in Table 200 on page 387, define the size of each IN endpoint.

Table 178. USB IN Endpoint 1–3 Start Address Subregisters (USBIxADDR)

Bit	7	6	5	4	3	2	1	0
Field	INADDR							
Reset	see description below							
R/W	R0/W*	R0/W*	R0/W*	R0/W*	R0/W*	R0/W*	R0/W*	R0/W*
Address	If USBSA = 09h, 0Ah, 0Bh in the USB Subaddress Register, accessible through the USB Subdata Register							

Note: *R0/W = Write, but reads back as 0.

Bit	Description
[7:0] INADDR	IN Endpoint Start Address 00–FF: The start address of IN endpoint memory buffers except IN endpoint 0. The first starting address (IN endpoint 0) is configured in the USBISTADDR Register. INSTADDR + {0, INADDR[7:0], 0} maps to endpoint buffer memory address [9:0], therefore the minimum increment of INADDR is 2 bytes of buffer memory. The size in bytes of an IN endpoint is determined by subtracting consecutive starting address values then multiplying by 2. INADDR should be set to 00h for any IN endpoint that doesn't exist (or is not used). See the USB Endpoint Buffer Memory section on page 341 for details. **Reset State:** USBI1ADDR: 20h USBI2ADDR: 40h USBI3ADDR: 60h

17.3.21. USB OUT 0–3 Byte Count Subregisters

The USB OUT 0–3 Byte Count subregisters, shown in Table 190, contain the USB OUT endpoint byte counts.

Table 190. USB OUT 0–3 Byte Count Subregisters (USBOxBC)

Bit	7	6	5	4	3	2	1	0
Field	Reserved	BC						
Reset	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R
Address	If USBSA = 45h, 47h, 49h, 4Bh in the USB Subaddress Register, accessible through the USB Subdata Register							

Bit	Description
[7]	**Reserved** This bit is reserved and must be programmed to 0.
[6:0] BC	**OUT Byte Count** 00–40: BC contains the number of bytes sent during the last OUT transfer from the host to the OUT endpoint x. 41-7F: Reserved.

17.3.27. USB Endpoint Pairing Subregister

The USB Endpoint Paring Subregister, shown in Table 197, controls pairing of USB endpoints.

Table 197. USB Endpoint Pairing Subregister (USBPAIR)

Bit	7	6	5	4	3	2	1	0
Field	Reserved				PROUT23	Reserved		PRIN23
Reset	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R/W	R	R	R/W
Address	If USBSA = 5Dh in the USB Subaddress Register, accessible through the USB Subdata Register							

Bit	Description
[7:4]	**Reserved** These bits are reserved and must be programmed to 0000.
[3] PROUT23	**OUT 2 and OUT 3 Pairing** 0: OUT 2 and OUT 3 are not paired. 1: OUT 2 and OUT 3 are paired.
[2:1]	**Reserved** These bits are reserved and must be programmed to 00.
[0] PRIN23	**IN 2 and IN 3 Pairing** 0: IN 2 and IN 3 are not paired. 1: IN 2 and IN 3 are paired.

18.2.8.1. Linked List Descriptor Request Priority

Because a linked list descriptor fetch has the highest priority, other DMA requests are ignored while a descriptor is being transferred from the Register File to the DMA registers.

18.2.8.2. Round Robin Priority

Round-robin priority is the default at System Reset, and is selected by clearing the PRIORITY bit. With round-robin priority, each channel request is serviced for the length of its burst size or until it deasserts a DMA request, whichever occurs first. After a channel is serviced, it is assigned lowest priority and is taken out of the rotation until all other requesting channels are serviced.

18.2.8.3. Fixed Priority

Fixed priority is selected by setting the PRIORITY bit. With fixed priority, channel requests are serviced with the following priority order from highest to lowest: DMA0, DMA1, DMA2, DMA3. Lower-priority DMA channels are not serviced until higher-priority DMA channels deassert DMA request.

18.2.9. Interrupts

Independent interrupt control is provided for end-of-count and watermark interrupts. An indication of whether the most recent interrupt was due to an end-of-count or watermark is provided by the IRQS bit in the DMA 0–3 Subregister Selection and Status registers.

18.2.10. End-of-Count Interrupt

An interrupt is generated when the end-of-count is reached. If interrupted on an end-of-count, the EOCIRQE bit is set in the DMAxCTL0 Subregister. The EOCIRQE bit can be cleared if the application is not required to service the buffer, or will service the buffer in conjunction with a future buffer.

18.2.11. Watermark Interrupt

The DMA Controller is able to generate an interrupt prior to an end-of-count being reached. If the value of the WMCNT bit in the DMAxCNTH Subregister matches the current count, {CNTH, CNTL}, in the DMAxCNTH and DMAxCNTL subregisters, a watermark interrupt will be generated. To disable watermark interrupts, configure WMCNT=0h.

Only a single watermark interrupt will be generated for a given count value.

20.2.4. AES Output Feedback (OFB) Mode

The following subsections describe AES OFB Mode.

20.2.4.1. AES CBC Mode Description

AES OFB Mode is selected by configuring MODE=01 in the AES Control Register. To encrypt in this mode, the AES accelerator uses the encryption key to operate on the previous AES accelerator output which is then XORed with plain text to generate cipher text. Because the previous AES accelerator output is not available for the first operation, an Initialization Vector is utilized instead. An OFB encryption flow diagram is shown in Figure 66 and an OFB encryption example is provided in the OFB Mode Encryption Example section on page 430.

To decrypt in this mode, the AES accelerator uses the decryption key to operate on the previous AES accelerator output which is then XORed with cipher text to generate plain text. Because the previous AES accelerator output is not available for the first operation, an Initialization Vector is utilized instead. Both encryption and decryption for OFB Mode require the AES accelerator to be set to encrypt (DECRYPT=0). An OFB encryption flow diagram is shown in Figure 67.

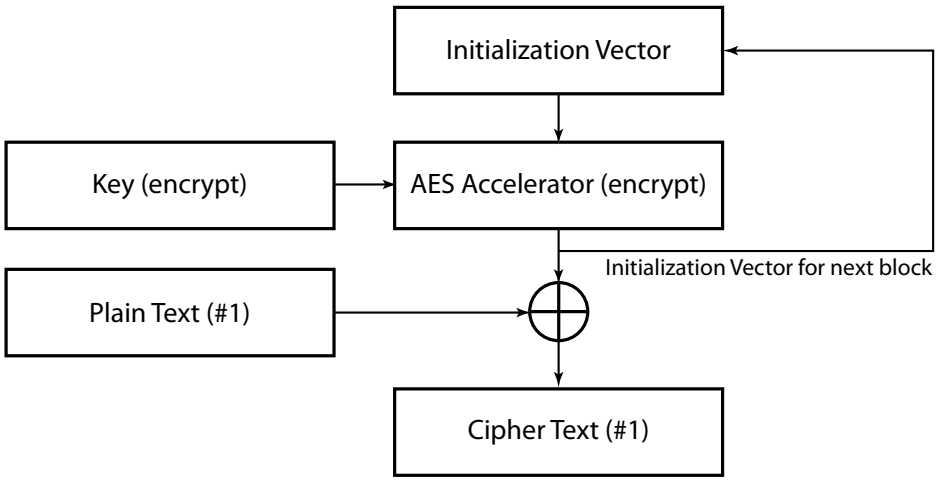

Figure 66. OFB Mode Encryption Flow Diagram

Chapter 21. Analog-to-Digital Converter

The F6482 Series MCUs include a seventeen-channel Successive Approximation Register Analog-to-Digital Converter (SAR ADC). This ADC converts an analog input signal to a 12-bit or 14-bit binary number, and includes the following additional features:

- 12-bit or 2-pass 14-bit resolution
- Twelve analog input sources multiplexed with general-purpose I/O ports
- Five internal analog input sources including: Op Amp A output, Op Amp B output, temperature sensor, bandgap, and $A_{VDD}/2$ fixed reference
- Four input modes: two single-ended modes, balanced differential mode, and unbalanced differential mode
- Conversion initiated by software or Event System input
- Channel scanning function
- Optional conversion averaging of 2, 4, 8, 16 samples
- Continuous conversion function that can be used with or without channel sequencing
- DMA support
- Fast conversion time, as low as 3µs
- Programmable timing controls including ADC clock prescaler
- Window check function
- Interrupt on conversion complete or outside window
- Internal voltage reference selections of A_{VDD} or buffered VBIAS from the Reference System (2.5V, 2.0V, 1.5V, 1.25V)
- Buffered VBIAS internal reference voltage can be driven externally on $V_{REF}+$
- Ability to utilize external reference voltage
- In-situ calibration for all operating modes
- Auto-disable
- Two power settings

21.1. Architecture

The ADC can be operated with either single-ended inputs or differential inputs. The architecture, shown in Figure 70, consists of input multiplexers, sample-and-hold, an internal

available current levels of 10µA, 100µA, and 1mA, respectively. The 1mA level is not recommended for AVDD < 3V. When using an external resistor, R_{EXT}, and a Programmable Reference 1 level of 0.3125V, the current will be 0.3125V ÷ R_{EXT}. The current should not exceed 1.2mA, and the Programmable Reference 1 level should not exceed A_{VDD} − 1V.

The current levels provided by the internal resistors differ by 10x, which can be convenient for applications such as temperature diode measurement. By taking two voltage measurements at 10x different currents, the absolute temperature is directly proportional to the difference in the sensed diode voltages and natural log of the current ratio (10:1). This application (force current and sense voltage) can be accomplished with only one package pin if sensing with the ADC or, alternatively, with two package pins when sensing with Op Amp A.

The current drive network is connected to AMPBOUT by selecting the appropriate GPIO alternate function and writing OUTCTL=01 for the current source, or OUTCTL=10 for the current sink.

23.3. Op Amp Register Definitions

The four op amp registers are briefly summarized in Table 251; their bits are defined in Tables 252 through 255.

Table 251. Op Amp Register Summary

Name	Address	Description
AMPACTL0	F94h	Configuration for Op Amp A
AMPACTL1	F95h	Programmable Gain & Configuration for Op Amp A
AMPBCTL0	F96h	Configuration for Op Amp B
AMPBCTL1	F97h	Source/Sink Current & Configuration for Op Amp B

23.3.1. Op Amp A Control 0 Register

The Op Amp A Control 0 Register, shown in Table 252, contains configuration for Op Amp A.

BIASGSEL bit in the LCDCTL1 Register. When the high transition bias drive is selected (BIASGSEL=1), the internal charge pump output current capacity is also increased.

The high drive biasing duration is selected using the HBDDUR bit in the LCDCTL1 Register. See the Electrical Characteristics chapter on page 598 to learn more about bias generator current consumption and the bias drive.

26.2.6.3. V_{LCD} and Bias Generator Source Selection

LCD bias generator source options include the internal charge pump, V_{DD} connected internally, and an external supply. As shown in Table 264, V_{LCD} source selection is determined by the CPEN bit in the LCDCTL1 Register and the VLCDDIR bit in the LCDCTL3 Register. When the LCD Controller is disabled by clearing the LCD bit in the PWRCTL0 Register, V_{LCD} is not driven, and no bias generator sources are connected to the bias generator.

Table 264. V_{LCD} and Bias Generator Source Selection

Control Settings			Selected Functionality		
LCD (PWRCTL0)	VLCDDIR (LCDCTL3)	CPEN (LCDCTL1)	V_{LCD} Connection	Bias Generator Source	Charge Pump State
1	1	0	No connect	V_{DD}	OFF
1	1	1	Bias generator & internal charge pump	Internal charge pump	ON
1	0	0	Bias generator & external supply	External supply	OFF
1	0	1	Bias generator*	No connect	OFF
0	x	x	No connect	No connect	OFF

Note: *Typically not selected, because the bias generator resistive network will discharge V_{LCD}.

26.2.7. LCD Outputs

Selecting LCD Controller outputs to drive the GPIO pins is a GPIO alternate function selection. See the General-Purpose Input/Output chapter on page 55 to learn more about selecting LCD outputs.

26.2.8. Waveform Generation

To enable waveform generation, set the WGENEN bit in the LCDCTL3 Register. The following sections describe waveform generation. The waveform characteristics, as summarized in Table 265, are selected with the LCDMODE bit in the LCTCTL2 Register.

30.2. Operation

This section describes the OCD interface and its operation in debug and high-speed synchronous modes as well as baud rates, OCD data formats, resets, breakpoints and flow control.

30.2.1. On-Chip Debugger Interface

The On-Chip Debugger (OCD) uses the DBG pin for communication with an external host. This one-pin interface is a bidirectional open-drain interface that transmits and receives data. Data transmission is half-duplex, in that transmit and receive cannot occur simultaneously. The serial data on the DBG pin is sent using the standard asynchronous data format defined in RS-232. This pin interfaces the F6482 Series device to the serial port of a host PC using minimal external hardware. Figure 97 shows the connections between the debug connector and the Z8 Encore! microcontroller. Two different methods for connecting the DBG pin to an RS-232 interface are depicted in Figures 98 and 99.

Figure 97. Target OCD Connector Interface

```
DBG ← Size[7:0]
DBG ← 1–256 data bytes
```

Read Register (09h). The Read Register command reads data from the Register File. Data can be read 1–256 bytes at a time (256 bytes can be read by setting *size* to zero). If the device is not in Debug Mode, or if the Read Protect option bit is enabled and on-chip RAM is being read from, this command returns FFh for all of the data values.

```
DBG ← 09h
DBG ← {0h,Register Address[11:8]
DBG ← Register Address[7:0]
DBG ← Size[7:0]
DBG → 1–256 data bytes
```

Write Program Memory (0Ah). The Write Program Memory command writes data to Program Memory. This command is equivalent to the LDC and LDCI instructions. Data can be written 1–65536 bytes at a time (65536 bytes can be written by setting size to 0). The on-chip Flash Controller must be written and unlocked for the programming operation to occur. If the Flash Controller is not unlocked, the data is discarded. If the device is not in Debug Mode, or if the Read Protect option bit is enabled, the data is discarded.

```
DBG ← 0Ah
DBG ← Program Memory Address[15:8]
DBG ← Program Memory Address[7:0]
DBG ← Size[15:8]
DBG ← Size[7:0]
DBG ← 1–65536 data bytes
```

Read Program Memory (0Bh). The Read Program Memory command reads data from Program Memory. This command is equivalent to the LDC and LDCI instructions. Data can be read 1–65536 bytes at a time (65536 bytes can be read by setting *size* to 0). If the device is not in Debug Mode or if the Read Protect option bit is enabled, this command returns FFh for the data.

```
DBG ← 0Bh
DBG ← Program Memory Address[15:8]
DBG ← Program Memory Address[7:0]
DBG ← Size[15:8]
DBG ← Size[7:0]
DBG → 1–65536 data bytes
```

Write Data Memory (0Ch). The Write Data Memory command writes data to Data Memory. This command is equivalent to the LDE and LDEI instructions. Data is written 1–65536 bytes at a time (65536 bytes can be written by setting *size* to 0). If the device is not in Debug Mode, or if the Read Protect option bit is enabled, the data is discarded.

```
DBG ← 0Ch
DBG ← Data Memory Address[15:8]
```

Figure 111 and Table 355 provide timing information for the UART pins for situations in which CTS is not used for flow control. DE asserts after the Transmit Data Register has been written. DE remains asserted for multiple characters as long as the Transmit Data Register is written with the next character before the current character has completed.

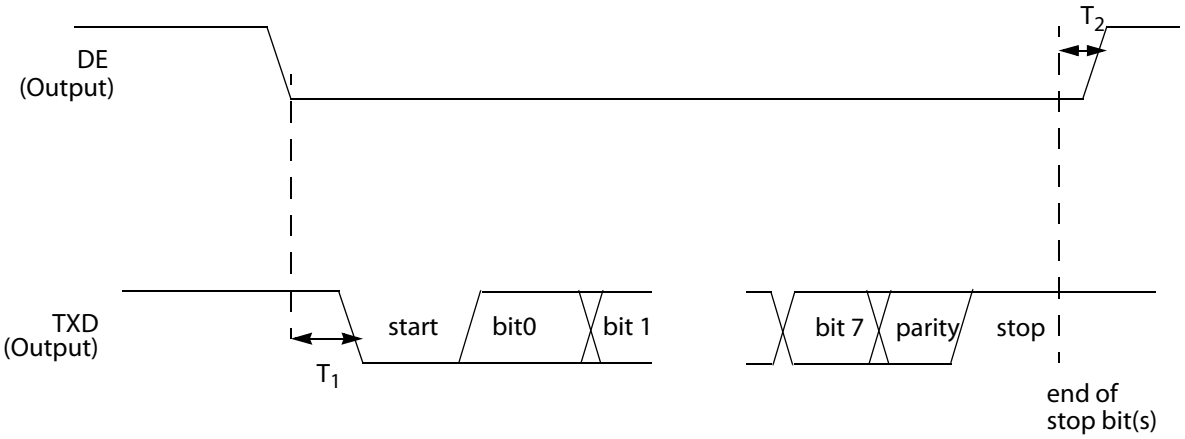

Figure 111. UART Timing Without CTS

Table 355. UART Timing Without CTS

		Delay (ns)	
Parameter	**Abbreviation**	**Min**	**Max**
T_1	DE assertion to TXD falling edge (start bit) delay	1 * SYSCLK period	1 bit time
T_2	End of Stop Bit(s) to DE deassertion delay (Tx Data Register is empty)	± 5	