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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	eZ8
Core Size	8-Bit
Speed	24MHz
Connectivity	DALI, DMX, I²C, LINbus, SPI, UART/USART, USB
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	67
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3.75K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 12x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f3282at024xk

Bit	Description (Continued)
[4] LVD	**Low-Voltage Detection Enable** 0=LVD disabled. 1=LVD enabled (this applies even in Stop Mode).
[3] TEMP	**Temperature Sensor Enable** 0=Temperature Sensor disabled. 1=Temperature Sensor enabled (this applies even in Stop Mode if FRECOV=1).
[2] FRECOV	Fast Recovery 0=Fast Recovery disabled. 1=Fast Recovery enabled. Fast Recovery provides for the shortest Stop-Mode recovery latency at the expense of higher Stop Mode current consumption. See the Reset, Stop-Mode Recovery and Low-Voltage Detection chapter on page 38 to learn more. In addition, this bit must be set for certain peripherals to remain active during Stop Mode as described in this chapter.
[1] COMP0	**Comparator 0 Enable** 0=Comparator 0 is disabled. 1=Comparator 0 is enabled (this applies even in Stop Mode if FRECOV=1).
[0] COMP1	**Comparator 1 Enable** 0=Comparator 1 is disabled). 1=Comparator 1 is enabled (this applies even in Stop Mode if FRECOV=1).

Table 19. Port Alternate Function Mapping (Z8Fxx81 64-Pin Parts) (Continued)

Port	Pin	Mnemonic	Alternate Function Description	Alternate Function Set Subregisters
Port C[2] (cont'd.)	PC6	T2IN/$\overline{\text{T2OUT}}$	Timer 2 Input/Timer2 Output Complement	AFS1[6]: 0, AFS2[6]: 0
		SCKOUT	System Clock Out	AFS1[6]: 1, AFS2[6]: 0
		ESOUT[0]	Event System Output 0	AFS1[6]: 0, AFS2[6]: 1
		Reserved		AFS1[6]: 1, AFS2[6]: 1
	PC7	T2OUT	Timer 2 Output	AFS1[7]: 0, AFS2[7]: 0
		$\overline{\text{CTS1}}$	UART 1 Clear to Send	AFS1[7]: 1, AFS2[7]: 0
		ESOUT[1]	Event System Output 1	AFS1[7]: 0, AFS2[7]: 1
		Reserved		AFS1[7]: 1, AFS2[7]: 1
Port D[1]	PD0	$\overline{\text{RESET}}$	External Reset	AFS1[0]: 0
		Reserved		AFS1[0]: 1
	PD1	C1INN	Comparator 1 Input (N)	AFS1[1]: 0
		ANA7/AMPBINN	ADC Analog Input/OpAmp B Input (N)	AFS1[1]: 1
	PD2	C1INP	Comparator 1 Input (P)	AFS1[2]: 0
		ANA6/AMPBINP	ADC Analog Input/OpAmp B Input (P)	AFS1[2]: 1
	PD3	C1OUT	Comparator 1 Output	AFS1[3]: 0
		ANA8/AMPBOUT	ADC Analog Input/OpAmp B Output	AFS1[3]: 1
	PD4	RXD1	UART 1 Receive Data	AFS1[4]: 0
		Reserved		AFS1[4]: 1
	PD5	TXD1	UART 1 Transmit Data	AFS1[5]: 0
		Reserved		AFS1[5]: 1
	PD6	DE1	UART 1 Driver Enable	AFS1[6]: 0
		Reserved		AFS1[6]: 1
	PD7	C0OUT	Comparator 0 Output	AFS1[7]: 0
		Reserved		AFS1[7]: 1

Notes
1. Because there are at most two choices of alternate function for some pins of Ports A, B, D, E and F, the Alternate Function Set register AFS2 is not implemented. Additionally, alternate function selection, as described in the Port A–J Alternate Function Subregisters (see page 88), must also be enabled.
2. The alternate function selection for Port C, as described in the Port A–J Alternate Function Subregisters (see page 88), must also be enabled.

Table 20. Port Alternate Function Mapping (Z8Fxx82 64-Pin Parts) (Continued)

Port	Pin	Mnemonic	Alternate Function Description	Alternate Function Set Subregisters
Port F[1]	PF0	ESOUT[0]	Event System Out 0	AFS1[0]: 0
		SEG2	LCD Segment	AFS1[0]: 1
	PF1	ESOUT[1]	Event System Out 1	AFS1[1]: 0
		SEG7	LCD Segment	AFS1[1]: 1
	PF2	ESOUT[2]	Event System Out 2	AFS1[2]: 0
		SEG8	LCD Segment	AFS1[2]: 1
	PF3	ESOUT[3]	Event System Out 3	AFS1[3]: 0
		SEG9	LCD Segment	AFS1[3]: 1
	PF4	Reserved		AFS1[4]: 0
		SEG10	LCD Segment	AFS1[4]: 1
	PF5	Reserved		AFS1[5]: 0
		SEG15	LCD Segment	AFS1[5]: 1
	PF6	$\overline{SS1}$	SPI 1 Slave Select	AFS1[6]: 0
		SEG20	LCD Segment	AFS1[6]: 1
	PF7	MISO1	SPI 1 Master In Slave Out	AFS1[7]: 0
		SEG23	LCD Segment	AFS1[7]: 1

Notes
1. Because there are at most two choices of alternate function for some pins of Ports A, B, D, F, G and H, the Alternate Function Set register AFS2 is not implemented. Additionally, alternate function selection, as described in the Port A–J Alternate Function Subregisters (see page 88), must also be enabled.
2. The alternate function selection for Port C, as described in the Port A–J Alternate Function Subregisters (see page 88), must also be enabled.
3. Because there is only a single alternate function for each Port J pin, the Alternate Function Set registers are not implemented for Port J. Additionally, alternate function selection, as described in the Port A–J Alternate Function Subregisters (see page 88), must also be enabled.

System Clock. The WTO is enabled automatically to allow the recovery. Although this oscillator runs at a much slower speed than the original system clock, the CPU continues to operate allowing execution of a clock failure vector and software routines that either remedy the oscillator failure or issue a failure alert. This automatic switch-over is not available if WTO is the System Clock source.

The System Clock source failure detection circuitry asserts if the System Clock frequency drops below 1 kHz ±50%. If an external signal is selected as the System Clock source, it is possible that a very slow but nonfailing clock can generate a failure condition. Under these conditions, do not enable the System Clock failure circuitry (SCKFEN should be cleared).

8.3.2. Watchdog Timer Failure

In the event of a Watchdog Timer Oscillator (WTO) failure, a similar nonmaskable interrupt-like event is issued. This event does not trigger an attendant clock switch-over, but alerts the CPU of the failure. After a Watchdog Timer failure, it is no longer possible to detect a System Clock failure. The failure detection circuitry does not function if the Watchdog Timer is used as the System Clock. In this case, it is necessary to disable the detection circuitry by clearing WTOFEN.

The WTO failure-detection circuit counts system clocks while looking for a Watchdog Timer clock. The logic counts 8004 system clock cycles before determining that a failure has occurred. The system clock rate determines the speed at which the Watchdog Timer failure can be detected. A very slow system clock results in very slow detection times.

8.4. High Frequency Crystal Oscillator

The products in the F6482 Series contain an on-chip High Frequency Crystal Oscillator (HFXO) for use with external crystals with 1 MHz to 24 MHz frequencies. HFXO features include:

- Optimized for low current consumption
- Selectable as System Clock
- Selectable as the PLL reference clock, which in turn, can generate System Clock and/or generate clocking for the USB

Alternatively, the X_{IN} input pin can also accept a 1 MHz–24MHz CMOS-level clock input signal. If an external clock generator is used, the X_{OUT} pin must be left unconnected.

Note: Although the X_{IN} pin can be used as an main system clock input for an external clock generator, configuring PA0 as CLKIN is better suited for such use. To learn more, see the System Clock Selection section on page 98).

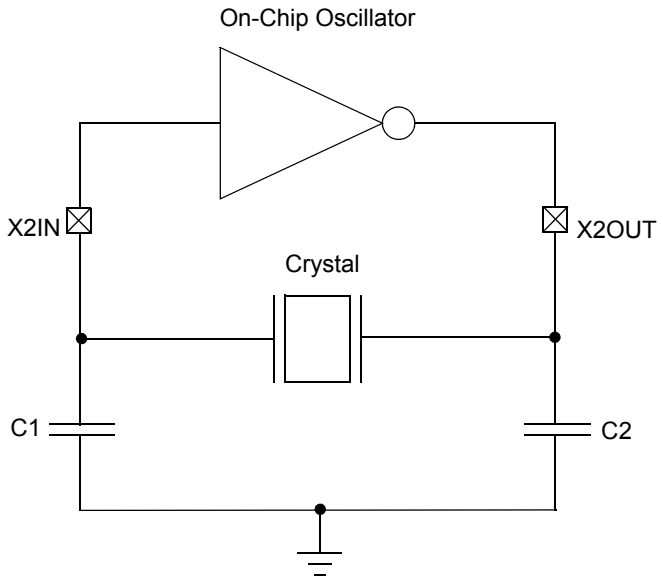

Figure 13. Recommended 32.768 kHz Crystal Oscillator Configuration

8.6. Internal Precision Oscillator

The Internal Precision Oscillator (IPO) can be selected as PCLK and is designed for use without external components. IPO features include:

- On-chip RC oscillator that does not require external components
- Elimination of crystals in applications for which high timing accuracy is not required
- 32.768 kHz nominal frequency
- Accuracy: ± 2% over operational temperature and voltage range

8.6.1. Operation

IPOEN in the CLKCTL1 Register controls whether the IPO is enabled. During System Reset, IPOEN is set, enabling the IPO. If the IPO is disabled, user code can set IPOEN to enable the IPO, it should also check that the IPO is stable, by reading IPORDY, before selecting the IPO as PCLK.

The IPO is an RC relaxation oscillator that offers low sensitivity to power supply and temperature variation. At System Reset, the IPO is enabled and selected as PCLK which, in turn, is selected as input to the FLL. If the IPO is not required, it can be disabled by clearing IPOEN in CLKCTL1 to reduce system power consumption.

10.1.3. Timer 0–2 PWM0 High and Low Byte Registers

The Timer 0–2 PWM0 High and Low Byte (T*x*PWM0H and T*x*PWM0L) registers, shown in Tables 79 and 80, are used for Pulse Width Modulator (PWM) operations. These registers also store the Capture values for the Capture, Capture/Compare and Demodulation modes. When the timer is enabled, writes to these registers are buffered, and loading of the registers is delayed until a timer reload to 0001h occurs; i.e., unless PWM0UE=1.

Table 79. Timer 0–2 PWM0 High Byte Registers (T*x*PWM0H)

Bit	7	6	5	4	3	2	1	0
Field	PWM0H							
Reset	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	T0PWM0H @ F04h, T1PWM0H @ F0Ch, T2PWM0H @ F14h							
Note: *x* references bits in the range [2:0].								

Table 80. Timer 0–2 PWM0 Low Byte Registers (T*x*PWM0L)

Bit	7	6	5	4	3	2	1	0
Field	PWM0L							
Reset	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	T0PWM0L @ F05h, T1PWM0L @ F0Dh, T2PWM0L @ F15h							
Note: *x* references bits in the range [2:0].								

Bit	Description
[7:0] PWM0H, PWM0L	**Pulse Width Modulator 0 High and Low Bytes** These two bytes, {PWM0H[7:0], PWM0L[7:0]}, form a 16-bit value that is compared to the current 16-bit timer count. When a match occurs, the PWM output changes state. The PWM output value is set by the TPOL bit in the Timer Control 1 Register (T*x*CTL1). The T*x*PWM0H and T*x*PWM0L registers also store the 16-bit captured timer value when operating in Capture, Capture/Compare and Demodulation modes.

b. If Multiprocessor Mode is not enabled, then enable parity if appropriate and select either even or odd parity.
c. Set or clear the CTSE bit to enable or disable control from the remote receiver via the $\overline{CTS}$ pin.

8. Execute an EI instruction to enable interrupts.

The UART-LDD is now configured for interrupt-driven data transmission. Because the UART-LDD Transmit Data Register is empty, an interrupt is generated immediately. When the UART-LDD Transmit interrupt is detected and there is transmit data ready to send, the associated interrupt service routine (ISR) performs the following:

1. If in Multiprocessor Mode, writes to the UART-LDD Control 1 Register to select the outgoing address bit:
   – Sets the Multiprocessor Bit Transmitter (MPBT) if sending an address byte, clears it if sending a data byte.
2. Writes the data byte to the UART-LDD Transmit Data Register. The transmitter automatically transfers the data to the Transmit Shift Register and transmits the data.
3. Executes the IRET instruction to return from the interrupt-service routine and wait for the Transmit Data Register to again become empty.

If a transmit interrupt occurs and there is no transmit data ready to send, the interrupt service routine executes the IRET instruction. When the application does have data to transmit, software can set the appropriate interrupt request bit in the Interrupt Controller to initiate a new transmit interrupt. Another alternative would be for the software to write the data to the Transmit Data Register instead of invoking the interrupt service routine.

14.1.4. Receiving Data Using Polled Method

Observe the following steps to configure the UART-LDD for polled data reception:

1. Write to the UART-LDD Baud Rate High and Low Byte registers to set the appropriate baud rate.
2. Enable the UART-LDD pin functions by configuring the associated GPIO port pins for alternate function operation.
3. If Multiprocessor Mode is appropriate, write to the UART-LDD Control 1 Register to enable Multiprocessor (9-bit) Mode functions.
4. Write to the UART-LDD Control 0 Register to:
   a. Set the Receive Enable (REN) bit to enable the UART-LDD for data reception.

6. The I2C controller receives the first byte and responds with Acknowledge or Not Acknowledge, depending on the state of the NAK bit in the I2CCTL Register. The I2C controller generates the receive data interrupt by setting the RDRF bit in the I2CISTAT Register.
7. The software responds by reading the I2CISTAT Register, finding the RDRF bit=1 and then reading the I2CDATA Register, which clears the RDRF bit. If the software can accept only one more data byte, it sets the NAK bit in the I2CCTL Register.
8. The master and slave loops through Step 5 to Step 7 until the master detects a Not Acknowledge instruction or runs out of data to send.
9. The master sends the stop or restart signal on the bus. Either of these signals can cause the I2C controller to assert the stop interrupt (the stop bit=1 in the I2CISTAT Register). Because the slave received data from the master, the software takes no action in response to the stop interrupt other than reading the I2CISTAT Register to clear the stop bit.

16.2.6.7. Slave Transmit Transaction With 7-Bit Address

The data transfer format for a master reading data from a slave in 7-bit address mode is shown in Figure 52. The procedure that follows describes the I2C Master/Slave Controller operating as a slave in 7-bit addressing mode and transmitting data to the bus master.

S	Slave Address	R=1	A	Data	A	Data	$\overline{A}$	P/S

Figure 52. Data Transfer Format, Slave Transmit Transaction with 7-bit Address

1. The software configures the controller for operation as a slave in 7-bit addressing mode, as follows:
   a. Initialize the MODE field in the I2C Mode Register for either SLAVE ONLY Mode or MASTER/SLAVE Mode with 7-bit addressing.
   b. Optionally set the GCE bit.
   c. Initialize the SLA[6:0] bits in the I2C Slave Address Register.
   d. Set IEN=1 in the I2C Control Register. Set NAK=0 in the I2C Control Register.
2. The master initiates a transfer by sending the address byte. The SLAVE Mode I2C controller finds an address match and detects that the R/$\overline{W}$ bit=1 (read by the master from the slave). The I2C controller acknowledges, indicating that it is ready to accept the transaction. The SAM bit in the I2CISTAT Register is set to 1, causing an interrupt. The RD bit is set to 1, indicating a read from the slave.
3. The software responds to the interrupt by reading the I2CISTAT Register, thereby clearing the SAM bit. Because RD=1, the software responds by loading the first data byte into the I2CDATA Register. The software sets the TXI bit in the I2CCTL Regis-

When the DAC is enabled, data existing in the data registers is converted. The data registers can be written while the DAC is disabled to provide the initial data word to be converted when the DAC is enabled.

Data can be right-justified or left-justified, as selected by the JUSTIFY bit in the DACCTL Register. If data is left-justified, 8-bit resolution can be achieved by writing only the Data High Register, DACD_H.

22.2.2. Power Control

The DAC is capable of performing conversions at three different power settings, as selected by the POWER bit. When POWER=00, the DAC runs at its highest current consumption and with the fastest settling time. When POWER=10, the DAC runs at its lowest current consumption and with the slowest settling time. The lower power consumption setting can reduce overall current consumption for applications with slower switching requirements.

22.2.3. Voltage References

DAC positive voltage reference selection options are selected by REFSEL to be one of the following:

- A_{VDD} (REFSEL=000)
- Internal voltage reference buffer connected to $V_{REF}+$ (REFSEL=1xx) which buffers the DAC internal voltage reference from the Reference System
- External voltage reference on $V_{REF}+$ (REFSEL=011)

The DAC negative reference should always be configured as $V_{REF}-$ using the GPIO Alternate Function Selection, which is described in the General-Purpose Input/Output chapter on page 55. Unless using AV_{DD} (REFSEL=000), the DAC positive voltage reference should be configured as $V_{REF}+$ using the GPIO Alternate Function selection. When using the internal voltage reference buffer connected to $V_{REF}+$ (REFSEL=1xx), an external bypass capacitor is required. Typically, an external bypass capacitor is also employed for an external voltage reference on $V_{REF}+$ (REFSEL=011).

The Reference System offers four possible internal voltage reference level settings that are also selected by REFSEL, namely: 1.25V, 1.5V, 2.0V, and 2.5V. Care should be exercised to ensure that A_{VDD} is always at least 0.5V greater than the selected internal voltage reference level. When the internal voltage reference buffer is selected, it is automatically enabled if both the DAC is enabled and the DAC output is selected using the GPIO alternate function registers.

The ADC voltage reference buffer can also be configured to connect to $V_{REF}+$. If both the ADC voltage reference buffer and the DAC voltage reference buffer are selected to connect to $V_{REF}+$, hardware will connect only the DAC voltage reference buffer to $V_{REF}+$.

Bit	Description (Continued)
[5:3] REFSEL	**DAC Positive Voltage Reference Select** If REFSEL = 1xx and the ADC is also configured to drive V_{REF}+, the DAC voltage reference buffer selection is used. 000: Internal connection to AV_{DD}. 001: Reserved. 010: Reserved. 011: V_{REF}+ pin driven by an external source. 100: 1.25V internal voltage reference from the Reference System is buffered and drives the V_{REF}+ pin. 101: 1.5V internal voltage reference from the Reference System is buffered and drives the V_{REF}+ pin. 110: 2.0V internal voltage reference from the Reference System is buffered and drives the V_{REF}+ pin. 111: 2.5V internal voltage reference from the Reference System is buffered and drives the V_{REF}+ pin.
[2] DFORMAT	**Data Format** 0: Data is unsigned (binary). 1: Data is signed (two's complement).
[1] DACTRIG	**DAC Triggering** 0: DAC conversion is triggered by a software or DMA write to the DACD_H register. 1: DAC conversion is triggered by an Event System input. While converting the data, interrupt request and DMA request will be asserted allowing transfer of the next data word to be converted.
[0] JUSTIFY	**Data Register Justification** 0: Data is left-justified. 1: Data is right-justified.

Chapter 23. Operational Amplifiers

Two low-power operational amplifiers (op amps) are available with Zilog's F6482 Series MCUs: Op Amp A and Op Amp B. These amplifiers are identical to each other, but each has different selectable features. Op Amp A can be configured internally with various voltage gain settings, whereas Op Amp B can be configured internally as a current source/sink. Both op amps can be internally configured to provide unity gain feedback. Each op amp input and output is accessible from the package pins.

Features include:

- Two general-purpose op amps (Op Amp A and Op Amp B), individually enabled and configured
- Rail-to-rail inputs and outputs
- Two power vs. bandwidth settings featuring low active currents of 1 µA and 30 µA
- Flexible multiplexed op amp inputs and outputs
- Outputs can drive selectable internal destinations such as the ADC, comparators and op amp inputs without consuming a GPIO
- Internal input and output connections available to conserve pins
- Can be internally configured as a unity gain buffer
- Op Amp A can be configured as a programmable gain amplifier using an internal programmable resistive feedback network that provides 16 gain steps
- Op Amp B can be configured internally as a regulated current source or sink
  - Internal current levels typically configured as 10 µA, 100 µA, or 1 mA
  - High-accuracy current sourcing/sinking with external resistor

23.1. Architecture

Op Amp A and Op Amp B have identical amplifiers but have different selectable features. Figure 80 shows a simplified block diagram of Op Amp A, including input connections and feedback paths for unity gain and programmable gain.

Bit	Description (Continued)
[3:2] INNSEL	**Negative Input Signal Select** 00: GPIO pin used as Comparator 0 negative input, C0INN. 01: If PREFEN=0, bandgap reference from the Reference Generator. If PREFEN=1, Programmable Reference 0, with level selected by PREFLVL and source selected by PREFSRC. 10: 1.25V (nominal) reference from the Reference Generator. 11: GPIO pin used as DAC output, DAC.
[1:0] INPSEL	**Positive Input Signal Select** 00: GPIO pin used as Comparator 0 positive input, C0INP 01: Temperature sensor. 10: GPIO pin used as Op Amp B output, AMPBOUT. 11: Op Amp A output. This selection provides an internal connection that does not involve the GPIO used as Op Amp A output, AMPAOUT.

24.4.3. Comparator 0 Control 1 Register

The Comparator 0 Control 1 Register is shown in Table 259. It provides control for Comparator 0 and Programmable Reference 0.

Table 259. Comparator 0 Control 1 Register (CMP0CTL1)

Bit	7	6	5	4	3	2	1	0
Field	POLSEL	PREFEN	PREFSRC	PREFLVL				
Reset	0	0	0	0	0	1	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F91h							

Bit	Description
[7] POLSEL	**Polarity Select** 0: Noninverted comparator output. The comparator output is High when the positive comparator input voltage is greater than the negative comparator input voltage. 1: Inverted comparator output. The comparator output is Low when the positive comparator input voltage is greater than the negative comparator input voltage.
[6] PREFEN	**Programmable Reference Enable** 0: Programmable Reference disabled. The bandgap is selected as the comparator negative input if INNSEL=01. 1: Programmable Reference enabled as defined by PREFSRC and PREFLVL. The Programmable Reference level is selected as the comparator negative input if INNSEL=01.

Table 263. LCD Display Memory Organization (Continued)

Subaddress in LCDSA*	Bit in LCDMEMAx, LCDMEMBx Subregisters							
	7	6	5	4	3	2	1	0
LCDMEMAx	COM3	COM2	COM1	COM0	COM3	COM2	COM1	COM0
12h	SEG05				SEG04			
11h	SEG03				SEG02			
10h	SEG01				SEG00			

Note: *LCDSA in the LCDSA Register contains the subregister address.

26.2.3. LCD Frame Timing

The LCD frame timing is a function of the LCD Controller clock selection, prescaler divide ratio, frame rate divide ratio, duty and contrast control. The LCD Controller clock selection, prescaler divide ratio, and frame rate divide ratio are configured in the LCD-CLK Register. Either PCLK or the WTO can be selected as the LCD Controller input clock source using the CLKSEL bit. The prescaler divide ratio is selected using the PRES-CALE bit, and the prescaler output clocks the frame rate divider and dynamic bias generator, as described in the Bias Generator Selection section on page 507. The frame rate divide ratio is selected using the FDIV bit, and results in the frame clock.

Duty, bias, and waveform type are configured with the LCDMODE bit in the LCD Control 2 Register (LCDCTL2). Contrast control is configured with CONTRAST in the LCD Control 1 Register (LCDCTL1), which selects the number of dead frame clock cycles per frame (Type A waveforms) or per frame pair (Type B waveforms). See the Waveform Generation section on page 508 and the Contrast Control section on page 516 to learn more.

For static, 1/2 and 1/4 duty:

Frame rate = (LCD Controller input clock frequency) ÷ ((8 + DEAD CYCLES) * PRESCALE * FDIV)

In this equation, DEAD CYCLES is selected by the value of CONTRAST.

For 1/3 duty:

Frame rate = (LCD Controller input clock frequency) ÷ ((6 + DEAD CYCLES) * PRESCALE * FDIV

In this equation, DEAD CYCLES is selected by the value of CONTRAST.

For Type A waveforms, the common signals (COMx) repeat each LCD frame, whereas for Type B waveforms, the common signals repeat after every two LCD frames.

- The Page Select Register can be written when the Flash Controller is unlocked.
- The Mass Erase command is enabled through the Flash Control Register

! Caution: For security reasons, the Flash controller allows only a single page to be opened for write/erase. When writing multiple Flash pages, the Flash controller must go through the unlock sequence again to select another page.

27.3. Flash Control Register Definitions

This section defines the features of the following Flash Control registers.

Flash Control Register

Flash Status Register: see page 536

Flash Page Select Register: see page 537

Flash Block Protect Register: see page 538

Flash Programming Configuration: see page 539

27.3.1. Flash Control Register

The Flash Controller must remain unlocked when using the Flash Control Register (shown in Table 278) before programming or erasing Flash memory. The Flash Controller is unlocked by writing the Flash Page Select Register, then 73h 8Ch, sequentially, to the Flash Control Register. A final write must then be made to the Flash Page Select Register with the same value as the previous write. When the Flash Controller is unlocked, Mass Erase or Page Erase can be initiated by writing the appropriate command to the FCTL. Page Erase applies only to the active page selected in the Flash Page Select Register. Mass Erase is enabled only through the On-Chip Debugger. Writing an invalid value or an invalid sequence returns the Flash Controller to its locked state. The write-only Flash Control Register shares its Register File address with the read-only Flash Status Register.

28.2.2. Trim Bit Data Register

The Trim Bit Data Register, shown in Table 285, contains the read or write data for access to the trim option bits.

Table 285. Trim Bit Data Register (TRMDR)

Bit	7	6	5	4	3	2	1	0
Field	TRMDR							
Reset	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FF7h							

Bit	Description
[7:0] TRMDR	**Trim Bit Data** 00–FF: TRMDR is a portal providing access to all trim option bit registers as selected by the TRMADR Register.

28.3. Flash Option Bit Address Space

The first two bytes of Flash Program Memory, at addresses 0000h and 0001h, are reserved for the user-programmable Flash Option bits. See Table 286.

Table 286. Flash Option Bits at Program Memory Address 0000h

Bit	7	6	5	4	3	2	1	0
Field	WDT_RES	WDT_AO	Reserved		VBOCTL		FRP	FWP
Reset*	X	X	X	X	1	1	X	X
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	Program Memory 0000h							

Note: *RESET = POR reset only; X=undefined; R/W=read/write.

Bit	Description
[7] WDT_RES	**Watchdog Timer Reset** 0: Watchdog Timer time-out generates an interrupt request. Interrupts must be globally enabled for the eZ8 CPU to acknowledge the interrupt request. 1: Watchdog Timer time-out causes a System Reset. This setting is the default for unprogrammed (erased) Flash.

Table 329. Supply Current Characteristics (Continued)

		T_A = –40°C to +85°C				
Symbol	**Parameter**	**Min**	**Typical[1]**	**Max**	**Units**	**Conditions[2]**
I_{DDS1}	Stop Mode Device Current with FRECOV = 1		2.9		µA	All peripherals disabled including VBO and WDT[3,4,6]
I_{DDS2}	Stop Mode Device Current with FRECOV = 0		0.7		µA	All peripherals disabled including VBO and WDT[3,4,6]

Notes:
1. These values are provided for design guidance only and are not tested in production.
2. Typical conditions are defined as 3.0V at 25°C, unless otherwise noted.
3. All internal pull ups are disabled and all push-pull outputs are unloaded.
4. All open-drain outputs are pulled up to V_{DD}/AV_{DD} and are at a High state.
5. System clock source is an external square wave clock signal driven through the CLKIN pin.
6. All inputs are at V_{DD}/AV_{DD} or V_{SS}/AV_{SS} as appropriate.

33.3. AC Characteristics

Table 330 lists the AC characteristics and timing of the F6482 Series products. All AC timing information assumes a standard load of 50pF on all outputs.

Table 330. AC Characteristics

		V_{DD} = 1.8 to 3.6V T_A = –40°C to +85°C				
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
F_{SYSCLK}	System Clock Frequency			24	MHz	See Figure 106
T_{XIN}	CLKIN Period	41.66			ns	TCLK = $1/F_{SYSCLK}$
T_{XINH}	CLKIN High Time	16.66		25	ns	TCLK = 41.66 ns
T_{XINL}	CLKIN Low Time	16.66		25	ns	TCLK = 41.66 ns
T_{XINR}	CLKIN Rise Time			3	ns	TCLK = 41.66 ns
T_{XINF}	CLKIN Fall Time			3	ns	TCLK = 41.66 ns
T_{XIN2}	CLK2IN Period		30.5		µs	TCLK = $1/F_{PCLK}$
F_{PCLK}	Peripheral Clock Frequency		32.768		kHz	

33.4.2. Voltage Brown-Out

Table 332 presents electrical and timing data for the F6482 Series' Voltage Brown-Out function.

Table 332. Voltage Brown-Out Electrical Characteristics and Timing

		T_A = –40°C to +85°C				
Symbol	**Parameter**	**Min**	**Typ***	**Max**	**Units**	**Conditions**
$I_{DD}VBO$	VBO Active Current		2		µA	Normal and Halt modes
			0.07		µA	Stop Mode
V_{VBO}	Voltage Brown-Out Reset Voltage Threshold	1.8	1.85	1.9	V	$V_{DD}=V_{VBO}$
V_{HYS}	Hysteresis of V_{VBO}		100		mV	
T_{RESET}	Reset Delay		10		ms	$V_{DD} > V_{POR}$, $V_{DD} > V_{VBO}$

Note: *Data in the Typical column is from characterization at 3.0V and 25°C. These values are provided for design guidance only and are not tested in production.

33.4.3. Stop-Mode Recovery

Table 333 presents electrical and timing data for the F6482 Series' Stop-Mode Recovery function.

Table 333. Stop-Mode Recovery (SMR) Timing

		T_A = –40°C to +85°C				
Symbol	**Parameter**	**Min**	**Typ***	**Max**	**Units**	**Conditions**
T_{SMRD}	Stop-Mode Recovery Latency		6 SYSCLKs + T_{SMRD}			FRECOV=0
			6 SYSCLKs			FRECOV=1
T_{SMRD}	Stop-Mode Recovery Delay		300		µs	

Note: *Data in the Typical column is from characterization at 3.0V and 25°C. These values are provided for design guidance only and are not tested in production.

33.4.14. Liquid Crystal Display

Table 344 presents electrical and timing data for the F6482 Series' Liquid Crystal Display (LCD) function.

Table 344. LCD Electrical Characteristics

		T_A = –40°C to +85°C V_{DD} = 1.8V to 3.6V				
Symbol	**Parameter**	**Min**	**Typ***	**Max**	**Units**	**Conditions**
V_{VLCD}	VLCD pin Voltage	1.8		3.6	V	
I_{DD}LCD	LCD Active Current with Internal Charge Pump Off (CPEN=0)		0.67[2]		µA	BIASGSEL=0, HBDUR=000
			1.19[2]		µA	BIASGSEL=0, HBDUR=001
			0.67[2]		µA	BIASGSEL=1, HBDUR=000
			2.75[2]		µA	BIASGSEL=1, HBDUR=001
I_{DD}CP	LCD Charge Pump Active Current (CPEN=1)		1.9[3]		µA	Doubler (CPTSEL=1, BIASGSEL=0)
			2.7[3]		µA	Tripler (CPTSEL=0, BIASGSEL=0)
			–		µA	Doubler (CPTSEL=1, BIASGSEL=1)
			–		µA	Tripler (CPTSEL=0, BIASGSEL=1)

Notes:
1. Data in the Typical column is from characterization at 3.0V and 25°C. These values are provided for design guidance only and are not tested in production.
2. Based on PCLK= 32.768kHz (CKSEL=0), 32 Hz frame rate (PRESCALE=011, FDIV=0111), and LCD mode of 1/4 duty, 1/3 bias, type A waveform (LCDMODE=1011). Either VLCD=3V (VLCDDIR=0) or V_{DD}=3V (VLCDDIR=0, CPEN=0). No LCD panel load.
3. VLCD=3.06V (CONTRAST=100), V_{DD}=3.0V.

Table 356. F6482 Series Ordering Information

Part Number	Flash	Register RAM	LCD	128B NVDS	I²C Master/Slave Controller	ESPI	USB	I/O Lines	Interrupt Vectors	16-Bit Timers w/ PWM	12-Bit A/D Channels	UART with LIN/DALI/DMX	Comparator	Op Amp	Temperature Sensor	Multichannel Timer	Description
Z8 Encore! XP F1682 Series with 16KB Flash, 12-Bit Analog-to-Digital Converter																	
Extended Temperature: –40 °C to 85 °C																	
Z8F1682AT024XK	16KB	2KB	1	1	1	2	1	67	41	3	12	2	2	2	1	1	LQFP 80-pin package
Z8F1682AR024XK	16KB	2KB	1	1	1	2	0	51	30	3	8	1	1	1	1	0	LQFP 64-pin package
Z8F1681AR024XK	16KB	2KB	0	1	1	2	1	52	40	3	12	2	2	2	1	1	LQFP 64-pin package
Z8F1681QN024XK	16KB	2KB	0	1	1	1	1	36	39	3	10	2	2	2	1	1	QFN 44-pin package
Z8F1681AN024XK	16KB	2KB	0	1	1	1	1	36	39	3	10	2	2	2	1	1	LQFP 44-pin package
Z8F1681QK024XK	16KB	2KB	0	1	1	1	1	26	31	3	9	1	1	1	1	0	QFN 32-pin package
Z8 Encore! XP F6482 Series Development Kit																	
Z8F64820100ZCOG	Z8 Encore! XP F6482 Series Development Kit																
ZUSBSC00100ZACG	USB Smart Cable Accessory Kit																
ZUSBOPTSC01ZACG	USB Opto-Isolated Smart Cable Accessory Kit																
ZENETSC0100ZACG	Ethernet Smart Cable Accessory Kit																

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