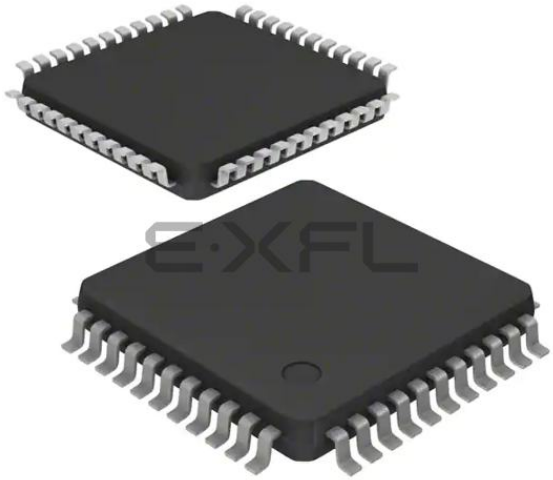

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	eZ8
Core Size	8-Bit
Speed	24MHz
Connectivity	DALI, DMX, I²C, LINbus, SPI, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	60KB (60K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3.75K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 10x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f6081an024xk

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Table 8. Register File Address Map (Continued)

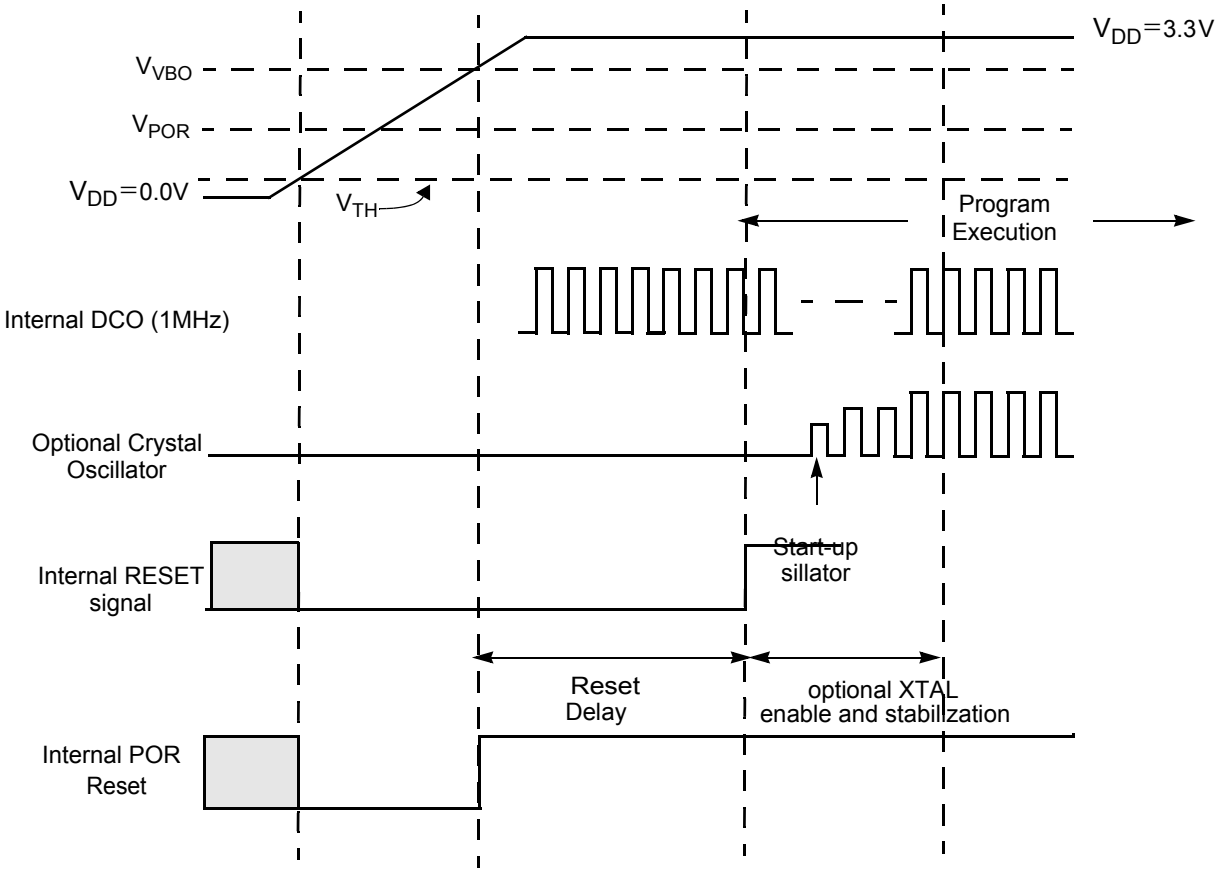
Address (Hex)	Register Description	Mnemonic	Reset (Hex)	Page #
Timer 1 (Continued)				
F0B	Timer 1 Reload Low Byte	T1RL	FF	176
F0C	Timer 1 PWM0 High Byte	T1PWM0H	00	177
F0D	Timer 1 PWM0 Low Byte	T1PWM0L	00	177
F0E	Timer 1 Control 0	T1CTL0	00	179
F0F	Timer 1 Control 1	T1CTL1	00	180
F24	Timer 1 PWM1 High Byte	T1PWM1H	00	178
F25	Timer 1 PWM1 Low Byte	T1PWM1L	00	178
F26	Timer 1 Control 2	T1CTL2	00	184
F27	Timer 1 Status	T1STA	00	185
F2D	Timer 1 Noise Filter Control	T1NFC	00	186
Timer 2				
F10	Timer 2 High Byte	T2H	00	175
F11	Timer 2 Low Byte	T2L	01	175
F12	Timer 2 Reload High Byte	T2RH	FF	176
F13	Timer 2 Reload Low Byte	T2RL	FF	176
F14	Timer 2 PWM0 High Byte	T2PWM0H	00	177
F15	Timer 2 PWM0 Low Byte	T2PWM0L	00	177
F16	Timer 2 Control 0	T2CTL0	00	179
F17	Timer 2 Control 1	T2CTL1	00	180
F18–F1F	Reserved	–	XX	
F28	Timer 2 PWM1 High Byte	T2PWM1H	00	180
F29	Timer 2 PWM1 Low Byte	T2PWM1L	00	178
F2A	Timer 2 Control 2	T2CTL2	00	184
F2B	Timer 2 Status	T2STA	00	185
F2E	Timer 2 Noise Filter Control	T2NFC	00	186
F2F	Reserved	–	XX	
RTC				
F30	Real-Time Clock Seconds	RTC_SEC	XX	213
F31	Real-Time Clock Minutes	RTC_MIN	XX	214
F32	Real-Time Clock Hours	RTC_HRS	XX	216
F33	Real-Time Clock Day-of-the-Month	RTC_DOM	XX	217

the supply voltage reaches a safe circuit operating level when the device is powered on. V_{DD} must be greater than both V_{POR} and V_{VBO} to exit the Reset state.

After power on, the POR circuit keeps idle until the supply voltage drops below V_{TH} voltage. Figure 8 on page 42 shows this POR behavior.

After the F6482 Series MCU exits the POR state, the eZ8 CPU fetches the Reset vector. Following this POR, the POR/VBO status bit in the Reset Status Register is set to 1.

For the POR threshold voltage (V_{POR}) and POR start voltage V_{TH} , see the Electrical Characteristics chapter on page 598.



Notes
1. Not to Scale.
2. Internal Reset and POR Reset are Low active.

Figure 7. Power-On Reset Operation

Chapter 7. General-Purpose Input/Output

The F6482 Series products support a maximum of 67 port pins (ports A–J) for general-purpose input/output (GPIO) operations. Each port contains control and data registers. The GPIO control registers determine data direction, open-drain, output drive current, programmable pull-ups, Stop-Mode Recovery functionality, and alternate pin functions. Each port pin is individually programmable.

7.1. GPIO Port Availability by Device

Table 16 lists the port pins available with each device and package type.

Table 16. Port Availability by Device and Package Type

Device	Pkg.	12-Bit ADC	I^2C	LCD	SPI	UART	USB	Port A	Port B	Port C	Port D	Port E	Port F	Port G	Port H	Port J	Total I/O
Z8F6481QK, Z8F6081QK, Z8F3281QK, Z8F1681QK	32-pin QFN	9	1	–	1	1	1	[7:0]	[6:0]	[7:0]	[0]	[1:0]	–	–	–	–	26
Z8F6481AN, Z8F6081AN, Z8F3281AN, Z8F1681AN	44-pin LQFP	10	1	–	1	2	1	[7:0]	[4:0]	[7:0]	[7:0]	[6:0]	–	–	–	–	36
Z8F6481QN, Z8F6081QN, Z8F3281QN, Z8F1681QN	44-pin QFN	10	1	–	1	2	1	[7:0]	[4:0]	[7:0]	[7:0]	[6:0]	–	–	–	–	36
Z8F6481AR, Z8F6081AR, Z8F3281AR, Z8F1681AR	64-pin LQFP	12	1	–	2	2	1	[7:0]	[7:0]	[7:0]	[7:0]	[6:0]	[7:0]	[4:0]	–	–	52
Z8F6482AR, Z8F6082AR, Z8F3282AR, Z8F1682AR	64-pin LQFP	8	1	1	2	1	0	[7:0]	[5:0]	[7:0]	[0]	–	[7:0]	[7:0]	[7:0]	[3:0]	51
Z8F6482AT, Z8F6082AT, Z8F3282AT, Z8F1682AT	80-pin LQFP	12	1	1	2	2	1	[7:0]	[7:0]	[7:0]	[7:0]	[6:0]	[7:0]	[7:0]	[7:0]	[3:0]	67

Table 18. Port Alternate Function Mapping (44-Pin Parts) (Continued)

Port	Pin	Mnemonic	Alternate Function Description	Alternate Function Set Subregisters
Port E[1]	PE0	DP	USB DP	AFS1[0]: 0
		T0IN/$\overline{\text{T0OUT}}$	Timer 0 Input/Timer 0 Output Complement	AFS1[0]: 1
	PE1	DM	USB DM	AFS1[1]: 0
		T0OUT	Timer 0 Output	AFS1[1]: 1
	PE2	T4IN	Multi Channel Timer Input	AFS1[2]: 0
		Reserved		AFS1[2]: 1
	PE3	T4CHA	Multi Channel Timer Input/Output A	AFS1[3]: 0
		ESOUT[0]	Event System Out 0	AFS1[3]: 1
	PE4	T4CHB	Multi Channel Timer Input/Output B	AFS1[4]: 0
		ESOUT[1]	Event System Out 1	AFS1[4]: 1
	PE5	T4CHC	Multi Channel Timer Input/Output C	AFS1[5]: 0
		ESOUT[2]	Event System Out 2	AFS1[5]: 1
	PE6	T4CHD	Multi Channel Timer Input/Output D	AFS1[6]: 0
		ESOUT[3]	Event System Out 3	AFS1[6]: 1

Notes
1. Because there are at most two choices of alternate function for some pins of Ports A, B, D and E, the Alternate Function Set register AFS2 is not implemented. Additionally, alternate function selection, as described in the Port A–J Alternate Function Subregisters (see page 88), must also be enabled.
2. The alternate function selection for Port C, as described in the Port A–J Alternate Function Subregisters (see page 88), must also be enabled.

$$PLL_{CLK} = \frac{PLL_{CLKIN}}{(PLLRDIV + 1)} \times \frac{(PLLNDIV+1)}{(PLLODIV+1)}$$

The operands in the above equation can be defined as:

- PLL_{CLKIN} is either HFXO or the External Clock Drive, as selected by the PLLSEL
- PLL_{RDIV} + 1 is the PLL reference divider ratio
- PLL_{NDIV} + 1 is the PLL feedback divider ratio
- PLL_{ODIV} + 1 is the PLL output divider ratio

The PLL should be configured in accordance with the following requirements:

- PLL_{CLK}IN: 0.3125 MHz–24 MHz
- Reference divider output frequency (PLL core input clock): 0.3125–24 MHz, 1.5 MHz – the recommended minimum for when clocking the USB
- PLL VCO frequency (input to output divider): 80 MHz–384 MHz
- PLL_{CLK} (PLL output): 48 MHz max. If PLL_{CLK} is >25 MHz and is selected as the source for System Clock, SCKDIV must be configured such that System Clock does not exceed 24 MHz.

Table 37 lists common PLL configurations to generate a 48 MHz PLL_{CLK} for the USB that satisfy the 2500 ppm data rate requirement.

Table 37. Common PLL Configurations for 48 MHz PLLCLK

PLL_{CLKIN} (MHz)	PLL_{RDIV}	PLL Core (MHz)	PLL_{NDIV}	VCO (MHz)	PLL_{ODIV}
1.5	0	1.5	63	96	1
1.6	0	1.6	59	96	1
2	0	2	47	96	1
2.4	0	2.4	39	96	1
3	0	3	31	96	1
3.2	0	3.2	29	96	1
3.84	0	3.84	24	96	1
4	0	4	23	96	1
4.5	2	1.5	63	96	1
4.8	1	2.4	39	96	1
5	0	5	47	240	4

Bit	Description (Continued)
[2:0] SCKSEL	**System Clock Source Select** There is a delay from the writing of SCKSEL to the actual switching from the currently active clock source to the new, desired clock source. Reading SCKSEL return the currently active clock source. 000: Digitally Controlled Oscillator (DCO). 001: Peripheral Clock (PCLK). 010: High Frequency Crystal Oscillator (HFXO) or external clock drive, CLKIN on PA0, based on PLL Clock Source Select (PLLSEL). 011: Phase Locked Loop (PLL). 100: Watchdog Timer Oscillator (WTO). 101: Reserved. 110: Reserved. 111: Reserved.

8.11.2. Clock Control 1 Register

The Clock Control 1 (CLKCTL1) Register, shown in Table 39, enables/disables the IPO and LFXO, selects PCLK Stop Mode behavior, selects the PCLK source, enables/disables WTO failure detection, and contains a ready bit for the IPO. Before writing CLKCTL1, the clock control registers must be unlocked as described in the Clock System Control Register Unlocking/Locking section on page 103.

Table 39. Clock Control 1 Register (CLKCTL1)

Bit	7	6	5	4	3	2	1	0
Field	IPORDY	Reserved	WTOFEN	PCKSEL		PCKSM	LFXOEN	IPOEN
Reset	0	0	0	0	0	0	0	1
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Address	F83h							

Bit	Description
[7] IPORDY	**Internal Precision Oscillator (IPO) Ready Flag** 0: The IPO is not ready. 1: The IPO is ready.
[6]	**Reserved** This bit is reserved and must be programmed to 0.
[5] WTOFEN	**Watchdog Timer Oscillator Failure Detection Enable** 0: Failure detection of Watchdog Timer Oscillator is disabled. 1: Failure detection of Watchdog Timer Oscillator is enabled.

If an initial starting value other than 0001h is loaded into the Timer High and Low Byte registers, the One-Shot Mode equation must be used to determine the first PWM time-out period.

If TPOL is set to 0, the ratio of the PWM output High time to the total period is calculated using the following equation:

$$\text{PWM Output High Time Ratio (\%)} = \frac{\text{Reload Value - PWM Value}}{\text{Reload Value}} \times 100$$

If TPOL is set to 1, the ratio of the PWM output High time to the total period is calculated using the following equation:

$$\text{PWM Output High Time Ratio (\%)} = \frac{\text{PWM Value}}{\text{Reload Value}} \times 100$$

10.1.3.8. Capture Mode

In Capture Mode (TMODE=0100), the current timer count value is recorded when the appropriate external Timer Input 0 transition occurs. The Capture count value is written to the Timer PWM0 High and Low Byte registers. The Timer counts timer clocks up to the 16-bit reload value. The TPOL bit in the Timer Control 1 Register determines if the Capture occurs on a rising edge or a falling edge of the Timer Input 0 signal. When the Capture event occurs, an interrupt is generated and the timer continues counting. The INPCAP bit in Timer Control 0 Register is set to indicate the timer interrupt is due to an input capture event.

The timer continues counting up to the 16-bit reload value stored in the Timer Reload High and Low Byte registers. Upon reaching the reload value, the timer generates an interrupt and continues counting. The INPCAP bit in Timer Control 0 Register is cleared to indicate the timer interrupt is not due to an input capture event.

Observe the following steps to configure a timer for Capture Mode and initiate the count:

1. Write to the Timer Control 1 Register to:
   - Disable the timer
   - Configure the timer for Capture Mode
   - Set the prescale value
   - Set the Capture edge (rising or falling) for the Timer Input 0
2. Write to the Timer Control 2 Register to choose the timer clock source.
3. Write to the Timer Control 0 Register to set the timer interrupt configuration field TICONFIG.
4. Write to the Timer High and Low Byte registers to set the starting count value (typically 0001h).

17.3.3. USB Control Register

The USB Control Register, shown in Table 172, selects the USB Module endpoint buffer memory addressing method and the endpoint buffer memory section for the USBSD access.

Table 172. USB Control Register (USBCTL)

Bit	7	6	5	4	3	2	1	0
Field	Reserved	AI	EPSEL			Reserved		
Reset	0	0	0	0	0	0	0	0
R/W	R	R/W	R/W	R/W	R/W	R	R	R
Address	F5Bh							

Bit	Description
[7]	**Reserved** This bit is reserved and must be programmed to 0.
[6] AI	Addressing Select 0: Accesses to the endpoint buffer selected by EPSEL will auto-increment. 1: Accesses to the endpoint buffer selected by EPSEL will not auto-increment.
[5:3] EPSEL	Endpoint Select 000: IN endpoint 0 buffer memory. 001: IN endpoint 1 buffer memory. 010: IN endpoint 2 buffer memory. 011: IN endpoint 3 buffer memory. 100: OUT endpoint 0 buffer memory. 101: OUT endpoint 1 buffer memory. 110: OUT endpoint 2 buffer memory. 111: OUT endpoint 3 buffer memory.
[2:0]	**Reserved** These bits are reserved and must be programmed to 000.

17.3.16. USB OUT Interrupt Enable Subregister

The USB OUT Interrupt Enable Subregister, shown in Table 185, controls the enabling of OUT endpoint interrupt requests.

Table 185. USB OUT Interrupt Enable Subregister (USBOUTIEN)

Bit	7	6	5	4	3	2	1	0
Field	Reserved				OUT3IEN	OUT2IEN	OUT1IEN	OUT0IEN
Reset	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Address	If USBSA = 2Dh in the USB Subaddress Register, accessible through the USB Subdata Register							

Bit	Description
[7:4]	**Reserved** These bits are reserved and must be programmed to 0000.
[3] OUT3IEN	**OUT Endpoint 3 Interrupt Enable** 0: Interrupts from OUT endpoint 3 are disabled. 1: Interrupts from OUT endpoint 3 are enabled.
[2] OUT2IEN	**OUT Endpoint 2 Interrupt Enable** 0: Interrupts from OUT endpoint 2 are disabled. 1: Interrupts from OUT endpoint 2 are enabled.
[1] OUT1IEN	**OUT Endpoint 1 Interrupt Enable** 0: Interrupts from OUT endpoint 1 are disabled. 1: Interrupts from OUT endpoint 1 are enabled.
[0] OUT0IEN	**OUT Endpoint 0 Interrupt Enable** 0: Interrupts from OUT endpoint 0 are disabled. 1: Interrupts from OUT endpoint 0 are enabled.

Bit	Description (Continued)
[1] CHAIN32	**Chain DMA3and DMA2** 0: DMA3 and DMA2 are independent of each other. 1: DMA3 and DMA2 are chained together, as described in the Chain Operation section on page 393.
[0] CHAIN10	**Chain DMA1 and DMA0** 0: DMA1 and DMA0 are independent of each other. 1: DMA1 and DMA0 are chained together, as described in the Chain Operation section on page 393.

18.3.4. DMA Source Address Subregisters

The DMAxSRCH and DMAxSRCL subregisters, shown in Tables 207 and 208, combine to form the 12-bit source address for the DMA transaction. Upon each byte transfer, the source address is updated based on the SRCCTL configuration in the DMAx Control 0 Subregister. In addition, DMAxSRCH contains transfer in list (TXLIST) control.

Table 207. DMA Source Address High Subregister (DMAxSRCH)

Bit	7	6	5	4	3	2	1	0
Field	TXLIST	Reserved			SRCH			
Reset	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Address	If DMASA = 0h in the DMAxSA Register, accessible through the DMA 0–3 Subregister							

Bit	Description
[7] TXLIST	**Transfer In List** TXLIST has an effect only during linked list operation, see the Linked List Control Options section on page 395 for details.
[6:4]	**Reserved** These bits are reserved and must be programmed to 000.
[3:0] SRCH	**Source Address High** 0–F: Upper 4 bits of the DMA source address.

output, ESOUT[3:0], that is available for a particular port pin. See the General-Purpose Input/Output chapter on page 55 to learn more regarding alternate function selection.

19.4. Timing Considerations

The Event System essentially performs a multiplexing function. Signals sourced to Event System channels do not go through a synchronization process within the Event System. As such, the signals on Event System channels must be sufficient in duration for detection by their corresponding destinations. Any source and destination pair that are using the same clock, one of SYSCLK, PCLK, or the WTO, can be connected to each other via the Event System without concern about source signal duration. When the Event System source and destination pair are using dissimilar clocks, the Event System source signal should be at least 1.5 times the duration of the clock period of the Event System destination to assure that the destination will detect the signal from the source.

19.5. Event System Usage Examples

To illustrate the usage of the Event System, let's examine the following two examples.

Example 1: Triggering Periodic ADC Conversions Using a Timer. In this example, a timer serves as the signal source to Event System channel 0 and the this channel is selected to trigger ADC conversions.

- Select Timer 0 out as the signal source for Event System channel 0, as follows:
  - Write 00h to the ESSSA Register to select the ESCH0SRC Subregister.
  - Write 10h to the ESSSD Register. This accesses the ESCH0SRC Subregister to select Timer 0 out as the Event System channel 0 source.
- Configure the ADC conversion parameters. For instance, the ADC could be configured with a window function such that interrupts are generated only when the window is exceeded.
- If a DMA is desired, configure the DMA Controller to transfer the ADC results to memory.
- Configure the ADC to respond to Event System channel 0, as follows:
  - Write 04h to the ESDSA Register to select the ESDST04CH Subregister.
  - Write 08h to the ESDSD Register. This accesses ESDST04CH Subregister to enable Event System connection to the ADC and to select channel 0 as input to the ADC.

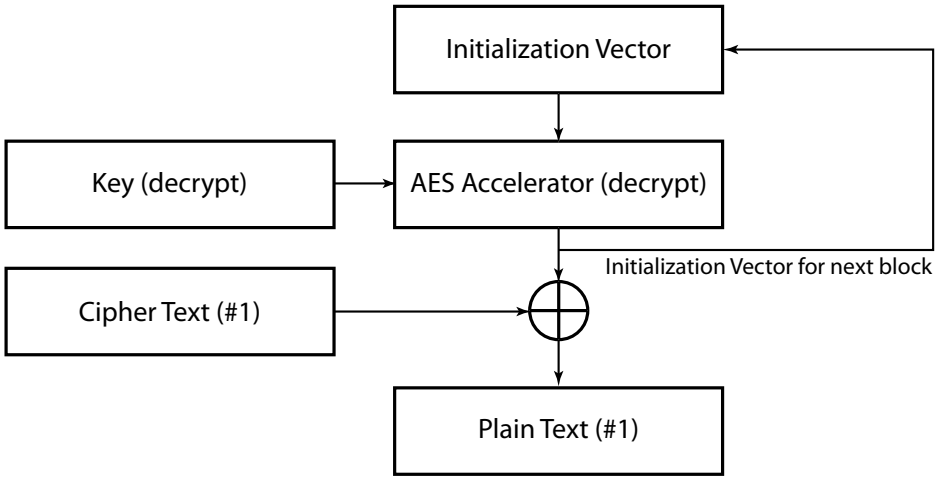


Figure 67. OFB Mode Decryption Flow Diagram

20.2.4.2. OFB Mode Encryption Example

The following steps are required to support OFB Mode encryption operation.

1. Write the AESCTRL Register as follows: AES_EN=1, MODE=01 (OFB), DECRYPT=0, AUTODIS=1.
2. Write the AESKEY Register with the encryption key.
3. Set the IVEN bit.
4. Write the Initialization Vector to the AESIV Register.
5. Clear the IVEN bit; DMA and IRQ will not occur while this bit is set.
6. Write the plain text data to the AESDATA Register, or use DMA.
7. Set the START/BUSY bit in the AESSTAT Register, or use auto-start by setting AUTODIS=0 in Step 1.
8. Poll the START/BUSY bit, or use an interrupt.
9. Read the cipher text from the AESDATA Register, or use DMA. The Initialization Vector is overwritten in preparation for the next 128-bit data block AES encryption operation, as shown in Figure 66.

Chapter 22. Digital-to-Analog Converter

The F6482 Series MCUs include a high-performance Digital-to-Analog Converter (DAC). This DAC converts a 12-bit digital input code to an analog output signal. The DAC offers the following features:

- 12-bit resolution
- Output driven externally on GPIO; internal connections to comparators and ADC
- Conversion initiated by software or Event System input
- Data buffering option
- Data can be left- or right-justified with either unsigned (binary) or signed (two's-complement) format
- DMA support
- Internal positive voltage reference selections of A_{VDD} or the DAC V_{REF} from the Reference System (2.5V, 2.0V, 1.5V, 1.25V) which is driven on V_{REF}+ for decoupling
- Ability to utilize external reference voltage
- Three power settings providing programmable power vs. settling time; see the Electrical Characteristics chapter on page 598 to learn more

22.1. Architecture

The DAC architecture, shown in Figure 78, consists of a data register, an internal voltage reference buffer, and a 12-bit DAC.

Bit	Description (Continued)
[5] PREFSRC	**Programmable Reference Source Selection** 0: VBIAS is the highest tap of the Programmable Reference. 1: AV_{DD} is the highest tap of the Programmable Reference.
[4:0] PREFLVL	**Programmable Reference Level Selection** 0000 to 1111: Programmable reference level=(PREFSRC selection) * (PREFLVL + 1) ÷ 32.

26.3.3. LCD Clock Register

The LCD Clock Register, shown in Table 269, controls the clocking of the LCD including: clock selection, clock prescale division and frame clock division.

Table 269. LCD Clock Register (LCDCLK)

Bits	7	6	5	4	3	2	1	0
Field	CLKSEL	PRESCALE			FDIV			
Reset	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FB3h							

Bit	Description
[7] CLKSEL	**LCD Clock Selection** 0: PCLK. 1: WTO.
[6:4] PRESCALE	**LCD Clock Prescale Divider** 000: Divide by 1. 001: Divide by 2. 010: Divide by 4. 011: Divide by 8. 100: Divide by 16. 101: Divide by 32. 110: Reserved. 111: Reserved.
[3:0] FDIV	**Frame Divider** 0000: Divide by 8. 0001: Divide by 9. 0010: Divide by 10. 0011: Divide by 11. 0100: Divide by 12. 0101: Divide by 13. 0110: Divide by 14. 0111: Divide by 16. 1000: Divide by 18. 1001: Divide by 20. 1010: Divide by 22. 1011: Divide by 24. 1100: Divide by 26. 1101: Divide by 28. 1110: Divide by 30. 1111: Divide by 32.

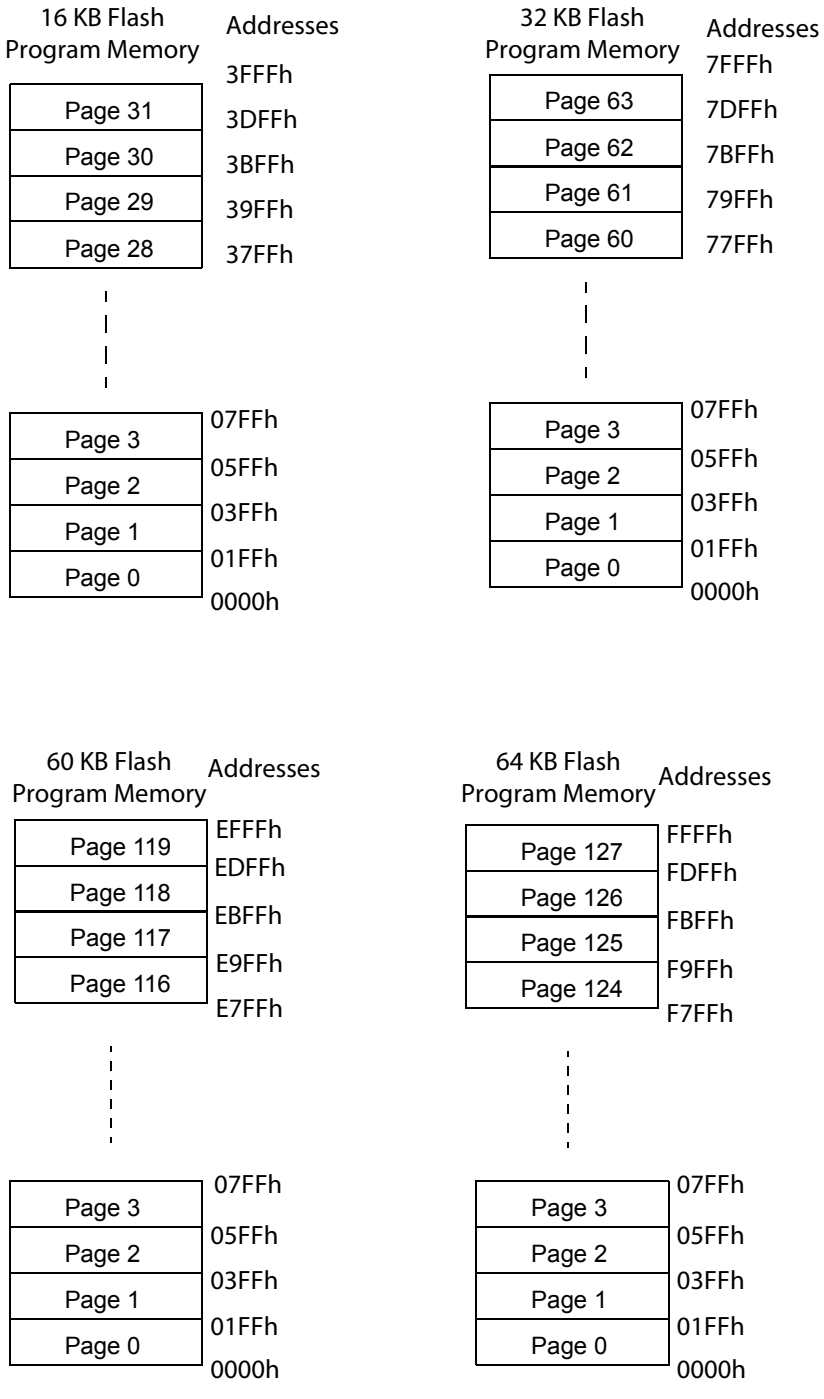


Figure 94. Flash Memory Arrangement

27.2.1. Flash Operation Timing

Before performing either a program or erase operation on Flash memory, the Digitally Controlled Oscillator (DCO) must be running and must be locked using the Frequency Locked Loop (FLL) to a minimum frequency of 1 MHz.

27.2.2. Flash Code Protection Against External Access

The user code contained within Flash memory can be protected against external access with the On-Chip Debugger. Programming the FRP Flash option bit prevents the reading of user code with the On-Chip Debugger. To learn more, see the Flash Option Bit Address Space section on page 544 and the On-Chip Debugger section on page 558.

27.2.3. Flash Code Protection Against Accidental Program and Erasure

The F6482 Series provides several levels of protection against accidental program and erasure of the Flash memory contents. This protection is provided by a combination of the Flash option bits, the register locking mechanism, the page select redundancy, and the block level protection control of the Flash Controller.

27.2.3.1. Flash Code Protection Using the Flash Option Bits

The FWP Flash option bit provides Flash Program Memory protection as listed in Table 277. To learn more, see the Flash Option Bit Address Space section on page 544.

Table 277. Flash Code Protection Using the Flash Option Bit

FWP	Flash Code Protection Description
0	Programming and erasing disabled for all of Flash Program Memory. In user code programming, Page Erase, and Mass Erase are all disabled. Mass Erase is available through the On-Chip Debugger.
1	Programming and Page Erase are enabled for all of Flash Program Memory. Mass Erase is available through the On-Chip Debugger.

27.2.3.2. Flash Code Protection Using the Flash Controller

At Reset, the Flash Controller locks to prevent accidental program or erasure of Flash memory. Observe the following procedure to unlock the Flash Controller from user code:

1. Write the Page Select Register with the target page.
2. Write the first unlock command, 73h, to the Flash Control Register.
3. Write the second unlock command, 8Ch, to the Flash Control Register.
4. Rewrite the Page Select Register with the target page previously stored in this register in Step 1.

Tables 317 through 324 contain the instructions belonging to each group and the number of operands required for each instruction. Some instructions appear in more than one table, because these instructions should be considered as a subset of more than one category. Within these tables, the source operand is identified as *src*, the destination operand is *dst*, and the condition code is *cc*.

Table 317. Arithmetic Instructions

Mnemonic	Operands	Instruction
ADC	dst, src	Add with Carry
ADCX	dst, src	Add with Carry using Extended Addressing
ADD	dst, src	Add
ADDX	dst, src	Add using Extended Addressing
CP	dst, src	Compare
CPC	dst, src	Compare with Carry
CPCX	dst, src	Compare with Carry using Extended Addressing
CPX	dst, src	Compare using Extended Addressing
DA	dst	Decimal Adjust
DEC	dst	Decrement
DECW	dst	Decrement Word
INC	dst	Increment
INCW	dst	Increment Word
MULT	dst	Multiply
SBC	dst, src	Subtract with Carry
SBCX	dst, src	Subtract with Carry using Extended Addressing
SUB	dst, src	Subtract
SUBX	dst, src	Subtract using Extended Addressing

Table 337. Analog-to-Digital Converter Electrical Characteristics and Timing (Continued)

		V_{DD}=1.8V to 3.6V T_A=–40°C to +85°C				
Symbol	**Parameter**	**Min**	**Typ***	**Max**	**Units**	**Conditions**
V_{INT_REF}	Internal Reference Voltage	–1.5%	1.25	+1.5%	V	REFSEL=1x, REFLVL=00, AV_{DD} ≥ 1.8V
		–1.5%	1.50	+1.5%	V	REFSEL=1x, REFLVL=01, AV_{DD} ≥ 2.0V
		–1.5%	2.0	+1.5%	V	REFSEL=1x, REFLVL=10, AV_{DD} ≥ 2.5V
		–1.5%	2.5	+1.5%	V	REFSEL=1x, REFLVL=11, AV_{DD} ≥ 3.0V
			AV_{DD}			REFSEL=00, INMODE=0x
V_{EXT_REFP}	External Positive Reference Voltage	1.25		AV_{DD}	V	REFSEL=01, INMODE=0x
		1.25		AV_{DD}–0.5V	V	REFSEL=01, INMODE=1x
V_{EXT_REFN}	External Negative Reference Voltage	AV_{SS}	AV_{SS}	VREFP – 1.25V	V	
IDDVEXT	External Reference Active Current (included in IDDADCE)	20	40	55	µa	
C_{VREF}	V_{REF} Capacitance		1		µF	
V_{INANA}	Analog Input Range	VREFN		VREFP	V	
C_{IN}	Analog Input Capacitance			5	pF	
R_{IN}	Analog Input Resistance		750	2000	Ω	
T_S	Sampling Time[2]	0.2			µs	INMODE=0x
		0.8			µs	INMODE=1x; POWER=00
		2.0			µs	INMODE=1x; POWER=10
T_{S_TSENSE}	Sampling Time[2] for Temperature Sensor		24		µs	
$T_{S\_VDD/2}$	Sampling Time[2] for V_{DD}/2 Fixed Reference		24		µs	

Notes:
1. Data in the Typical column is from characterization at 3.0V and 25°C. These values are provided for design guidance only and are not tested in production.
2. T_S is applied twice if INMODE=10 and RESOLUT=1.
3. T_{SS} is applied twice if RESOLUT=1.