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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	eZ8
Core Size	8-Bit
Speed	24MHz
Connectivity	DALI, DMX, I²C, LINbus, SPI, UART/USART, USB
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	67
Program Memory Size	60KB (60K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3.75K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 12x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f6082at024xk2246

1.4.4. Clock System

The clock system generates a System Clock, a low-frequency Peripheral Clock, and the Watchdog Timer Oscillator. It is comprised of:

- Watchdog Timer Oscillator (WTO).
- 32.768kHz Internal Precision Oscillator (IPO).
- Low Frequency Crystal Oscillator (LFXO) which is a low-power oscillator optimized for use with a 32.768kHz watch crystal. The IPO and LFXO can be used as clock sources for the Real-Time Clock (RTC), Liquid Crystal Display (LCD) and Timers in any mode, and as the reference clock for the Frequency Locked Loop (FLL).
- High Frequency Crystal Oscillator (HFXO) that provides highly accurate clock frequencies using an external crystal or ceramic resonator.
- Phase Locked Loop (PLL) which is clocked by the HFXO and can be selected as a system clock and/or as the USB clock.
- Digitally Controlled Oscillator (DCO).
- Frequency Locked Loop (FLL). The reference clock for the FLL can be either an Internal Precision Oscillator (IPO) or a Low Frequency Crystal Oscillator. The FLL, in conjunction with the DCO can be configured to generate system clock frequencies from 1 to 24MHz.

1.4.5. 12-Bit Analog-to-Digital Converter

The Analog-to-Digital Converter (ADC) converts an analog input signal to a 12-bit binary number. The ADC supports up to eight analog input sources multiplexed with GPIO ports. It is configurable for internal or external voltage reference and single-ended or differential inputs.

1.4.6. 12-Bit Digital-to-Analog Converter

The Digital-to-Analog Converter (DAC) converts a 12-bit digital code to an analog output voltage The DAC supports both internal and external references.

1.4.7. Low-Power Operational Amplifiers

Two low-power operational amplifiers (Op Amps) are provided: Op Amp A and Op Amp B. Op Amp A is a low-power, general-purpose operational amplifier with optional internal programmable gain settings. Op Amp B is a low-power, general-purpose operational amplifier that can optionally be internally configured as a current source/sink. Each Op Amp output can be internally routed to the ADC, a comparator, or an output pin. These op amps can function in all operating modes, including Stop Mode.

Table 20. Port Alternate Function Mapping (Z8Fxx82 64-Pin Parts) (Continued)

Port	Pin	Mnemonic	Alternate Function Description	Alternate Function Set Subregisters
Port B[1]	PB0	Reserved		AFS1[0]: 0
		ANA0/AMPAOUT	ADC Analog Input/OpAmp A Output	AFS1[0]: 1
	PB1	Reserved		AFS1[1]: 0
		ANA1/AMPAINN	ADC Analog Input/OpAmp A Input (N)	AFS1[1]: 1
	PB2	Reserved		AFS1[2]: 0
		ANA2/AMPAINP	ADC Analog Input/OpAmp A Input (P)	AFS1[2]: 1
	PB3	Reserved		AFS1[3]: 0
		V_{REF}–	Voltage Reference (M)	AFS1[3]: 1
	PB4	Reserved		AFS1[4]: 0
		V_{REF}+	Voltage Reference (P)	AFS1[4]: 1
	PB5	Reserved		AFS1[5]: 0
		ANA9	ADC Analog Input	AFS1[5]: 1
Port C[2]	PC0	Reserved		AFS1[0]: 0, AFS2[0]: 0
		ANA4/VBIAS/ C0INP	ADC or Voltage Bias with low current drive capability or Comparator 0 Input (P)	AFS1[0]: 1, AFS2[0]: 0
		Reserved		AFS1[0]: x, AFS2[0]: 1
	PC1	MISO0	SPI 0 Master In/Slave Out	AFS1[1]: 0, AFS2[1]: 0
		ANA5/C0INN	ADC or Comparator 0 Input (N)	AFS1[1]: 1, AFS2[1]: 0
		Reserved		AFS1[1]: x, AFS2[1]: 1
	PC2	$\overline{SS0}$	SPI 0 Slave Select	AFS1[2]: 0, AFS2[2]: 0
		ANA3	ADC Analog Input	AFS1[2]: 1, AFS2[2]: 0
		Reserved		AFS1[2]: x, AFS2[2]: 1
	PC3	MISO0	SPI 0 Master In/Slave Out	AFS1[3]: 0, AFS2[3]: 0
		ANA11/DAC	ADC or DAC	AFS1[3]: 1, AFS2[3]: 0
		C0OUT	Comparator 0 Output	AFS1[3]: 0, AFS2[3]: 1
		Reserved		AFS1[3]: 1, AFS2[3]: 1

Notes
1. Because there are at most two choices of alternate function for some pins of Ports A, B, D, F, G and H, the Alternate Function Set register AFS2 is not implemented. Additionally, alternate function selection, as described in the Port A–J Alternate Function Subregisters (see page 88), must also be enabled.
2. The alternate function selection for Port C, as described in the Port A–J Alternate Function Subregisters (see page 88), must also be enabled.
3. Because there is only a single alternate function for each Port J pin, the Alternate Function Set registers are not implemented for Port J. Additionally, alternate function selection, as described in the Port A–J Alternate Function Subregisters (see page 88), must also be enabled.

System Clock. The WTO is enabled automatically to allow the recovery. Although this oscillator runs at a much slower speed than the original system clock, the CPU continues to operate allowing execution of a clock failure vector and software routines that either remedy the oscillator failure or issue a failure alert. This automatic switch-over is not available if WTO is the System Clock source.

The System Clock source failure detection circuitry asserts if the System Clock frequency drops below 1 kHz ±50%. If an external signal is selected as the System Clock source, it is possible that a very slow but nonfailing clock can generate a failure condition. Under these conditions, do not enable the System Clock failure circuitry (SCKFEN should be cleared).

8.3.2. Watchdog Timer Failure

In the event of a Watchdog Timer Oscillator (WTO) failure, a similar nonmaskable interrupt-like event is issued. This event does not trigger an attendant clock switch-over, but alerts the CPU of the failure. After a Watchdog Timer failure, it is no longer possible to detect a System Clock failure. The failure detection circuitry does not function if the Watchdog Timer is used as the System Clock. In this case, it is necessary to disable the detection circuitry by clearing WTOFEN.

The WTO failure-detection circuit counts system clocks while looking for a Watchdog Timer clock. The logic counts 8004 system clock cycles before determining that a failure has occurred. The system clock rate determines the speed at which the Watchdog Timer failure can be detected. A very slow system clock results in very slow detection times.

8.4. High Frequency Crystal Oscillator

The products in the F6482 Series contain an on-chip High Frequency Crystal Oscillator (HFXO) for use with external crystals with 1 MHz to 24 MHz frequencies. HFXO features include:

- Optimized for low current consumption
- Selectable as System Clock
- Selectable as the PLL reference clock, which in turn, can generate System Clock and/or generate clocking for the USB

Alternatively, the X_{IN} input pin can also accept a 1 MHz–24MHz CMOS-level clock input signal. If an external clock generator is used, the X_{OUT} pin must be left unconnected.

Note: Although the X_{IN} pin can be used as an main system clock input for an external clock generator, configuring PA0 as CLKIN is better suited for such use. To learn more, see the System Clock Selection section on page 98).

8.4.1. Operating Modes

The HFXO and external clock drive support three frequency bands:

- Low gain for use with medium frequency crystals, ceramic resonators or external clock drive (1MHz to 8MHz)
- Medium gain for use with medium frequency crystals, ceramic resonators or external clock drive (> 8MHz to 16MHz)
- Maximum gain for use with high-frequency crystals or external clock drive (> 16MHz to 24MHz)

The HFXO and external clock drive band is selected using HXFOBAND in the CLKCTL2 Register.

8.4.2. HFXO Operation

HFXOEN in the CLKCTL2 Register controls whether the HFXO is enabled. During System Reset, HFXOEN is cleared, disabling the HFXO. When user code sets HFXOEN to enable the crystal oscillator, it should also check that the HFXO is stable, by reading HFXORDY, before using it as the PLL clock source or selecting the HFXO as System Clock. HFXORDY is cleared when the HFXO is disabled.

Figure 12 shows a recommended configuration for connection with external load capacitors and a fundamental-mode, parallel-resonant crystal operating. See the Electrical Characteristics chapter on page 598 for additional details regarding the characteristics of the HFXO. Printed circuit board layout should minimize crystal pin parasitic capacitance.

Table 73. Triggered One-Shot Mode Initialization Example (Continued)

Register	Value	Comment
T0H	00h	Timer starting value=0001h.
T0L	01h	
T0RH	ABh	Timer reload value=ABCDh.
T0RL	CDh	
PAADDR	02h	Selects Port A Alternate Function Register.
PACTL[1:0]	11b	PACTL[0] enables Timer 0 Input Alternate function if also selected by the Alternate Function Set 1 Register. PACTL[1] enables Timer 0 Output Alternate function if also selected by the Alternate Function Set 1 Register.
PAADDR	07h	Selects Port A Alternate Function Set 1 Register.
PACTL[1:0]	00b	PACTL[0] enables Timer 0 Input Alternate function. PACTL[1] enables Timer 0 Output Alternate function.
ESDADDR	10h	Selects the Timer 0 Input 0 Event System Destination.
ESDCTL	00h	Disconnects the Event System Input0 to Timer 0.
IRQ0ENH[5]	0b	Disables the Timer 0 interrupt.
IRQ0ENL[5]	0b	
T0CTL1	83h	TEN=1 enables the timer. All other bits remain in their appropriate settings.

Note: After receiving an input trigger, Timer 0 will:
1. Count ABCDh timer clocks.
2. Upon Timer 0 reload, generate a single clock cycle active High output pulse on the Timer 0 Output.
3. Wait for the next input trigger event.

10.1.3.3. Dual Input Triggered One-Shot Mode

In Dual Input Triggered One-Shot Mode (TMODE=1010), the first to arrive of the timer Input 0 or Input 1 signals triggers counting. In addition, the input that was first to arrive is recorded by the timer for later use in interrupt and output generation. Two timer output options and four interrupt options are available. Previous and current timer input triggers can be used in the interrupt control. If a trigger event occurs while counting, INPCAP is set to indicate that the interrupt is due to the trigger event. If a reload occurs, INPCAP is cleared to indicate that the interrupt is not due to a trigger event. The timer operates in the following sequence:

1. The Timer idles until a trigger is received. Due to the assertion of an input, both inputs must initially be deasserted to receive a new trigger. The Timer trigger, in essence the first to arrive of the timer Input 0 and Input 1 signals, is taken from the GPIO port pin timer input alternate function or from the Event System. If required, enable the Noise Filter and set the Noise Filter control by writing to the relevant bits in the Noise Filter Control Register. The TPOL bit in the Timer Control 1 Register selects whether the

Table 139. UART-LDD Baud Rates, 19.99848 MHz System Clock

Applicable Rate (kHz)	BRG Divisor (Decimal)	Actual Rate (kHz)	Error (%)	Applicable Rate (kHz)	BRG Divisor (Decimal)	Actual Rate (kHz)	Error (%)
1250.0	1	1250.0	–0.06	9.60	130	9.61	0.10
625.0	2	625.0	–0.06	4.80	260	4.81	0.10
250.0	5	250.0	–0.06	2.40	521	2.40	–0.09
115.2	11	113.6	–1.41	1.20	1042	1.20	0.01
57.6	22	56.79	–1.41	0.60	2083	0.60	0.01
38.4	33	37.86	–1.41	0.30	4167	0.30	0.01
19.2	65	19.2	0.10				

Table 140. UART-LDD Baud Rates, 10.0 MHz System Clock

Applicable Rate (kHz)	BRG Divisor (Decimal)	Actual Rate (kHz)	Error (%)	Applicable Rate (kHz)	BRG Divisor (Decimal)	Actual Rate (kHz)	Error (%)
1250.0	N/A	N/A	N/A	9.60	65	9.62	0.16
625.0	1	625.0	0.00	4.80	130	4.81	0.16
250.0	3	208.3	–16.67	2.40	260	2.40	0.16
115.2	5	125.0	8.51	1.20	521	1.20	–0.03
57.6	11	56.8	–1.36	0.60	1042	0.60	–0.03
38.4	16	39.1	1.73	0.30	2083	0.30	0.2
19.2	33	18.9	–1.36				

Table 141. UART-LDD Baud Rates, 7.3728 MHz System Clock

Applicable Rate (kHz)	BRG Divisor (Decimal)	Actual Rate (kHz)	Error (%)	Applicable Rate (kHz)	BRG Divisor (Decimal)	Actual Rate (kHz)	Error (%)
1250.0	N/A	N/A	N/A	9.60	48	9.60	0.00
625.0	N/A	N/A	N/A	4.80	96	4.80	0.00
250.0	2	230.4	–7.84	2.40	192	2.40	0.00
115.2	4	115.2	0.00	1.20	384	1.20	0.00
57.6	8	57.6	0.00	0.60	768	0.60	0.00
38.4	12	38.4	0.00	0.30	1536	0.30	0.00
19.2	24	19.2	0.00				

$$\text{SPI Baud Rate (bits/s)} = \frac{\text{System Clock Frequency (Hz)}}{2 \times \text{BRG[15:0]}}$$

The minimum baud rate is obtained by setting BRG[15:0] to 0000h for a clock divisor value of (2 x 65536=131072).

When the ESPI is disabled, the Baud Rate Generator can function as a basic 16-bit timer with interrupt on time-out. Observe the following steps to configure the Baud Rate Generator as a timer with interrupt on time-out:

1. Disable the ESPI by clearing the ESPIEN1,0 bits in the ESPI Control Register.
2. Load the appropriate 16-bit count value into the ESPI Baud Rate High and Low Byte registers.
3. Enable the Baud Rate Generator timer function and associated interrupt by setting the BRGCTL bit in the ESPI Control Register to 1.

When configured as a general-purpose timer, the SPI BRG interrupt interval is calculated using the following equation:

$$\text{SPI BRG Interrupt Interval (s)} = \text{System Clock Period (s)} \times \text{BRG[15:0]}$$

15.4. ESPI Control Register Definitions

The ESPI control registers are defined in this section.

15.4.1. ESPI 0-1 Data Registers

The ESPI 0-1 Data Registers, shown in Table 144, address both the outgoing Transmit Data Registers and the incoming Receive Data Registers. Reads from an ESPI Data Register return the contents of the Receive Data Register. The Receive Data Register is updated with the contents of the Shift Register at the end of each transfer. Writes to an ESPI Data Register load the Transmit Data Register unless TDRE=0. Data is shifted out starting with bit 7. The last bit received resides in bit position 0. In either the Master or Slave modes, if TDRE=0, writes to this register are ignored.

When the character length is less than 8 bits (as set by the NUMBITS field in the ESPI Mode Register), the transmit character must be left-justified in the ESPI Data Register. A received character of less than 8 bits is right-justified (i.e., the last bit received is in bit position 0). For example, if the ESPI is configured for 4-bit characters, the transmit characters must be written to ESPIDATA[7:4] and the received characters are read from ESPIDATA[3:0].

- When the second DMA interrupt occurs, it indicates that the Nth byte has been received. Set the stop bit in the I2CCTL Register; this stop bit is polled by software to determine when the transaction is actually completed.
- Clear the DMAIF bit in the I2CMODE Register.

16.2.7.3. Slave Write Transaction with Data DMA

In a transaction in which the I^2C master/slave operates as a slave that receives data written by a master, the software must set the NAK bit after the (N–1)st byte has been received or during the reception of the last byte. As in the Master Read transaction described previously, the watermark DMA interrupt is used to notify software when the (N–1)st byte has been received.

- Configure the selected DMA channel for I^2C receive. The IEOB bit must be set in the DMAxCTL0 Register for the last buffer to be transferred. Typically, one buffer will be defined with a transfer length of N where N bytes are expected to be received from the master. The watermark is set to 1 by setting WMCNT to 0001 in the DMAxCNTH Register.
- The I^2C interrupt must be enabled in the interrupt controller to alert software of any I^2C error conditions.
- The I^2C master/slave must be configured as defined in a previous section describing SLAVE Mode transactions. The TXI bit in the I2CCTL Register must be cleared.
- When the SAM interrupt occurs, set the DMAIF bit in the I2CMODE Register.
- The DMA transfers the data to memory as it is received from the master.
- When the first DMA interrupt occurs indicating that the (N–1)st byte is received, the NAK bit must be set in the I2CCTL Register.
- When the second DMA interrupt occurs, it indicates that the Nth byte is received. A stop I^2C interrupt occurs (SPRS bit set in the I2CSTAT Register) when the master issues the stop (or restart) condition.
- Clear the DMAIF bit in the I2CMODE Register.

16.2.7.4. Slave Read Transaction with Data DMA

In this transaction the I^2C master/slave operates as a slave, sending data to the master.

- Configure the selected DMA channel for I^2C transmit. The IEOB bit must be set in the DMAxCTL0 Register for the last buffer to be transferred. Typically, a single buffer with a transfer length of N is defined.
- The I^2C interrupt must be enabled in the interrupt controller to alert software of any I^2C error conditions. A Not Acknowledge interrupt occurs on the last byte transferred.
- The I^2C master/slave must be configured as defined in the sections above describing SLAVE Mode transactions. The TXI bit in the I2CCTL Register must be cleared.

Chapter 17. Universal Serial Bus

The Z8 Encore! Universal Serial Bus (USB) Module provides USB full-speed device functionality with eight USB endpoints. It includes the following features:

- Full-speed (12Mbps) USB device
- IN endpoint 0 and OUT endpoint 0 control endpoints
- IN endpoints 1–3 and OUT endpoints 1–3 capable of bulk and interrupt transfers
- USB Suspend, host-initiated Resume, and device-initiated Resume (remote wake-up)
- USB clock of 48MHz from internal PLL or external clock source; see the Clock System chapter on page 96 to learn more
- 512 bytes of dedicated USB endpoint buffer memory; each endpoint buffer memory can be configured as 8, 16, 32, or 64 bytes
- Integrated full-speed USB PHY with integrated pull-up resistor
- Support for two DMA channels

17.1. Architecture

The architecture, shown in Figure 54,consists of a USB device, USB endpoint buffer memory, and a USB PHY.

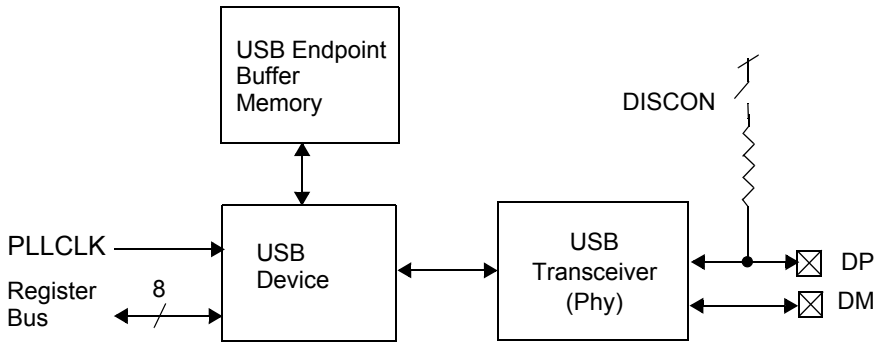

Figure 54. USB Block Diagram

Table 208. DMA Source Address Low Subregister (DMAxSRCL)

Bit	7	6	5	4	3	2	1	0
Field	SRCL							
Reset	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	If DMASA = 1h in the DMAxSA Register, accessible through the DMA 0–3 Subregister							

Bit	Description
[7:0] SRCL	**Source Address Low** 00–FF: Lower 8-bits of the DMA source address.

18.3.5. DMA Destination Address Subregisters

The DMAxDSTH and DMAxDSTL subregisters, shown in Tables 209 and 210, combine to form the 12-bit destination address for the DMA transaction. Upon each byte transfer, the destination address is updated based on the DSTCTL configuration in the DMAx Control 0 Subregister.

Table 209. DMA Destination Address High Subregister (DMAxDSTH)

Bit	7	6	5	4	3	2	1	0
Field	Reserved				DSTH			
Reset	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Address	If DMASA = 2h in the DMAxSA Register, accessible through the DMA 0–3 Subregister							

Bit	Description
[7:4]	**Reserved** These bits are reserved and must be programmed to 0000.
[3:0] DSTH	**Destination Address High** 0–F: Upper 4 bits of the DMA destination address.

19.6. Event System Register Definitions

Four register addresses provide access to the Event System subregisters that control source and destination selection for each Event System channel. Table 219 lists these Event System registers and subregisters.

Table 219. Event System Registers and Subregisters

Event System Source Selection Registers and Subregisters		
Register Mnemonic	**Address**	**Register Name**
ESSSA	F98h	Event System Source Subaddress Register
ESSSD	F99h	Event System Source Subdata Register
Subregister Mnemonic	**Subregister Address***	**Subregister Name**
ESCHxSRC	0–7h	Event System Channel 0–7 Source subregisters

Event System Destination Selection Registers and Subregisters		
Register Mnemonic	**Address**	**Register Name**
ESDSA	F9Ah	Event System Destination Subaddress Register
ESDSD	F9Bh	Event System Destination Subdata Register
Subregister Mnemonic	**Subregister Address***	**Subregister Name**
ESCHDSTx	0–3Fh	Event System Destination 0–3F Channel subregisters

Note: *The ESSSA Register contains the ESCHxSRC Subregister address; the ESDSA Register contains the ESCHDSTx Subregister address.

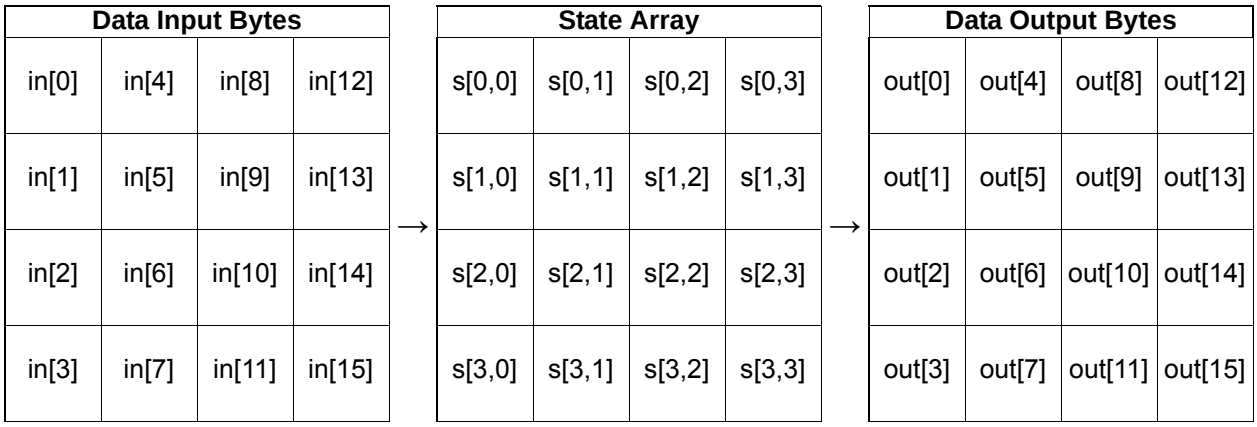

Figure 63. AES State Array Input and Output

Three status flags in the AESSTAT Register, KEYLD, IVLD and DATALD, indicate whether the AES accelerator has been properly setup with the 16-byte loads of the AESKEY, AESIV and AESDATA registers. The IVLD flag is only applicable when using the CBC or OFB confidentiality modes. Disabling the AES accelerator clears the load status flags, IVLD, KEYLD and DATALD. IVLD or KEYLD are also cleared during reloading of the respective registers. DATALD is cleared upon completion of an encryption/decryption operation in conjunction with clearing START/BUSY in the AESCTL Register.

The encryption/decryption operation can be initiated either manually or with auto-start. Setting the START/BUSY bit will manually start the requested encryption/decryption regardless of the load status flag settings. If the AUTODIS bit is cleared, encryption/decryption will auto-start when the 16th byte of data is loaded only if the KEYLD and IVLD (if applicable) are set. Table 226 describes conditions required to auto-start:

Table 226. Register Bit Settings for Auto-Start

AUTODIS	Mode	IVLD	KEYLD	DATALD	Auto-Start
0	01 (OFB) or 10 (CBC)	0	X	X	NO
0		0	0	X	NO
0		1	1	0	NO
0		1	1	1	YES
0	00 (ECB)	X	0	X	NO
0		X	1	0	NO
0		X	1	1	YES
1	X	X	X	X	NO

voltage reference buffer, and a 12-bit SAR ADC. The ADC digitizes the signal on a selected channel and stores the digitized data in the ADC data registers. In environments with high electrical noise, an external RC filter must be added at the input pins to reduce high-frequency noise.

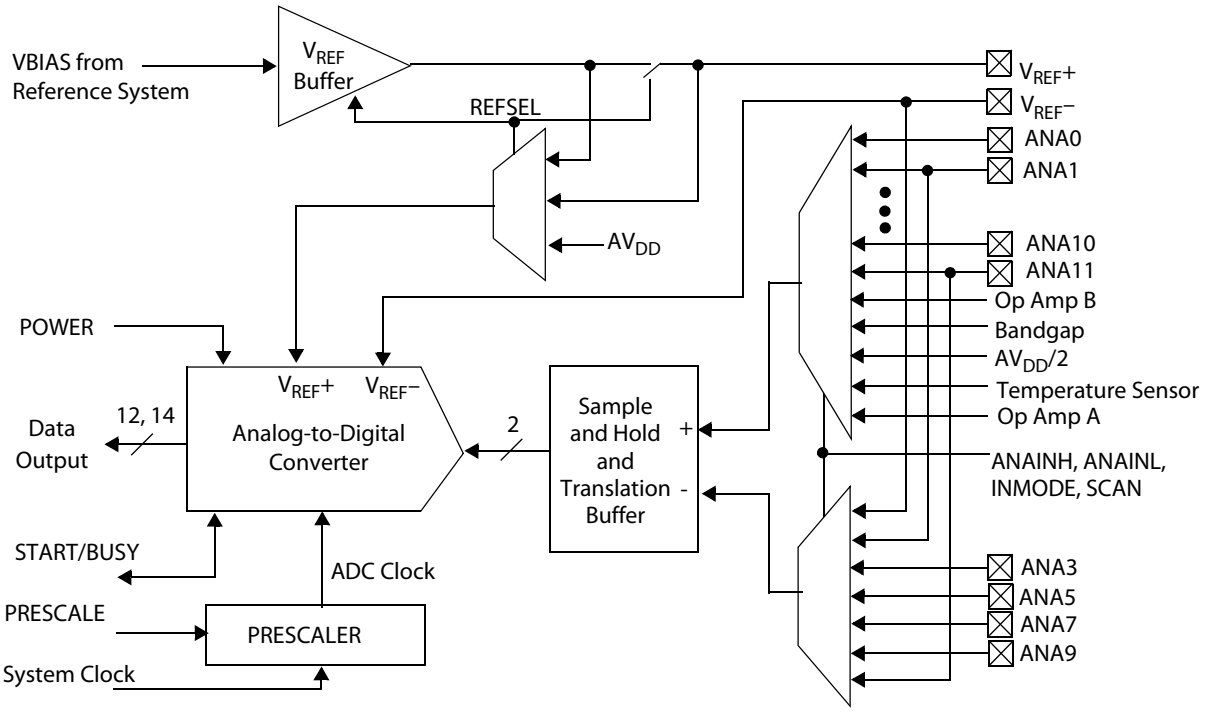

Figure 70. Analog-to-Digital Converter Block Diagram

21.2. Operation

The ADC converts the analog input, ANAx, to a digital representation. The ADC has selectable input modes, resolution, data format, conversion options, power options, window detection, and voltage reference options. The ADC can be serviced by the DMA.

Assuming zero gain and offset errors, any voltage outside the ADC input limits of V_{REF-} and V_{REF+} returns the minimum ADC output code or the maximum ADC output code, respectively.

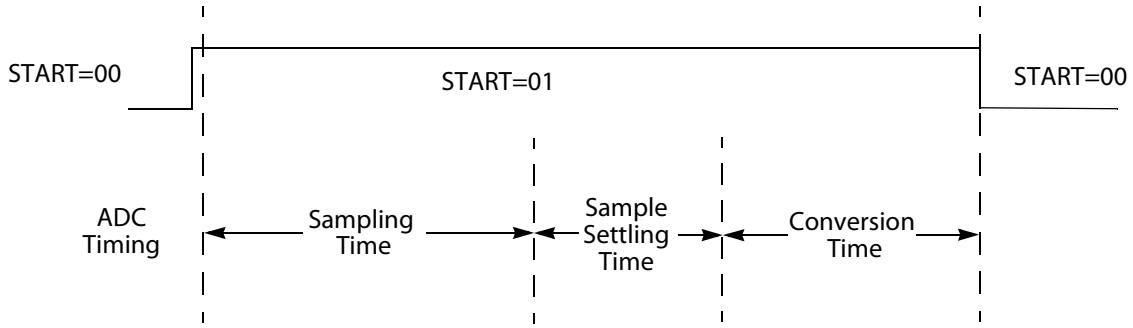

Figure 74. ADC Timing Diagram for 12-Bit Resolution

21.2.6.2. 2-Pass 14-Bit Resolution Timing

Each 2-pass 14-bit resolution (RESOLUT=1) ADC measurement consists of up to 5 phases:

1. Input sampling time as defined by the ST bit, is a function of source impedance and the desired accuracy, as discussed later in this section. The minimum input sampling period is 200ns for balanced differential input mode (INMODE=01), and 800ns with the input translation buffer enabled (INMODE=10, 11). For balanced differential input mode, ST occurs twice during a conversion.
2. Sample-and-hold amplifier settling time, as defined by the SST bit, is a minimum of 200ns for balanced differential mode (INMODE=01), and 1000ns with the input translation buffer enabled (INMODE=10, 11). SST occurs twice for all input modes.
3. Sample conversion time is 15 ADC clock cycles with a maximum frequency of 4.0MHz. Sample conversion occurs twice for all conversion modes.

Figure 75 shows the timing of a 2-pass 14-bit ADC conversion with (INMODE=10, 11), and Figure 76 shows the timing of a 2-pass 14-bit ADC conversion with (INMODE=01).

21.2.8. ADC Interrupts and DMA

The ADC can generate an interrupt request upon each new ADC result for any completed conversion or calibration (START= 01, 10, 11). The ADC can also generate an interrupt if the conversion result is outside the range defined by the window threshold registers (ADCUWINH, ADCUWINL, ADCLINH, ADCLWINL). Use the IRQ bit in the ADC Control 0 Register to select whether interrupts are generated due to only exceeding the window thresholds or due to both exceeding the window thresholds and end of convert. An interrupt request that is pending when the ADC is disabled or idle (ready) is not automatically cleared.

The ADC will assert a DMA request upon each new ADC result, and will deassert a DMA request whenever the ADCD_L Register (DMACTL=0) or ADCD_H Register (DMACTL=1) is read by the DMA or software. When DMACTL=0, the typical goal is to transfer both data bytes, and the DMA is configured to have fixed word address control for the DMA source address; the source address is configured to be the ADCD_H Register address. When DMACTL=1, the typical goal is to transfer only the most significant data byte, and the DMA is configured to have fixed address control for the DMA source address; the source address is configured to be the ADCD_H Register address.

If starting a new ADC conversion and DMA transfer sequence, reading the ADC_L Register (DMACTL=0) or the ADC_H Register (DMACTL=1) prior to enabling DMA and starting conversion ensures that any residual ADC DMA request from prior ADC activity is deasserted. A DMA request is not asserted upon the completion of an offset or gain calibration.

21.2.9. Calibration and Compensation

Both gain and offset calibration can be performed in situ to achieve even higher accuracy than specified in the Electrical Characteristics chapter on page 598. These calibration operations are performed using the current ADC configuration, as defined by the INMODE, PRESCALE, ST, and SST bits. After these parameters are reconfigured, initiating calibration prior to performing conversions can optimize results. Only initiate calibration when continuous conversion is not selected (i.e., CONTCONV = 0).

Offset calibration is performed when the START bits are written to 10. Prior to initiating offset calibration, 14-bit resolution must be selected by setting RESOLUT = 1. The offset result can be used for both 12-bit and 14-bit resolution conversions. The calibration is complete when START is cleared to 00. The offset calibration result is stored in the OFFSET field in the ADCOFF Register as a two’s-complement value, and is automatically applied to compensate subsequent conversions by hardware. OFFSET can be read by software and can be stored and rewritten any time to the ADCOFF Register to allow consistent usage of offset calibrations. For example, when using multiple input modes, each mode can exhibit a unique offset calibration value.

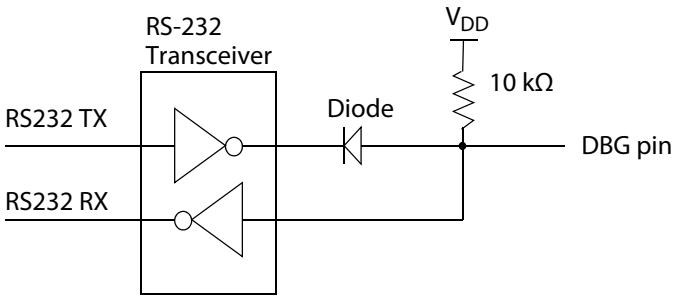

Figure 98. Interfacing the On-Chip Debugger's DBG Pin with an RS-232 Interface, #1 of 2

Caution: For proper operation of the F6482 Series device, all power pins (V_{DD} and AV_{DD}) must be supplied with power, and all ground pins (V_{SS} and AV_{SS}) must be properly grounded. The DBG pin should always be connected to V_{DD} through an external pull-up resistor.

The Serial Smart Cable (SSC) does not work with the F6482 device series because it does not fully support the silicon OCD. During external clock switching, the OCD sends a break command to the SSC. This causes the SSC to disconnect from the target and terminate the debug session. You must then reconnect to the target again. Use the Opto-Isolated USB, USB, or Ethernet Smart Cables when using in conjunction with ZDSII.

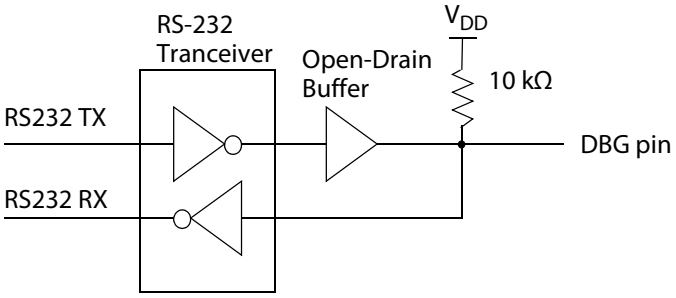

Figure 99. Interfacing the On-Chip Debugger's DBG Pin with an RS-232 Interface, #2 of 2

The majority of the OCD commands remain disabled when the eZ8 CPU is looping on a BRK instruction. The eZ8 CPU must be in Debug Mode before these commands can be issued.

30.2.9.1. Breakpoints in Flash Memory

The BRK instruction is op code 00h, which corresponds to the fully programmed state of a byte in Flash memory. To implement a breakpoint, write 00h to the desired address, overwriting the current instruction. To remove a breakpoint, erase the corresponding page of Flash memory and reprogram with the original data.

30.2.10. OCD Counter Register

The On-Chip Debugger contains a multipurpose 16-bit counter register that can be used for the following tasks:

- Count system clock cycles between breakpoints
- Generate a BRK when it counts down to 0
- Generate a BRK when its value matches the Program Counter

When configured as a counter, the OCDCNTR Register starts counting when the On-Chip Debugger exits Debug Mode, and stops counting when it reenters Debug Mode or when it reaches the maximum count of FFFFh. The OCDCNTR Register automatically resets itself to 0000h when the OCD exits Debug Mode if it is configured to count clock cycles between breakpoints.

If the OCDCNTR Register is configured to generate a BRK when it counts down to zero, it will not be reset when the CPU starts running. The counter will start counting down toward zero when the On-Chip Debugger exits Debug Mode. If the On-Chip Debugger enters Debug Mode before the OCDCNTR Register counts down to zero, the OCDCNTR will stop counting.

If the OCDCNTR Register is configured to generate a BRK when the program counter matches the OCDCNTR Register, the OCDCNTR Register will not be reset when the CPU resumes executing and it will not be decremented when the CPU is running. A BRK will be generated when the program counter matches the value in the OCDCNTR Register before executing the instruction at the location of the program counter.

! **Caution:** The OCDCNTR Register is used by many of the OCD commands. It counts the number of bytes for the register and memory read/write commands. It retains the residual value when generating the CRC. If the OCDCNTR is used to generate a BRK, its value must be written as a final step before exiting Debug Mode.

Table 337. Analog-to-Digital Converter Electrical Characteristics and Timing (Continued)

		V_{DD}=1.8V to 3.6V T_A=–40°C to +85°C				
Symbol	**Parameter**	**Min**	**Typ***	**Max**	**Units**	**Conditions**
V_{INT_REF}	Internal Reference Voltage	–1.5%	1.25	+1.5%	V	REFSEL=1x, REFLVL=00, AV_{DD} ≥ 1.8V
		–1.5%	1.50	+1.5%	V	REFSEL=1x, REFLVL=01, AV_{DD} ≥ 2.0V
		–1.5%	2.0	+1.5%	V	REFSEL=1x, REFLVL=10, AV_{DD} ≥ 2.5V
		–1.5%	2.5	+1.5%	V	REFSEL=1x, REFLVL=11, AV_{DD} ≥ 3.0V
			AV_{DD}			REFSEL=00, INMODE=0x
V_{EXT_REFP}	External Positive Reference Voltage	1.25		AV_{DD}	V	REFSEL=01, INMODE=0x
		1.25		AV_{DD}–0.5V	V	REFSEL=01, INMODE=1x
V_{EXT_REFN}	External Negative Reference Voltage	AV_{SS}	AV_{SS}	VREFP – 1.25V	V	
IDDVEXT	External Reference Active Current (included in IDDADCE)	20	40	55	µa	
C_{VREF}	V_{REF} Capacitance		1		µF	
V_{INANA}	Analog Input Range	VREFN		VREFP	V	
C_{IN}	Analog Input Capacitance			5	pF	
R_{IN}	Analog Input Resistance		750	2000	Ω	
T_S	Sampling Time[2]	0.2			µs	INMODE=0x
		0.8			µs	INMODE=1x; POWER=00
		2.0			µs	INMODE=1x; POWER=10
T_{S_TSENSE}	Sampling Time[2] for Temperature Sensor		24		µs	
$T_{S\_VDD/2}$	Sampling Time[2] for V_{DD}/2 Fixed Reference		24		µs	

Notes:
1. Data in the Typical column is from characterization at 3.0V and 25°C. These values are provided for design guidance only and are not tested in production.
2. T_S is applied twice if INMODE=10 and RESOLUT=1.
3. T_{SS} is applied twice if RESOLUT=1.

33.4.9. Comparator

Table 339 presents electrical and timing data for the F6482 Series' Comparator function.

Table 339. Comparator Electrical Characteristics

		T_A = –40°C to +85°C V_{DD} = 1.8V to 3.6V				
Symbol	**Parameter**	**Min**	**Typ***	**Max**	**Units**	**Conditions**
I_{DD}COMP	Comparator Active Current		0.2		µA	CPOWER=00
			1		µA	CPOWER=01
			4		µA	CPOWER=10
			27		µA	CPOWER=11
V_{ICM}	Input Common Mode Voltage	V_{SS}		V_{DD}	V	
V_{OS}	Input DC Offset		±2	±5	mV	
V_{HYS}	Input Hysteresis		0		mV	HYST=0x
			15		mV	HYST=10
			40		mV	HYST=11
T_{PROP}	Propagation Delay		5		µs	CPOWER=00
			1.5		µs	CPOWER=01
			700		ns	CPOWER=10
			150		ns	CPOWER=11
T_{WAKE}	Time for Wake up		2	5	µs	

Note: *Data in the Typical column is from characterization at 3.0V and 25°C. These values are provided for design guidance only and are not tested in production.