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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	eZ8
Core Size	8-Bit
Speed	24MHz
Connectivity	DALI, DMX, I²C, LINbus, SPI, UART/USART, USB
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	67
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3.75K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 12x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f6482at024xk

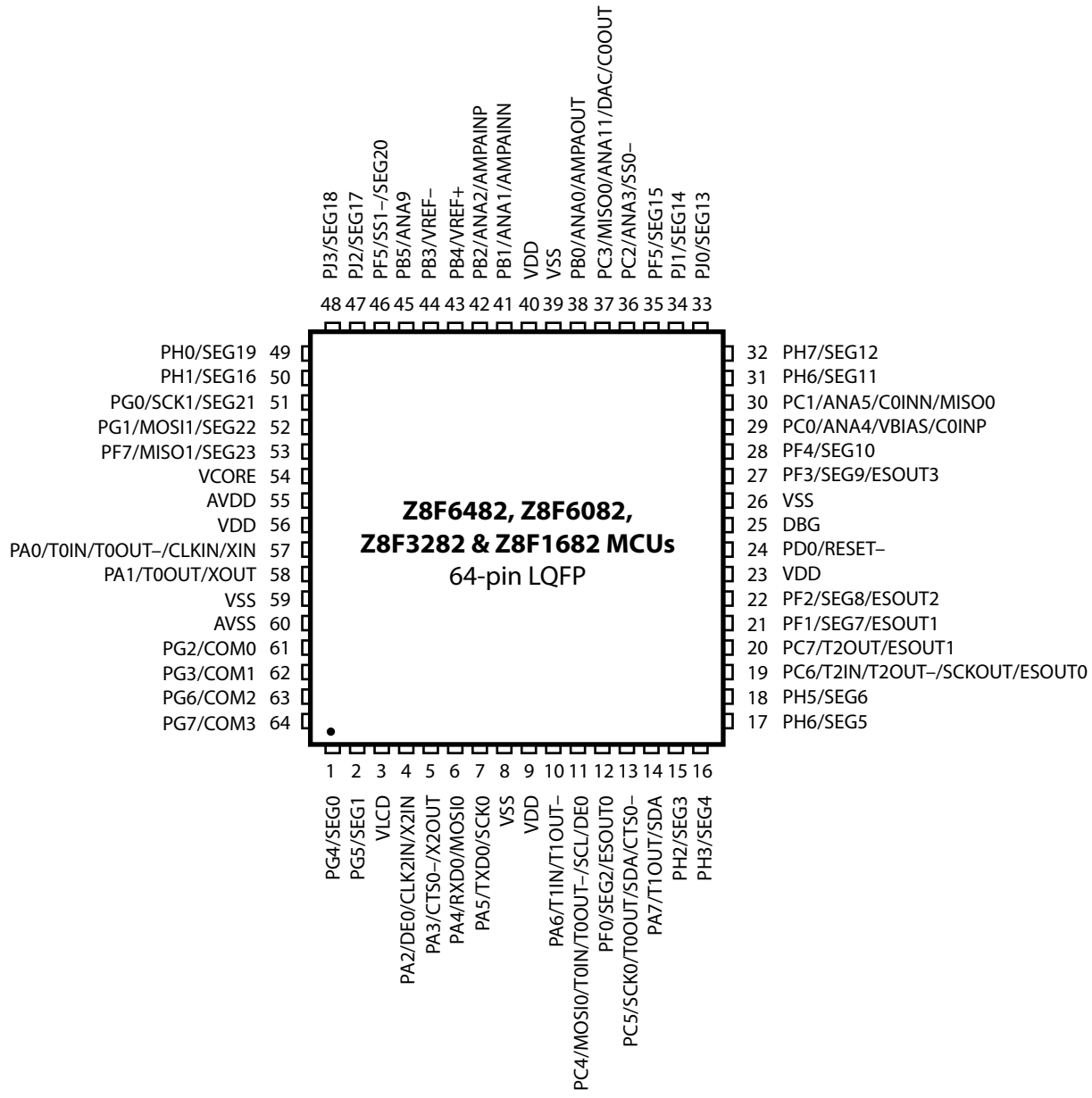

Figure 5. Z8F6482, Z8F6082, Z8F3282 & Z8F1682 MCUs, 64-Pin Low-Profile Quad Flat Package (LQFP)

5.3.3. Stop-Mode Recovery Using GPIO Port Pin Transition

Many of the GPIO Port pins can be configured as a Stop-Mode Recovery input source. Which GPIO can be configured as a Stop-Mode Recovery input source is described in the General-Purpose Input/Output chapter on page 55. On any GPIO pin enabled as a Stop-Mode Recovery source, a change in the input pin value (from High to Low or from Low to High) initiates Stop-Mode Recovery. In the Reset Status Register, the STOP bit is set to 1.

If the GPIO is also configured as an interrupt source, an interrupt will occur once interrupts are reenabled.

! Caution: In Stop Mode, the GPIO Port Input Data registers (PxIN) are disabled. The Port Input Data registers record the Port transition only if the signal stays on the Port pin until the end of the Stop-Mode Recovery delay. As a result, short pulses on the Port pin can initiate Stop-Mode Recovery without being written to the Port Input Data Register or without initiating an interrupt (if enabled for that pin).

5.3.4. Stop-Mode Recovery Using External $\overline{\text{RESET}}$ Pin

When the F6482 Series MCU is in Stop Mode and the external $\overline{\text{RESET}}$ pin is driven Low, a System Reset occurs. Because of a glitch filter operating on the $\overline{\text{RESET}}$ pin, the Low pulse must be greater than the minimum width specified, or it is ignored. For details, see the Electrical Characteristics chapter on page 598.

5.4. Low-Voltage Detection

In addition to the VBO Reset described earlier, it is also possible to generate an interrupt when the supply voltage drops below a user-selected value. To learn more about the available Low-Voltage Detection (LVD) threshold levels, see the Flash Option Bits chapter on page 540.

When the supply voltage drops below the LVD threshold, the LVD bit of the RSTSTAT Register is set to 1. This bit remains 1 until the low-voltage condition elapses. Reading or writing this bit does not clear it. The LVD circuit can also generate an interrupt when enabled; see the Interrupt Controller chapter on page 127. The LVD is not latched, so enabling the interrupt is the only way to guarantee detection of a transient low-voltage event.

The LVD circuit is either enabled or disabled by the Power Control Register bit 4. To learn more, see the Power Control Register Definitions section on page 52.

Table 19. Port Alternate Function Mapping (Z8Fxx81 64-Pin Parts)

Port	Pin	Mnemonic	Alternate Function Description	Alternate Function Set Subregisters
Port A[1]	PA0	T0IN/$\overline{\text{T0OUT}}$	Timer 0 Input/Timer 0 Output Complement	AFS1[0]: 0
		CLKIN	External Clock Input	AFS1[0]: 1
	PA1	T0OUT	Timer 0 Output	AFS1[1]: 0
		Reserved		AFS1[1]: 1
	PA2	DE0	UART 0 Driver Enable	AFS1[2]: 0
		CLK2IN	External Clock 2 Input	AFS1[2]: 1
	PA3	$\overline{\text{CTS0}}$	UART 0 Clear to Send	AFS1[3]: 0
		Reserved		AFS1[3]: 1
	PA4	RXD0/	UART 0 Receive Data	AFS1[4]: 0
		MOSI0	SPI 0 Master Out/Slave In	AFS1[4]: 1
	PA5	TXD0/	UART 0 Transmit Data	AFS1[5]: 0
		SCK0	SPI 0 Serial Clock	AFS1[5]: 1
	PA6	T1IN/$\overline{\text{T1OUT}}$	Timer 1 Input/Timer 1 Output Complement	AFS1[6]: 0
		SCL	I^2C Serial Clock	AFS1[6]: 1
	PA7	T1OUT	Timer 1 Output	AFS1[7]: 0
		SDA	I^2C Serial Data	AFS1[7]: 1

Notes
1. Because there are at most two choices of alternate function for some pins of Ports A, B, D, E and F, the Alternate Function Set register AFS2 is not implemented. Additionally, alternate function selection, as described in the Port A–J Alternate Function Subregisters (see page 88), must also be enabled.
2. The alternate function selection for Port C, as described in the Port A–J Alternate Function Subregisters (see page 88), must also be enabled.

Table 37. Common PLL Configurations for 48MHz PLLCLK (Continued)

PLL_{CLKIN} (MHz)	PLL_{RDIV}	PLL Core (MHz)	PLL_{NDIV}	VCO (MHz)	PLL_{ODIV}
6	1	3	31	96	1
6.4	2	2.133333	44	96	1
7.2	2	2.4	39	96	1
8	0	8	11	96	1
9	2	3	31	96	1
9.6	0	9.6	9	96	1
10	1	5	47	240	4
12	0	12	7	96	1
12.8	1	6.4	14	96	1
14.4	2	4.8	19	96	1
16	0	16	5	96	1
18	2	6	15	96	1
19.2	0	19.2	4	96	1
20	3	5	47	240	4
24	0	24	3	96	1

To avoid spurious PLL_{CLK} behavior when modifying PLLh divider ratios, write CLKCTLA and CLKCTLB only when the PLL is disabled.

8.11. Clock System Register Definitions

The Clock System registers enable and disable the various oscillator circuits, enable and disable the failure detection and recovery circuitry, and select clock sources for System Clock, Peripheral Clock, and PLL clock.

8.11.1. Clock Control 0 Register

The Clock Control 0 (CLKCTL0) Register, shown in Table 38, selects System Clock and System Clock division, enables/disables System Clock failure detection, and provides clock system register locking status and control. SCKSEL is reset by both System Reset and Stop-Mode Recovery.

Before writing CLKCTL0, the clock control registers must be unlocked as described in the Clock System Control Register Unlocking/Locking section on page 103.

! **Caution:** When the timer is operating on PCLK or the WTO, the timer clock is asynchronous to System Clock. To ensure error-free operation, disable the timer before modifying its operation (including changing the timer clock source).

When the Timer uses PCLK or the WTO and the Timer is enabled, any read from T*x*H or T*x*L is not recommended, because results can be unpredictable. Disable the Timer first, then read it. If capture, capture/compare, Capture Restart or demodulation mode is selected, any read from T*x*PWM0H, T*x*PWM0L, T*x*PWM1H, T*x*PWM1L, or T*x*STAT must be done after capture interrupt occurs, or results can be unpredictable. INPCAP in the Timer Control 0 Register has the same characteristics as these PWM registers. When the Timer clock selection is System Clock, registers can be written/read at any time.

10.1.2. Low-Power Modes

Timers can operate in both Halt Mode and Stop Mode. This section discusses each of these low-power modes.

10.1.2.1. Operation in Halt Mode

When the eZ8 CPU enters Halt Mode, the Timer will continue to operate if enabled. To minimize current in Halt Mode, the Timer can be disabled by clearing the TEN control bit. The Noise Filter, if enabled, will also continue to operate in Halt Mode and rejects any noise on the Timer Input 0.

10.1.2.2. Operation in Stop Mode

When the eZ8 CPU enters Stop Mode, the Timer continues to operate if enabled and PCLK or the WTO is selected as the timer clock. In Stop Mode, the timer interrupt (if enabled) automatically initiates a Stop-Mode Recovery and generates an interrupt request. In the Reset Status Register, the stop bit is set to 1. Also, timer interrupt request bit in Interrupt Request 0 Register is set. Following completion of the Stop-Mode Recovery, if interrupts are enabled, the CPU responds to the interrupt request by fetching the timer interrupt vector. The Noise Filter, if enabled, will also continue to operate in Stop Mode and rejects any noise on the Timer Input 0.

If System Clock is chosen as the timer clock, the Timer ceases to operate as System Clock is disabled in Stop Mode. In this case the registers are not reset and operation will resume after Stop-Mode Recovery occurs.

10.1.2.3. Power Reduction During Operation

Clearing TEN will inhibit clocking of the Timer. The CPU can still read/write registers when TEN is cleared.

Bit	Description (Continued)
[6] TPOL (cont'd)	**PWM Dual Output Mode** 0: Timer Output is forced Low (0) and Timer Output Complement is forced High (1) when the timer is disabled. When enabled, the Timer Output is forced High (1) upon PWM count match and forced Low (0) upon Reload. When enabled, the Timer Output Complement is forced Low (0) upon PWM count match and forced High (1) upon Reload. The PWMD field in Timer Control 0 Register is a programmable delay to control the number of cycles time delay before the Timer Output and the Timer Output Complement is forced to High (1). 1: Timer Output is forced High (1) and Timer Output Complement is forced Low (0) when the timer is disabled. When enabled, the Timer Output is forced Low (0) upon PWM count match and forced High (1) upon Reload. When enabled, the Timer Output Complement is forced High (1) upon PWM count match and forced Low (0) upon Reload. The PWMD field in Timer Control 0 Register is a programmable delay to control the number of cycles time delay before the Timer Output and the Timer Output Complement is forced to Low (0). **Capture Restart Mode** 0: Count is captured on the rising edge of the Timer Input 0 signal. 1: Count is captured on the falling edge of the Timer Input 0 signal. **Comparator Counter Mode** When the timer is disabled, the Timer Output signal is set to the value of this bit. When the timer is enabled, the Timer Output signal is complemented upon timer reload. **Triggered One-Shot Mode and Dual Input Triggered One-Shot Mode** OUTCTL = 0 0: Timer counting is triggered on the rising edge of the Timer Input 0 signal. 1: Timer counting is triggered on the falling edge of the Timer Input 0 signal. OUTCTL = 1 0: Timer counting is triggered on the rising edge of the Timer Input 0 signal. 1: Reserved. **Demodulation Mode** This functionality applies only if TPOLHI bit in Timer Control 2 Register is 0. If TPOLHI bit is 1 then timer counting is triggered on any edge of the Timer Input 0 signal and the current count is captured on both edges. The current count is captured into PWM0 registers on rising edges and PWM1 registers on falling edges of the Timer Input 0 signal. 0: Timer counting is triggered on the rising edge of the Timer Input 0 signal. The current count is captured into PWM0 High and Low byte registers on subsequent rising edges of the Timer Input 0 signal. 1: Timer counting is triggered on the falling edge of the Timer Input 0 signal. The current count is captured into PWM1 High and Low byte registers on subsequent falling edges of the Timer Input 0 signal.

11.3. Capture/Compare Channel Operation

The Multi-Channel timer supports four Capture/Compare channels: CHA, CHB, CHC, and CHD. Each channel has the following features:

- A 16-bit Capture/Compare Register (MCTCHyH and MCTCHyL registers) used to capture input event times or to generate time intervals. Any user software update of the Capture/Compare Register value when the timer is running takes effect only at the end of the counting cycle, not immediately. The end of the counting cycle is when the counter transitions from the reload value to 0 (Count Modulo Mode) or from 1 to 0 (Count Up/Down Mode).
- A dedicated bidirectional GPIO pin (T4CHA, B, C, or D) and Event System input/output that can be configured for the input capture function or to generate an output compare match or one-shot pulse.

Each channel is configured to operate in either One-Shot Compare, Continuous Compare, PWM Output, or Capture Mode.

11.3.1. One-Shot Compare Operation

In One-Shot Compare operation, a channel interrupt is generated when the channel compare value matches the timer count. The channel event flag, CHyEF, is set in the Channel Status 1 Register (MCTCHS1) to identify the responsible channel. Then the channel is automatically disabled. The timer continues counting according to the programmed mode. The channel output (TOutA, B, C, or D) changes state for one system clock cycle (from Low to High then back to Low or High to Low then back to High as determined by the CHPOL bit) on match.

11.3.2. Continuous Compare Operation

In Continuous Compare operation, a channel interrupt is generated when the channel compare value matches the timer count. The channel event flag (CHyEF) is set in the Channel Status1 Register (MCTCHS1) and the channel remains enabled. The timer continues counting according to the programmed mode. The channel output (TOutA, B, C, or D) changes state (from Low to High then back to Low, or High to Low then back to High as determined by the CHPOL bit) on match. For proper operation, configure the CHPOL bit prior to setting the CHEN bit.

11.3.3. PWM Output Operation

In PWM Output operation, the timer generates a PWM output signal on the channel output (TOutA, B, C, or D). The channel output toggles whenever the timer count matches the channel compare value (defined in the MCTCHyH and MCTCHyL) registers. In addition, a channel interrupt is generated and the channel event flag is set in the status register. The timer continues counting according to its programmed mode.

Bit	Description (Continued)
[2] TDRE	**Transmitter Data Register Empty** This bit indicates that the Transmit Data Register is empty and ready for additional data. Writing to the Transmit Data Register resets this bit. 0: Do not write to the Transmit Data Register. 1: The Transmit Data Register is ready to receive an additional byte for transmission.
[1] TXE	**Transmitter Empty** This bit indicates that the Transmit Shift Register is empty and character transmission is finished. 0: Data is currently transmitting. 1: Transmission is complete.
[0] CTS	**Clear to Send Signal** When this bit is read it returns the level of the $\overline{\text{CTS}}$ signal. If LBEN=1, the $\overline{\text{CTS}}$ input signal is replaced by the internal Receive Data Available signal to provide flow control in a loopback mode. CTS only affects transmission if the CTSE bit=1.

Table 124. UART-LDD 0–1 Status 0 Registers, LIN Mode (U*x*STAT0)

Bit	7	6	5	4	3	2	1	0
Field	RDA	PLE	OE	FE	BRKD	TDRE	TXE	ATB
Reset	0	0	0	0	0	1	1	0
R/W	R	R	R	R	R	R	R	R
Address	U0STAT0 @ F41h, U1STAT0 @ F49h							

Note: R=read; *x* = 0,1.

Bit	Description
[7] RDA	**Receive Data Available** This bit indicates that the Receive Data Register has received data. Reading the Receive Data Register clears this bit. 0: The Receive Data Register is empty. 1: There is a byte in the Receive Data Register.
[6] PLE	**Physical Layer Error** This bit indicates that transmit and receive data do not match when a LIN slave or master is transmitting. This could be by a fault in the physical layer or multiple devices driving the bus simultaneously. Reading the Status 0 Register or the Receive Data Register clears this bit. 0: Transmit and Receive data match. 1: Transmit and Receive data do not match.

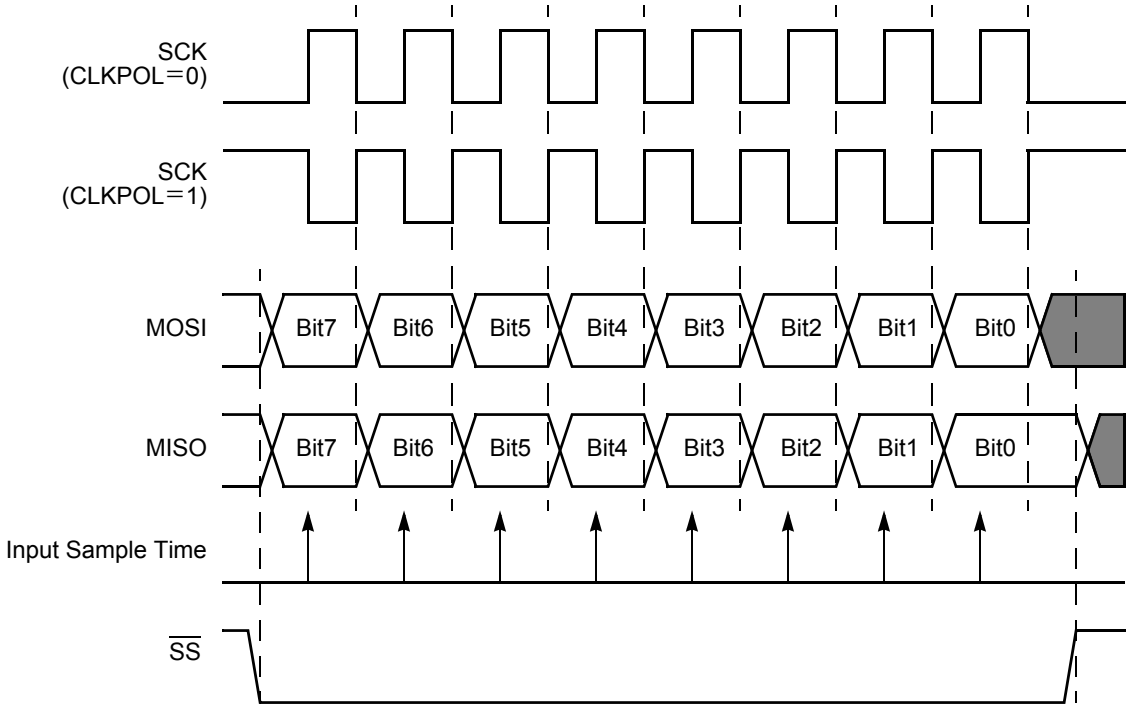

Figure 38. ESPI Timing when PHASE=0

15.3.2.2. Transfer Format When Phase Equals One

Figure 39 shows a timing diagram for an SPI-type transfer in which PHASE is 1. For SPI transfers, the clock only toggles during a character transfer. Two waveforms are depicted for SCK: one for CLKPOL=0 and another for CLKPOL=1.

Table 150 defines the valid ESPI states.

Table 150. ESPISTATE Values

ESPISTATE Value	Description
00_0000	Idle.
00_0001	Slave Wait for SCK.
00_0010	I^2S Slave Mode start delay.
00_0011	I^2S Slave Mode start delay.
01_0000	SPI Master Mode start delay.
11_0001	I^2S Master Mode start delay.
11_0010	I^2S Master Mode start delay.
10_1110	Bit 7 Receive.
10_1111	Bit 7 Transmit.
10_1100	Bit 6 Receive.
10_1101	Bit 6 Transmit.
10_1010	Bit 5 Receive.
10_1011	Bit 5 Transmit.
10_1000	Bit 4 Receive.
10_1001	Bit 4 Transmit.
10_0110	Bit 3 Receive.
10_0111	Bit 3 Transmit.
10_0100	Bit 2 Receive.
10_0101	Bit 2 Transmit.
10_0010	Bit 1 Receive.
10_0011	Bit 1 Transmit.
10_0000	Bit 0 Receive.
10_0001	Bit 0 Transmit.

15.4.7. ESPI 0-1 Baud Rate High and Low Byte Registers

The ESPI 0-1 Baud Rate High and Low Byte registers, shown in Tables 151 and 152, combine to form a 16-bit reload value, BRG[15:0], for the ESPI Baud Rate Generator. The ESPI baud rate is calculated using the following equation:

$$\text{SPI Baud Rate (bits/s)} = \frac{\text{System Clock Frequency (Hz)}}{2 \times \text{BRG[15:0]}}$$

Bit	Description (Continued)
[2] ARBLST	**Arbitration Lost** This bit is set when the I2C controller is enabled in MASTER Mode and loses arbitration (i.e., outputs a 1 on SDA and receives a 0 on SDA). The ARBLST bit clears when the I2CISTAT Register is read.
[1] SPRS	**Stop/Restart Condition Interrupt** This bit is set when the I2C controller is enabled in SLAVE Mode, and detects a stop or restart condition during a transaction directed to this slave. This bit clears when the I2CISTAT Register is read. Read the RSTR bit of the I2CSTATE Register to determine whether the interrupt was caused by a stop or restart condition.
[0] NCKI	**NAK Interrupt** In MASTER Mode, this bit is set when a Not Acknowledge condition is received or sent, and neither the start nor the stop bit is active. In MASTER Mode, this bit can only be cleared by setting the start or stop bits. In SLAVE Mode, this bit is set when a Not Acknowledge condition is received (i.e., a master reading data from a slave), indicating that the master is finished reading. A stop or restart condition follows. In SLAVE Mode this bit clears when the I2CISTAT Register is read.

16.3.3. I2C Control Register

The I2C Control Register, shown in Table 156, enables and configures I2C operation.

Note: The R/W1 bit can be set (written to 1) when IEN=1, but cannot be cleared (written to 0).

Table 156. I2C Control Register (I2CCTL)

Bit	7	6	5	4	3	2	1	0
Field	IEN	START	STOP	BIRQS	TXI	NAK	FLUSH	FILTEN
Reset	0	0	0	0	0	0	0	0
R/W	R/W	R/W1	R/W1	R/W	R/W	R/W1	W	R/W
Address	F52h							

Bit	Description
[7] IEN	**I2C Enable** This bit enables the I2C controller.

17.3.7. USB OUT Endpoint 1–3 Start Address Subregisters

The USB OUT 1–3 Start Address subregisters, shown in Table 176, in conjunction with the USBISTADDR Register shown in Table 177, define the size of each OUT endpoint.

Table 176. USB OUT Endpoint 1–3 Start Address Subregisters (USBO*x*ADDR)

Bit	7	6	5	4	3	2	1	0
Field	OUTADDR							
Reset	see below description							
R/W	R0/W*	R0/W*	R0/W*	R0/W*	R0/W*	R0/W*	R0/W*	R0/W*
Address	If USBSA = 01h, 02h, 03h in the USB Subaddress Register, it is accessible through the USB Subdata Register							

Note: *R0/W = Write but reads back as 0.

Bit	Description
[7:0] OUTADDR	**OUT Endpoint Start Address** 00–FF: The start address of OUT endpoint memory buffers except OUT endpoint 0. The first starting address (OUT endpoint 0) is fixed at buffer memory address 000h. {0, OUTADDR[7:0], 0} maps to buffer memory address [9:0]; therefore the minimum increment of OUTADDR is 2 bytes of buffer memory. The size in bytes of an OUT endpoint is determined by subtracting consecutive starting address values then multiplying by 2. OUTADDR should be set to 00h for any OUT endpoint that doesn't exist (or is not used). See USB Endpoint Buffer Memory on page 341 for details. **Reset State:** USBO1ADDR: 20h USBO2ADDR: 40h USBO3ADDR: 60h

17.3.11. USB Interrupt Identification Subregister

The USB Interrupt Identification Subregister, shown in Table 180, contains the USB Module interrupt identifier. When the USB Module generates a USB interrupt request, the USBIID Subregister is updated to indicate the source of the interrupt. If more than one USB interrupt request is asserted, the contents of IID reflect the highest priority interrupt based on the order listed in the IID description. To learn more, see the Interrupts section on page 355.

Table 180. USB Interrupt Identification Subregister (USBIID)

Bit	7	6	5	4	3	2	1	0
Field	Reserved	IID					Reserved	
Reset	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R
Address	If USBSA = 28h in the USB Subaddress Register, accessible through the USB Subdata Register							

Bit	Description
[7]	**Reserved** This bit is reserved and must be programmed to 0.
[6:2] IID	**Interrupt Identification (Source)** 00000: SUDAVIRQ in the USBIRQ Register. Highest priority. 00001: SOFIRQ in the USBIRQ Register. 00010: SUTOKIRQ in the USBIRQ Register. 00011: SUSPIRQ in the USBIRQ Register. 00100: URESIRQ in the USBIRQ Register. 00101: Reserved. 00110: IN0IRQ in the USBINIRQ Register. 00111: OUT0IRQ in the USBOUTIRQ Register. 01000: IN1IRQ in the USBINIRQ Register. 01001: OUT1IRQ in the USBOUTIRQ Register. 01010: IN2IRQ in the USBINIRQ Register. 01011: OUT2IRQ in the USBOUTIRQ Register. 01100: IN3IRQ in the USBINIRQ Register. 01101: OUT3IRQ in the USBOUTIRQ Register. Lowest priority. Others: Reserved.
[1:0]	**Reserved** These bits are reserved and must be programmed to 00.

Bit	Description (Continued)
[1] CHAIN32	**Chain DMA3and DMA2** 0: DMA3 and DMA2 are independent of each other. 1: DMA3 and DMA2 are chained together, as described in the Chain Operation section on page 393.
[0] CHAIN10	**Chain DMA1 and DMA0** 0: DMA1 and DMA0 are independent of each other. 1: DMA1 and DMA0 are chained together, as described in the Chain Operation section on page 393.

18.3.4. DMA Source Address Subregisters

The DMAxSRCH and DMAxSRCL subregisters, shown in Tables 207 and 208, combine to form the 12-bit source address for the DMA transaction. Upon each byte transfer, the source address is updated based on the SRCCTL configuration in the DMAx Control 0 Subregister. In addition, DMAxSRCH contains transfer in list (TXLIST) control.

Table 207. DMA Source Address High Subregister (DMAxSRCH)

Bit	7	6	5	4	3	2	1	0
Field	TXLIST	Reserved			SRCH			
Reset	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Address	If DMASA = 0h in the DMAxSA Register, accessible through the DMA 0–3 Subregister							

Bit	Description
[7] TXLIST	**Transfer In List** TXLIST has an effect only during linked list operation, see the Linked List Control Options section on page 395 for details.
[6:4]	**Reserved** These bits are reserved and must be programmed to 000.
[3:0] SRCH	**Source Address High** 0–F: Upper 4 bits of the DMA source address.

28.3.1.2. Trim Bit Addresses 0001h and 0002h

The Trim Option Bits registers at addresses 0001h and 00002h, shown in Tables 290 and 291, govern control of the temperature sensor trim bits.

Table 290. Trim Option Bits at Address 0001h (TTEMP0)

Bit	7	6	5	4	3	2	1	0
Field	Reserved		TS_GAIN					
Reset	X	X	X	X	X	X	X	X
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	Information Page Memory 0021h							

Note: X = undefined; R/W = read/write; R = read-only.

Bit	Description
[7:6]	**Reserved** These bits are reserved.
[5:0] TS_GAIN	**Temperature Gain Trim Bits** Contains gain trimming bits for the Temperature Sensor.

Table 291. Trim Option Bits at Address 0002h (TTEMP1)

Bit	7	6	5	4	3	2	1	0
Field	TS_OFFSET							
Reset	X	X	X	X	X	X	X	X
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	Information Page Memory 0022h							

Note: X = undefined; R/W = read/write; R = read-only.

Bit	Description
[7:0] TS_OFFSET	**Temperature Sensor Offset Trim Bits** Contains offset trimming bits for the Temperature Sensor.

Table 294. LVD_Trim Values

	LVD Threshold (V)			
LVD_TRIM	**Minimum**	**Typical**	**Maximum**	**Description**
00000		3.20		Maximum LVD threshold
00001		3.15		
00010		3.10		
00011		3.05		
00100		3.00		
00101		2.95		
00110		2.90		
00111		2.85		
01000		2.80		
01001		2.75		
01010		2.70		
01011		2.65		
01100		2.60		
01101		2.55		
01110		2.50		
01111		2.45		
10000		2.40		
10001		2.35		
10010		2.30		
10011		2.25		
10100		2.20		
10101		2.15		
10110		2.10		
10111		2.05		
11000		2.00		
11001		1.95		
11010		1.90		
11011		1.85		
11100		1.80		
11101		1.75		
11110		1.70		
11111		1.65		Minimum LVD threshold; default on Reset.

Table 338. Digital-to-Analog Converter Electrical Characteristics and Timing (Continued)

		V_{DD}=1.8V to 3.6V T_A=–40°C to +85°C				
Symbol	**Parameter**	**Min**	**Typ***	**Max**	**Units**	**Conditions**
R_{OUT}	Output Resistance		25	75	Ω	$V_{SS} \le V_{DACOUT} \le V_{DD}$
				3	Ω	V_{SS}+0.3V ≤ V_{DACOUT} ≤ V_{DD}–0.3V
V_{DAC}	DAC Output Voltage Range	AV_{SS}+0.1V		AV_{DD}–0.1V	V	
T_{SET_FS}	Settling Time, full scale		15		µs	POWER=00
			40		µs	POWER=01
			100		µs	POWER=10
T_{SET_CC}	Settling Time, code to code (adjacent codes)		1		µs	POWER=00
			2		µs	POWER=01
			5		µs	POWER=10
SR	Slew Rate		5		V/µs	POWER=00
			1.4		V/µs	POWER=01
			0.35		V/µs	POWER=10
T_{UP}	Update rate			1	µs	
T_{WAKE_DR}	Time for Wake up, Internal DAC Reference		0.5	1.1	ms	C_{VREFP}=1µF
T_{WAKE_DAC}	Time for Wake up, DAC		18		µs	POWER=00
			25		µs	POWER=01
			35		µs	POWER=10

Note: *Data in the Typical column is from characterization at 3.0V and 25°C. These values are provided for design guidance only and are not tested in production.

Table 344. LCD Electrical Characteristics (Continued)

		T_A = –40°C to +85°C V_{DD} = 1.8V to 3.6V				
Symbol	**Parameter**	**Min**	**Typ***	**Max**	**Units**	**Conditions**
V_{CPT}	LCD Charge Pump Output Voltage when tripler is selected (CPEN=1, CPTSEL=0)		2.5		V	V_{DD} ≥ 1.8V, CONTRAST=000
			2.64		V	V_{DD} ≥ 1.8V, CONTRAST=001
			2.78		V	V_{DD} ≥ 1.8V, CONTRAST=010
			2.92		V	V_{DD} ≥ 1.8V, CONTRAST=011
			3.06		V	V_{DD} ≥ 1.8V, CONTRAST=100
			3.20		V	V_{DD} ≥ 1.8V, CONTRAST=101
			3.35		V	V_{DD} ≥ 1.8V, CONTRAST=110
			3.5		V	V_{DD} ≥ 2.0V, CONTRAST=111
R_{BIAS}	Resistance of Bias Network (1/3 LCD waveform biasing, 1/2 LCD waveform biasing)		4.5, 4.5		MΩ	BIASGSEL=X, not during transition drive
			340, 240		kΩ	BIASGSEL=0, during medium transition drive
			100, 60		kΩ	BIASGSEL=1, during high transition drive
C_{VLCD}	Capacitance on VLCD pin		1		µF	
C_{PANEL}	VLCD Panel Capacitance			8000	pF	40 Hz frame frequency
TC_{VLCD}	Time to Charge VLCD with Internal Charge Pump	0.1		3	µF* s	BIASGSEL = 0

Notes:
1. Data in the Typical column is from characterization at 3.0V and 25°C. These values are provided for design guidance only and are not tested in production.
2. Based on PCLK= 32.768kHz (CKSEL=0), 32 Hz frame rate (PRESCALE=011, FDIV=0111), and LCD mode of 1/4 duty, 1/3 bias, type A waveform (LCDMODE=1011). Either VLCD=3V (VLCDDIR=0) or V_{DD}=3V (VLCDDIR=0, CPEN=0). No LCD panel load.
3. VLCD=3.06V (CONTRAST=100), V_{DD}=3.0V.

Table 346. IPO Electrical Characteristics (Continued)

		V_{DD}=1.8V to 3.6V T_A=–40°C to +85°C				
Symbol	**Parameter**	**Min**	**Typ***	**Max**	**Units**	**Conditions**
F_{IPO}	Output Frequency	–2%	32.768	+2%	kHz	
	Duty Cycle of Output	45		55	%	
T_{WAKE}	Time for Wake up		25		µs	

Note: *Data in the Typical column is from characterization at 3.0V and 25°C. These values are provided for design guidance only and are not tested in production.

33.4.17. High Frequency Crystal Oscillator

Table 347 presents electrical and timing data for the F6482 Series' High Frequency Crystal Oscillator function.

Table 347. High Frequency Crystal Oscillator (HFXO) Characteristics

		T_A=–40°C to +85°C V_{DD}=1.8V to 3.6V				
Symbol	**Parameter**	**Min**	**Typ***	**Max**	**Units**	**Conditions**
I_{DD}HFXO	HFXO Active Supply Current		100		µA	HFXOBAND=00[2]
			150		µA	HFXOBAND=01[2]
			200		µA	HFXOBAND=10[2]
F_{XTAL}	HFXO Frequency	1		8	MHz	HFXOBAND=00
		> 8		16	MHz	HFXOBAND=01
		>16		24	MHz	HFXOBAND=10
gm	Oscillator Transconductance	0.4			mA/V	HFXOBAND=00[2]
		1.0			mA/V	HFXOBAND=01[2]
		2.5			mA/V	HFXOBAND=10[2]
T_{WAKE}	Time for Wake up		2	4	ms	HFXOBAND=00[2]
			1.2	2.4	ms	HFXOBAND=01[2]
			1	2	ms	HFXOBAND=10[2]
	SCKOUT Duty Cycle	40	50	60	%	

Notes:
1. Data in the Typical column is from characterization at 3.0V and 25°C. These values are provided for design guidance only and are not tested in production.
2. C_{LOAD}=12.5 pF.

33.4.20. Digitally Controlled Oscillator and Frequency-Locked Loop

Table 350 presents electrical and timing data for the F6482 Series' Digitally Controlled Oscillator (DCO) and Frequency-Locked Loop functions.

Table 350. DCO and FLL Electrical Characteristics

		V_{DD}=1.8V to 3.6V T_A=–40°C to +85°C				
Symbol	**Parameter**	**Min**	**Typ***	**Max**	**Units**	**Conditions**
I_{DD}DCO	DCO Active Supply Current		25		µA	F_{DCO}=1MHz
			90		µA	F_{DCO}=10MHz
			125		µA	F_{DCO}=20MHz
			150		µA	F_{DCO}=24MHz
I_{DD}FLL	FLL Active Supply Current		20		µA	
F_{DCO}	DCO Frequency	1		24	MHz	
$F_{FLLCLKIN}$	FLL Input Clock Frequency		32.768		kHz	
	Duty Cycle of DCO Output	45		55	%	
	DCO Resolution		150		ps	
	DCO control word resolution, {DCOCTLCH, DCODTLCL}		600		ps	
	DCO Temperature Coefficient (FLL off)		+0.2		%/C	
	DCO Voltage Coefficient (FLL off)		+0.01		%/V	For changes in V_{DD}
T_{LOCK}	FLL Lock Time (FLLLOCK=1)		200		µs	PCLK=32.768kHz; fast locking selected
$T_{FLADONE}$	FLL Fast Lock Algorithm Time (FLADONE=1)		2.5		ms	PCLK=32.768kHz; fast locking selected

Note: *Data in the Typical column is from characterization at 3.0V and 25°C. These values are provided for design guidance only and are not tested in production.