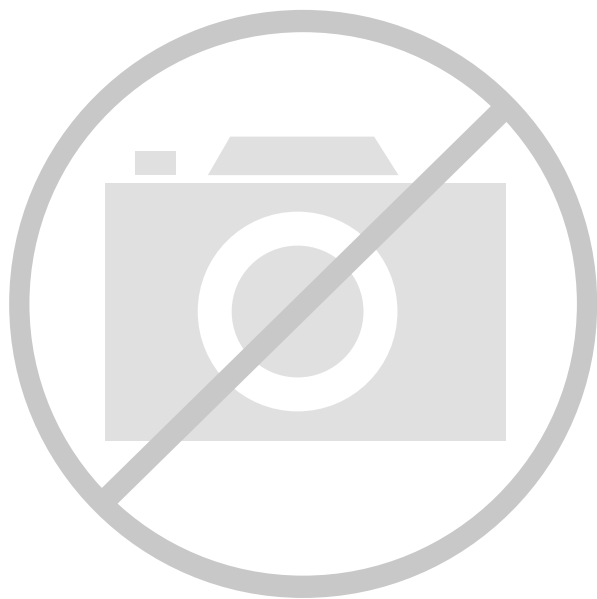




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Details

Product Status	Active
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	31
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 10x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	36-WFQFN Exposed Pad
Supplier Device Package	36-HWQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f213j4cnp-u0

1.2 Product List

Table 1.3 lists Product List for R8C/3JC Group, and Figure 1.1 shows a Part Number, Memory Size, and Package of R8C/3JC Group.

Table 1.3 Product List for R8C/3JC Group

Current of May 2010

Part No.	ROM Capacity		RAM Capacity	Package Type	Remarks
	Program ROM	Data flash			
R5F213J2CNP	8 Kbytes	1 Kbyte × 4	1 Kbyte	PWQN0036KA-B	N version
R5F213J4CNP	16 Kbytes	1 Kbyte × 4	1.5 Kbytes	PWQN0036KA-B	
R5F213J5CNP	24 Kbytes	1 Kbyte × 4	2 Kbytes	PWQN0036KA-B	
R5F213J6CNP	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PWQN0036KA-B	

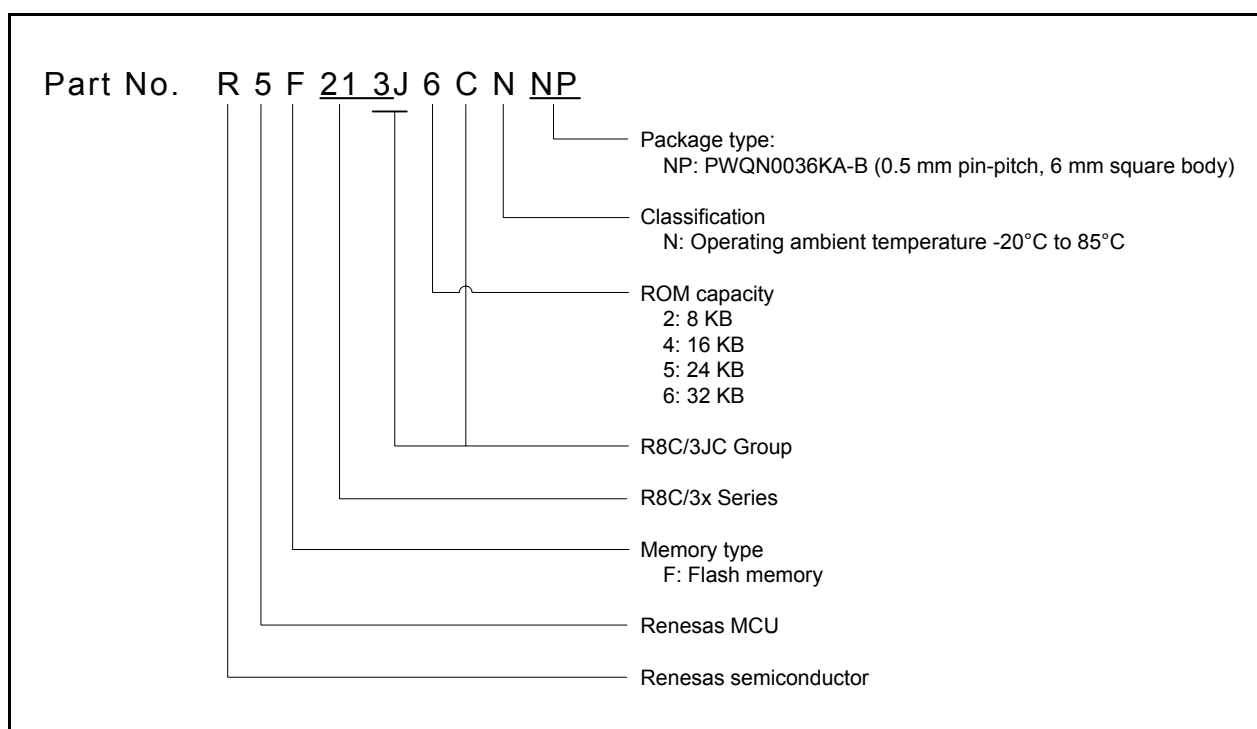


Figure 1.1 Part Number, Memory Size, and Package of R8C/3JC Group

Table 1.5 Pin Name Information by Pin Number (2)

Pin Number	Control Pin	Port	I/O Pin Functions for Peripheral Modules					
			Interrupt	Timer	Serial Interface	SSU	I ² C bus	A/D Converter, D/A Converter, Comparator B
31		P0_4		TREO/ (TRCIOB)				AN3
32		P0_3		(TRCIOB)	(CLK1)			AN4
33		P0_2		(TRCIOA/ TRCTRG)	(RXD1)			AN5
34		P0_1		(TRCIOA/ TRCTRG)	(TXD1)			AN6
35		P4_2						VREF
36	MODE							

Note:

1. Can be assigned to the pin in parentheses by a program.

1.5 Pin Functions

Tables 1.6 and 1.7 list Pin Functions.

Table 1.6 Pin Functions (1)

Item	Pin Name	I/O Type	Description
Power supply input	VCC, VSS	–	Apply 1.8 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS	–	Power supply for the A/D converter. Connect a capacitor between AVCC and AVSS.
Reset input	$\overline{\text{RESET}}$	I	Input “L” on this pin resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
XIN clock input	XIN	I	These pins are provided for XIN clock generation circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins ⁽¹⁾ . To use an external clock, input it to the XOUT pin and leave the XIN pin open.
XIN clock output	XOUT	I/O	
XCIN clock input	XCIN	I	These pins are provided for XCIN clock generation circuit I/O. Connect a crystal oscillator between the XCIN and XCOU pins ⁽¹⁾ . To use an external clock, input it to the XCIN pin and leave the XCOU pin open.
XCIN clock output	XCOU	O	
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT3}}$	I	$\overline{\text{INT}}$ interrupt input pins. $\overline{\text{INT0}}$ is timer RB, RC and RD input pin.
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Key input interrupt input pins
Timer RA	TRAIO	I/O	Timer RA I/O pin
	TRA0	O	Timer RA output pin
Timer RB	TRBO	O	Timer RB output pin
Timer RC	TRCLK	I	External clock input pin
	TRCTR	I	External trigger input pin
	TRCIOA, TRCIOB, TRCIO, TRCIOD	I/O	Timer RC I/O pins
Timer RD	TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1	I/O	Timer RD I/O pins
	TRDCLK	I	External clock input pin
Timer RE	TREO	O	Divided clock output pin
Serial interface	CLK0, CLK1, CLK2	I/O	Transfer clock I/O pins
	RXD0, RXD1, RXD2	I	Serial data input pins
	TXD0, TXD1, TXD2	O	Serial data output pins
	$\overline{\text{CTS2}}$	I	Transmission control input pin
	$\overline{\text{RTS2}}$	O	Reception control output pin
	SCL2	I/O	I ² C mode clock I/O pin
	SDA2	I/O	I ² C mode data I/O pin
I ² C bus	SCL	I/O	Clock I/O pin
	SDA	I/O	Data I/O pin
SSU	SSI	I/O	Data I/O pin
	$\overline{\text{SCS}}$	I/O	Chip-select signal I/O pin
	SSCK	I/O	Clock I/O pin
	SSO	I/O	Data I/O pin

I: Input O: Output I/O: Input and output

Note:

1. Refer to the oscillator manufacturer for oscillation characteristics.

Table 1.7 Pin Functions (2)

Item	Pin Name	I/O Type	Description
Reference voltage input	VREF	I	Reference voltage input pin to A/D converter and D/A converter
A/D converter	AN0 to AN1, AN3 to AN6, AN8 to AN11	I	Analog input pins to A/D converter
	ADTRG	I	A/D external trigger input pin
D/A converter	DA0, DA1	O	D/A converter output pins
Comparator B	IVCMP1, IVCMP3	I	Comparator B analog voltage input pins
	IVREF1, IVREF3	I	Comparator B reference voltage input pins
I/O port	P0_1 to P0_4, P0_6, P0_7, P1_0 to P1_7, P2_0 to P2_5, P3_1, P3_3 to P3_5, P3_7, P4_3 to P4_7, P6_6	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program. All ports can be used as LED drive ports.
Input port	P4_2	I	Input-only port

I: Input O: Output I/O: Input and output

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.

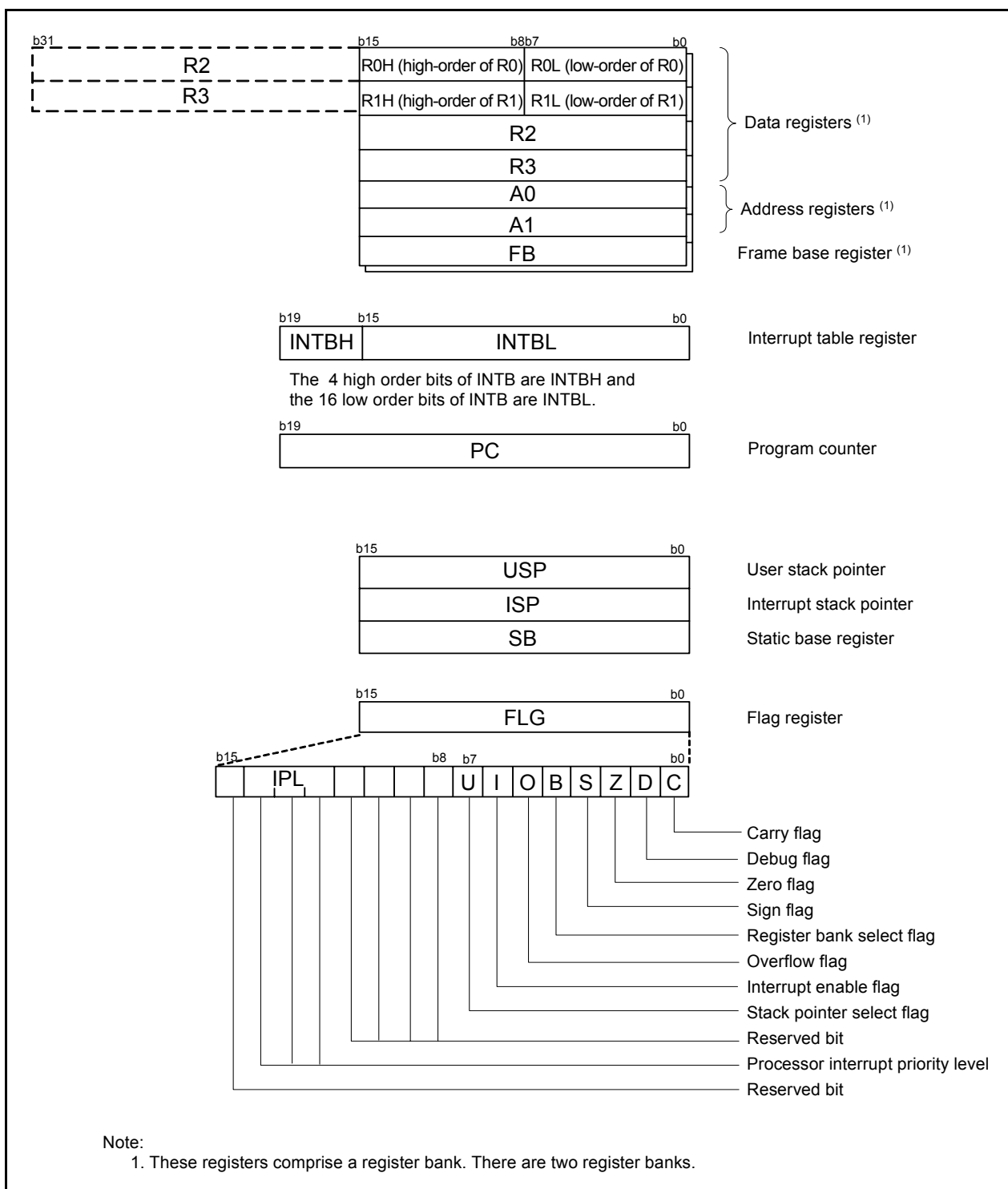


Figure 2.1 CPU Registers

4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.12 list the special function registers. Table 4.13 lists the ID Code Areas and Option Function Select Area.

Table 4.1 SFR Information (1) (1)

Address	Register	Symbol	After Reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	00101000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h	Module Standby Control Register	MSTCR	00h
0009h	System Clock Control Register 3	CM3	00h
000Ah	Protect Register	PRCR	00h
000Bh	Reset Source Determination Register	RSTFR	0XXXXXXb (2)
000Ch	Oscillation Stop Detection Register	OCD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDTC	00111111b
0010h			
0011h			
0012h			
0013h			
0014h			
0015h	High-Speed On-Chip Oscillator Control Register 7	FRA7	When shipping
0016h			
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h 10000000b (3)
001Dh			
001Eh			
001Fh			
0020h			
0021h			
0022h			
0023h	High-Speed On-Chip Oscillator Control Register 0	FRA0	00h
0024h	High-Speed On-Chip Oscillator Control Register 1	FRA1	When shipping
0025h	High-Speed On-Chip Oscillator Control Register 2	FRA2	00h
0026h	On-Chip Reference Voltage Control Register	OCVREFCR	00h
0027h			
0028h	Clock Prescaler Reset Flag	CPSRF	00h
0029h	High-Speed On-Chip Oscillator Control Register 4	FRA4	When Shipping
002Ah	High-Speed On-Chip Oscillator Control Register 5	FRA5	When Shipping
002Bh	High-Speed On-Chip Oscillator Control Register 6	FRA6	When Shipping
002Ch			
002Dh			
002Eh			
002Fh	High-Speed On-Chip Oscillator Control Register 3	FRA3	When shipping
0030h	Voltage Monitor Circuit Control Register	CMPA	00h
0031h	Voltage Monitor Circuit Edge Select Register	VCAC	00h
0032h			
0033h	Voltage Detect Register 1	VCA1	00001000b
0034h	Voltage Detect Register 2	VCA2	00h (4) 00100000b (5)
0035h			
0036h	Voltage Detection 1 Level Select Register	VD1LS	00000111b
0037h			
0038h	Voltage Monitor 0 Circuit Control Register	VW0C	1100X010b (4) 1100X011b (5)
0039h	Voltage Monitor 1 Circuit Control Register	VW1C	10001010b

X: Undefined

Notes:

1. The blank areas are reserved and cannot be accessed by users.
2. The CWR bit in the RSTFR register is set to 0 after power-on and voltage monitor 0 reset. Hardware reset, software reset, or watchdog timer reset does not affect this bit.
3. The CSPROINI bit in the OFS register is set to 0.
4. The LVDAS bit in the OFS register is set to 1.
5. The LVDAS bit in the OFS register is set to 0.

Table 4.3 SFR Information (3) (1)

Address	Register	Symbol	After Reset
0080h	DTC Activation Control Register	DTCTL	00h
0081h			
0082h			
0083h			
0084h			
0085h			
0086h			
0087h			
0088h	DTC Activation Enable Register 0	DTCEN0	00h
0089h	DTC Activation Enable Register 1	DTCEN1	00h
008Ah	DTC Activation Enable Register 2	DTCEN2	00h
008Bh	DTC Activation Enable Register 3	DTCEN3	00h
008Ch	DTC Activation Enable Register 4	DTCEN4	00h
008Dh	DTC Activation Enable Register 5	DTCEN5	00h
008Eh	DTC Activation Enable Register 6	DTCEN6	00h
008Fh			
0090h			
0091h			
0092h			
0093h			
0094h			
0095h			
0096h			
0097h			
0098h			
0099h			
009Ah			
009Bh			
009Ch			
009Dh			
009Eh			
009Fh			
00A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h			XXh
00A8h	UART2 Transmit/Receive Mode Register	U2MR	00h
00A9h	UART2 Bit Rate Register	U2BRG	XXh
00AAh	UART2 Transmit Buffer Register	U2TB	XXh
00ABh			XXh
00ACh	UART2 Transmit/Receive Control Register 0	U2C0	00001000b
00ADh	UART2 Transmit/Receive Control Register 1	U2C1	00000010b
00AEh	UART2 Receive Buffer Register	U2RB	XXh
00AFh			XXh
00B0h	UART2 Digital Filter Function Select Register	URXDF	00h
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h			
00B9h			
00BAh			
00BBh	UART2 Special Mode Register 5	U2SMR5	00h
00BCh	UART2 Special Mode Register 4	U2SMR4	00h
00BDh	UART2 Special Mode Register 3	U2SMR3	000X0X0Xb
00BEh	UART2 Special Mode Register 2	U2SMR2	X0000000b
00BFh	UART2 Special Mode Register	U2SMR	X0000000b

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.4 SFR Information (4) (1)

Address	Register	Symbol	After Reset
00C0h	A/D Register 0	AD0	XXh
00C1h			000000XXb
00C2h	A/D Register 1	AD1	XXh
00C3h			000000XXb
00C4h	A/D Register 2	AD2	XXh
00C5h			000000XXb
00C6h	A/D Register 3	AD3	XXh
00C7h			000000XXb
00C8h	A/D Register 4	AD4	XXh
00C9h			000000XXb
00CAh	A/D Register 5	AD5	XXh
00CBh			000000XXb
00CCh	A/D Register 6	AD6	XXh
00CDh			000000XXb
00CEh	A/D Register 7	AD7	XXh
00CFh			000000XXb
00D0h			
00D1h			
00D2h			
00D3h			
00D4h	A/D Mode Register	ADMOD	00h
00D5h	A/D Input Select Register	ADINSEL	11000000b
00D6h	A/D Control Register 0	ADCON0	00h
00D7h	A/D Control Register 1	ADCON1	00h
00D8h	D/A0 Register	DA0	00h
00D9h	D/A1 Register	DA1	00h
00DAh			
00DBh			
00DCh	D/A Control Register	DACON	00h
00DDh			
00DEh			
00DFh			
00E0h	Port P0 Register	P0	XXh
00E1h	Port P1 Register	P1	XXh
00E2h	Port P0 Direction Register	PD0	00h
00E3h	Port P1 Direction Register	PD1	00h
00E4h	Port P2 Register	P2	XXh
00E5h	Port P3 Register	P3	XXh
00E6h	Port P2 Direction Register	PD2	00h
00E7h	Port P3 Direction Register	PD3	00h
00E8h	Port P4 Register	P4	XXh
00E9h			
00EAh	Port P4 Direction Register	PD4	00h
00EBh			
00ECh	Port P6 Register	P6	XXh
00EDh			
00EEh	Port P6 Direction Register	PD6	00h
00EFh			
00F0h			
00F1h			
00F2h			
00F3h			
00F4h			
00F5h			
00F6h			
00F7h			
00F8h			
00F9h			
00FAh			
00FBh			
00FCh			
00FDh			
00FEh			
00FFh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.8 SFR Information (8) (1)

Address	Register	Symbol	After Reset
01C0h	Address Match Interrupt Register 0	RMAD0	XXh
01C1h			XXh
01C2h			0000XXXXb
01C3h	Address Match Interrupt Enable Register 0	AIER0	00h
01C4h	Address Match Interrupt Register 1	RMAD1	XXh
01C5h			XXh
01C6h			0000XXXXb
01C7h	Address Match Interrupt Enable Register 1	AIER1	00h
01C8h			
01C9h			
01CAh			
01CBh			
01CCh			
01CDh			
01CEh			
01CFh			
01D0h			
01D1h			
01D2h			
01D3h			
01D4h			
01D5h			
01D6h			
01D7h			
01D8h			
01D9h			
01DAh			
01DBh			
01DCh			
01DDh			
01DEh			
01DFh			
01E0h	Pull-Up Control Register 0	PUR0	00h
01E1h	Pull-Up Control Register 1	PUR1	00h
01E2h			
01E3h			
01E4h			
01E5h			
01E6h			
01E7h			
01E8h			
01E9h			
01EAh			
01EBh			
01ECh			
01EDh			
01EEh			
01EFh			
01F0h	Port P1 Drive Capacity Control Register	P1DRR	00h
01F1h	Port P2 Drive Capacity Control Register	P2DRR	00h
01F2h	Drive Capacity Control Register 0	DRR0	00h
01F3h	Drive Capacity Control Register 1	DRR1	00h
01F4h			
01F5h	Input Threshold Control Register 0	VLT0	00h
01F6h	Input Threshold Control Register 1	VLT1	00h
01F7h			
01F8h	Comparator B Control Register 0	INTCMP	00h
01F9h			
01FAh	External Input Enable Register 0	INTEN	00h
01FBh			
01FCh	INT Input Filter Select Register 0	INTF	00h
01FDh			
01FEh	Key Input Enable Register 0	KIEN	00h
01FFh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.11 SFR Information (11) (1)

Address	Register	Symbol	After Reset
2CB0h	DTC Control Data 14	DTCD14	XXh
2CB1h			XXh
2CB2h			XXh
2CB3h			XXh
2CB4h			XXh
2CB5h			XXh
2CB6h			XXh
2CB7h			XXh
2CB8h	DTC Control Data 15	DTCD15	XXh
2CB9h			XXh
2CBAh			XXh
2CBBh			XXh
2CBCh			XXh
2CBDh			XXh
2CBEh			XXh
2CBFh			XXh
2CC0h	DTC Control Data 16	DTCD16	XXh
2CC1h			XXh
2CC2h			XXh
2CC3h			XXh
2CC4h			XXh
2CC5h			XXh
2CC6h			XXh
2CC7h			XXh
2CC8h	DTC Control Data 17	DTCD17	XXh
2CC9h			XXh
2CCAh			XXh
2CCBh			XXh
2CCCh			XXh
2CCDh			XXh
2CCEh			XXh
2CCFh			XXh
2CD0h	DTC Control Data 18	DTCD18	XXh
2CD1h			XXh
2CD2h			XXh
2CD3h			XXh
2CD4h			XXh
2CD5h			XXh
2CD6h			XXh
2CD7h			XXh
2CD8h	DTC Control Data 19	DTCD19	XXh
2CD9h			XXh
2CDAh			XXh
2CDBh			XXh
2CDCh			XXh
2CDDh			XXh
2CDEh			XXh
2CDFh			XXh
2CE0h	DTC Control Data 20	DTCD20	XXh
2CE1h			XXh
2CE2h			XXh
2CE3h			XXh
2CE4h			XXh
2CE5h			XXh
2CE6h			XXh
2CE7h			XXh
2CE8h	DTC Control Data 21	DTCD21	XXh
2CE9h			XXh
2CEAh			XXh
2CEBh			XXh
2CECh			XXh
2CEDh			XXh
2CEEh			XXh
2CEFh			XXh

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 5.15 Recommended Operating Conditions

Symbol	Parameter			Conditions	Standard			Unit	
					Min.	Typ.	Max.		
V _{CC} /AV _{CC}	Supply voltage				1.8	—	5.5	V	
V _{SS} /AV _{SS}	Supply voltage				—	0	—	V	
V _{IH}	Input “H” voltage	Other than CMOS input				0.8 V _{CC}	—	V _{CC}	V
		CMOS input	Input level switching function (I/O port)	Input level selection: 0.35 V _{CC}	4.0 V ≤ V _{CC} ≤ 5.5 V	0.5 V _{CC}	—	V _{CC}	V
					2.7 V ≤ V _{CC} < 4.0 V	0.55 V _{CC}	—	V _{CC}	V
					1.8 V ≤ V _{CC} < 2.7 V	0.65 V _{CC}	—	V _{CC}	V
			Input level selection: 0.5 V _{CC}	4.0 V ≤ V _{CC} ≤ 5.5 V	0.65 V _{CC}	—	V _{CC}	V	
				2.7 V ≤ V _{CC} < 4.0 V	0.7 V _{CC}	—	V _{CC}	V	
				1.8 V ≤ V _{CC} < 2.7 V	0.8 V _{CC}	—	V _{CC}	V	
			Input level selection: 0.7 V _{CC}	4.0 V ≤ V _{CC} ≤ 5.5 V	0.85 V _{CC}	—	V _{CC}	V	
				2.7 V ≤ V _{CC} < 4.0 V	0.85 V _{CC}	—	V _{CC}	V	
				1.8 V ≤ V _{CC} < 2.7 V	0.85 V _{CC}	—	V _{CC}	V	
	External clock input (XOUT)				1.2	—	V _{CC}	V	
V _{IL}	Input “L” voltage	Other than CMOS input				0	—	0.2 V _{CC}	V
		CMOS input	Input level switching function (I/O port)	Input level selection: 0.35 V _{CC}	4.0 V ≤ V _{CC} ≤ 5.5 V	0	—	0.2 V _{CC}	V
					2.7 V ≤ V _{CC} < 4.0 V	0	—	0.2 V _{CC}	V
					1.8 V ≤ V _{CC} < 2.7 V	0	—	0.2 V _{CC}	V
			Input level selection: 0.5 V _{CC}	4.0 V ≤ V _{CC} ≤ 5.5 V	0	—	0.4 V _{CC}	V	
				2.7 V ≤ V _{CC} < 4.0 V	0	—	0.3 V _{CC}	V	
				1.8 V ≤ V _{CC} < 2.7 V	0	—	0.2 V _{CC}	V	
			Input level selection: 0.7 V _{CC}	4.0 V ≤ V _{CC} ≤ 5.5 V	0	—	0.55 V _{CC}	V	
				2.7 V ≤ V _{CC} < 4.0 V	0	—	0.45 V _{CC}	V	
				1.8 V ≤ V _{CC} < 2.7 V	0	—	0.35 V _{CC}	V	
	External clock input (XOUT)				0	—	0.4	V	
I _{OH} (sum)	Peak sum output “H” current	Sum of all pins I _{OH} (peak)			—	—	–160	mA	
I _{OH} (sum)	Average sum output “H” current	Sum of all pins I _{OH} (avg)			—	—	–80	mA	
I _{OH} (peak)	Peak output “H” current	Drive capacity Low			—	—	–10	mA	
		Drive capacity High			—	—	–40	mA	
I _{OH} (avg)	Average output “H” current	Drive capacity Low			—	—	–5	mA	
		Drive capacity High			—	—	–20	mA	
I _{OL} (sum)	Peak sum output “L” current	Sum of all pins I _{OL} (peak)			—	—	160	mA	
I _{OL} (sum)	Average sum output “L” current	Sum of all pins I _{OL} (avg)			—	—	80	mA	
I _{OL} (peak)	Peak output “L” current	Drive capacity Low			—	—	10	mA	
		Drive capacity High			—	—	40	mA	
I _{OL} (avg)	Average output “L” current	Drive capacity Low			—	—	5	mA	
		Drive capacity High			—	—	20	mA	
f _(XIN)	XIN clock input oscillation frequency			2.7 V ≤ V _{CC} ≤ 5.5 V	—	—	20	MHz	
				1.8 V ≤ V _{CC} < 2.7 V	—	—	5	MHz	
f _(XCIN)	XCIN clock input oscillation frequency			1.8 V ≤ V _{CC} ≤ 5.5 V	—	32.768	50	kHz	
f _{OCO40M}	When used as the count source for timer RC or timer RD ⁽³⁾			2.7 V ≤ V _{CC} ≤ 5.5 V	32	—	40	MHz	
f _{OCO-F}	f _{OCO-F} frequency			2.7 V ≤ V _{CC} ≤ 5.5 V	—	—	20	MHz	
				1.8 V ≤ V _{CC} < 2.7 V	—	—	5	MHz	
—	System clock frequency			2.7 V ≤ V _{CC} ≤ 5.5 V	—	—	20	MHz	
				1.8 V ≤ V _{CC} < 2.7 V	—	—	5	MHz	
f _(BCLK)	CPU clock frequency			2.7 V ≤ V _{CC} ≤ 5.5 V	—	—	20	MHz	
				1.8 V ≤ V _{CC} < 2.7 V	—	—	5	MHz	

Notes:

1. V_{CC} = 1.8 to 5.5 V and T_{opr} = –20 to 85°C (N version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.
3. f_{OCO40M} can be used as the count source for timer RC or timer RD in the range of V_{CC} = 2.7 V to 5.5V.

Table 5.16 A/D Converter Characteristics

Symbol	Parameter		Conditions		Standard			Unit
					Min.	Typ.	Max.	
–	Resolution		V _{ref} = AV _{CC}		–	–	10	Bit
–	Absolute accuracy	10-bit mode	V _{ref} = AV _{CC} = 5.0 V	AN0 to AN1 input, AN3 to AN6 input, AN8 to AN11 input	–	–	±3	LSB
			V _{ref} = AV _{CC} = 3.3 V	AN0 to AN1 input, AN3 to AN6 input, AN8 to AN11 input	–	–	±5	LSB
			V _{ref} = AV _{CC} = 3.0 V	AN0 to AN1 input, AN3 to AN6 input, AN8 to AN11 input	–	–	±5	LSB
			V _{ref} = AV _{CC} = 2.2 V	AN0 to AN1 input, AN3 to AN6 input, AN8 to AN11 input	–	–	±5	LSB
		8-bit mode	V _{ref} = AV _{CC} = 5.0 V	AN0 to AN1 input, AN3 to AN6 input, AN8 to AN11 input	–	–	±2	LSB
			V _{ref} = AV _{CC} = 3.3 V	AN0 to AN1 input, AN3 to AN6 input, AN8 to AN11 input	–	–	±2	LSB
			V _{ref} = AV _{CC} = 3.0 V	AN0 to AN1 input, AN3 to AN6 input, AN8 to AN11 input	–	–	±2	LSB
			V _{ref} = AV _{CC} = 2.2 V	AN0 to AN1 input, AN3 to AN6 input, AN8 to AN11 input	–	–	±2	LSB
φAD	A/D conversion clock		4.0 V ≤ V _{ref} = AV _{CC} ≤ 5.5 V ⁽²⁾		2	–	20	MHz
			3.2 V ≤ V _{ref} = AV _{CC} ≤ 5.5 V ⁽²⁾		2	–	16	MHz
			2.7 V ≤ V _{ref} = AV _{CC} ≤ 5.5 V ⁽²⁾		2	–	10	MHz
			2.2 V ≤ V _{ref} = AV _{CC} ≤ 5.5 V ⁽²⁾		2	–	5	MHz
–	Tolerance level impedance				–	3	–	kΩ
t _{CONV}	Conversion time	10-bit mode	V _{ref} = AV _{CC} = 5.0 V, φAD = 20 MHz		2.15	–	–	μs
		8-bit mode	V _{ref} = AV _{CC} = 5.0 V, φAD = 20 MHz		2.15	–	–	μs
t _{SAMP}	Sampling time		φAD = 20 MHz		0.75	–	–	μs
I _{Vref}	V _{ref} current		V _{CC} = 5 V, XIN = f1 = φAD = 20 MHz		–	45	–	μA
V _{ref}	Reference voltage				2.2	–	AV _{CC}	V
V _{IA}	Analog input voltage ⁽³⁾				0	–	V _{ref}	V
OCVREF	On-chip reference voltage		2 MHz ≤ φAD ≤ 4 MHz		1.19	1.34	1.49	V

Notes:

1. $V_{CC}/AV_{CC} = V_{ref} = 2.2$ to 5.5 V , $V_{SS} = 0\text{ V}$ and $T_{opr} = -20$ to 85°C (N version), unless otherwise specified.
2. The A/D conversion result will be undefined in wait mode, stop mode, when the flash memory stops, and in low-current-consumption mode. Do not perform A/D conversion in these states or transition to these states during A/D conversion.
3. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

Table 5.19 Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase endurance ⁽²⁾		1,000 ⁽³⁾	—	—	times
—	Byte program time		—	80	500	μs
—	Block erase time		—	0.3	—	s
t _d (SR-SUS)	Time delay from suspend request until suspend		—	—	5+CPU clock × 3 cycles	ms
—	Interval from erase start/restart until following suspend request		0	—	—	μs
—	Time from suspend until erase restart		—	—	30+CPU clock × 1 cycle	μs
t _d (CMDRST-READY)	Time from when command is forcibly terminated until reading is enabled		—	—	30+CPU clock × 1 cycle	μs
—	Program, erase voltage		2.7	—	5.5	V
—	Read voltage		1.8	—	5.5	V
—	Program, erase temperature		0	—	60	°C
—	Data hold time ⁽⁷⁾	Ambient temperature = 55°C	20	—	—	year

Notes:

1. V_{CC} = 2.7 to 5.5 V and T_{opr} = 0 to 60°C, unless otherwise specified.

2. Definition of programming/erasure endurance

The programming and erasure endurance is defined on a per-block basis.

If the programming and erasure endurance is n (n = 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.

However, the same address must not be programmed more than once per erase operation (overwriting prohibited).

3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).

4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.

5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.

6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.

7. The data hold time includes time that the power supply is off or the clock is not supplied.

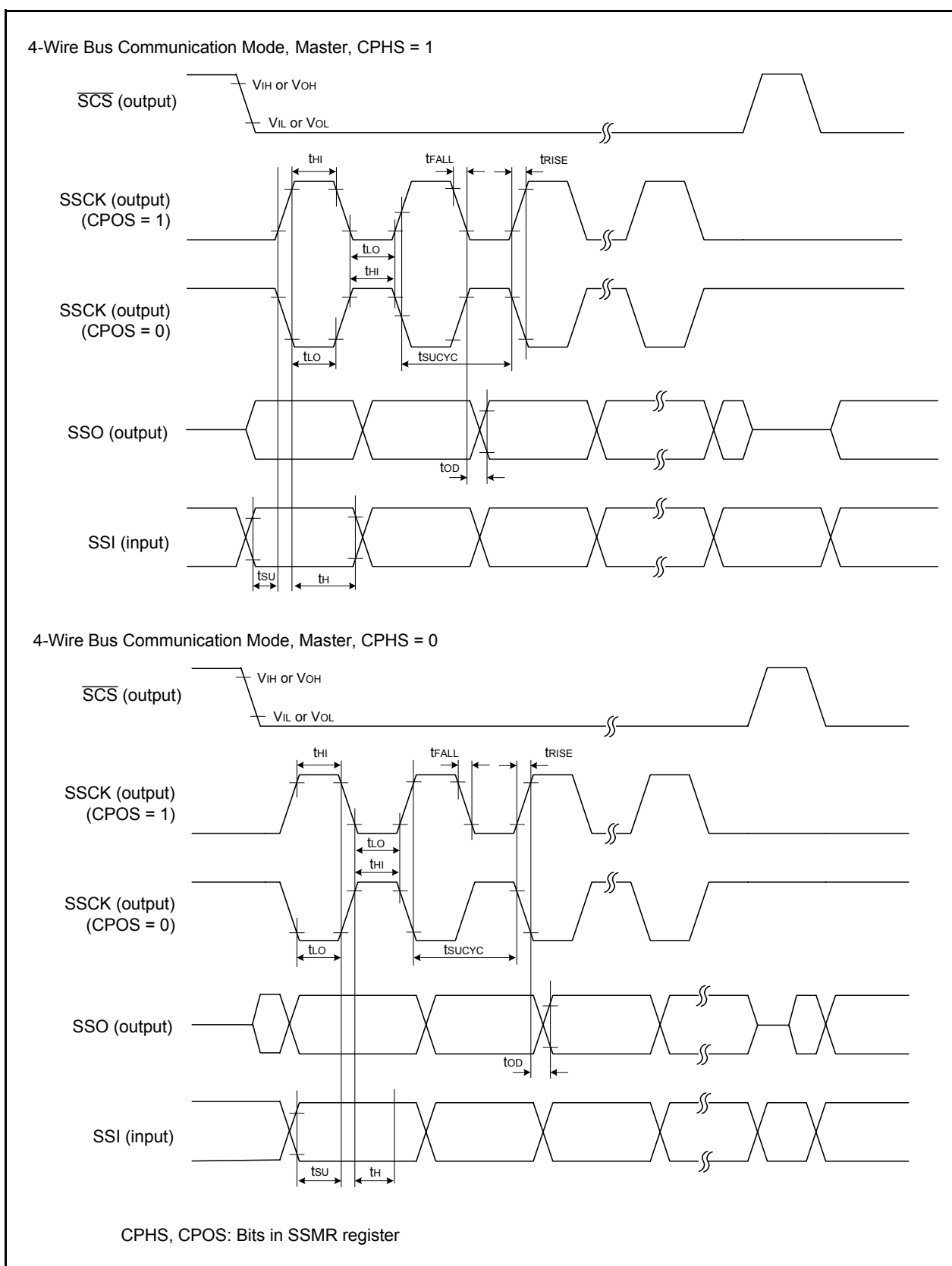


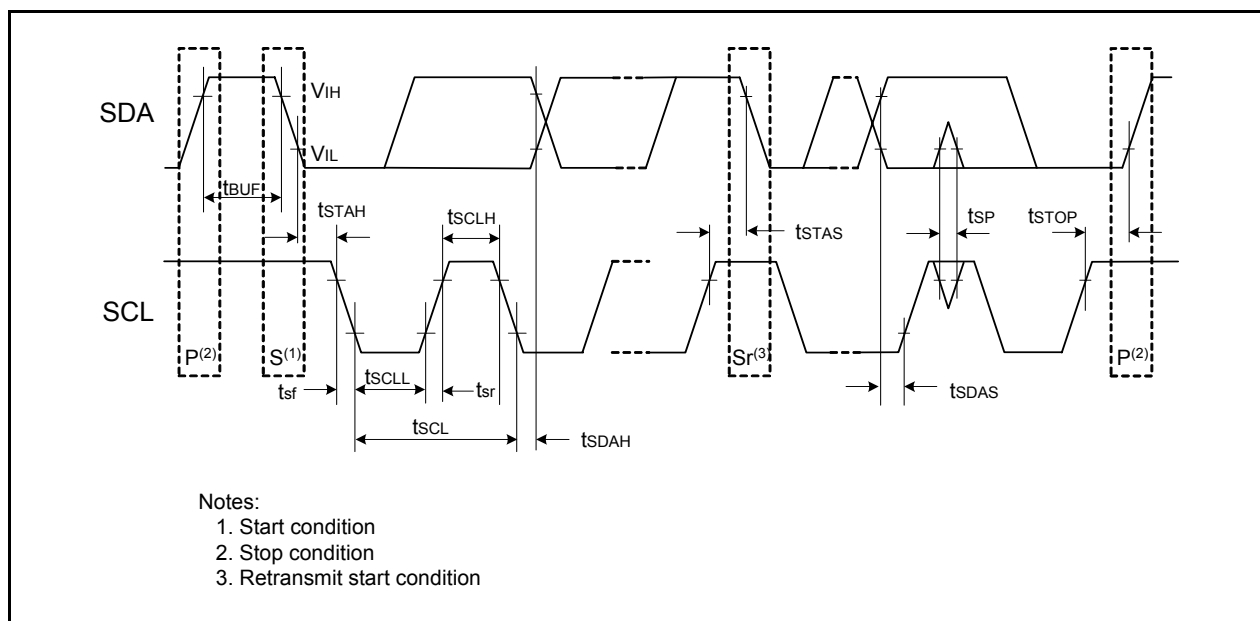
Figure 5.4 I/O Timing of Synchronous Serial Communication Unit (SSU) (Master)

Table 5.29 Timing Requirements of I²C bus Interface (1)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t _{SCL}	SCL input cycle time		12tcyc + 600 (2)	–	–	ns
t _{SCLH}	SCL input “H” width		3tcyc + 300 (2)	–	–	ns
t _{SCLL}	SCL input “L” width		5tcyc + 500 (2)	–	–	ns
t _{sf}	SCL, SDA input fall time		–	–	300	ns
t _{SP}	SCL, SDA input spike pulse rejection time		–	–	1tcyc (2)	ns
t _{BUF}	SDA input bus-free time		5tcyc (2)	–	–	ns
t _{STAH}	Start condition input hold time		3tcyc (2)	–	–	ns
t _{STAS}	Retransmit start condition input setup time		3tcyc (2)	–	–	ns
t _{STOP}	Stop condition input setup time		3tcyc (2)	–	–	ns
t _{SDAS}	Data input setup time		1tcyc + 40 (2)	–	–	ns
t _{SDAH}	Data input hold time		10	–	–	ns

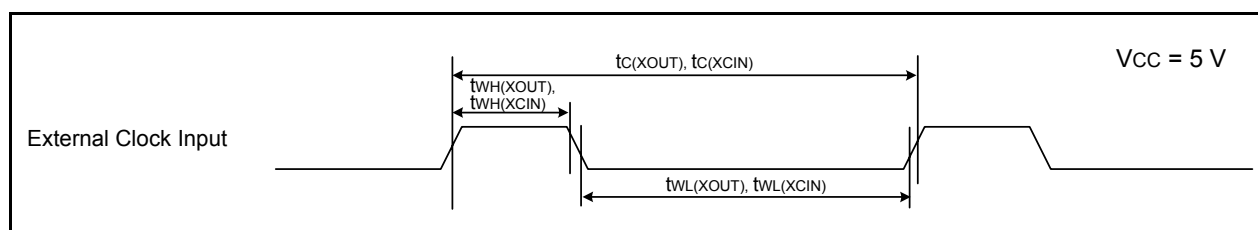
Notes:

1. V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V and T_{opr} = –20 to 85°C (N version), unless otherwise specified.
2. 1tcyc = 1/f₁(s)

**Figure 5.7 I/O Timing of I²C bus Interface**

Timing Requirements(Unless Otherwise Specified: $V_{CC} = 5\text{ V}$, $V_{SS} = 0\text{ V}$ at $T_{opr} = 25^{\circ}\text{C}$)**Table 5.32 External Clock Input (XOUT, XCIN)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XOUT)}$	XOUT input cycle time	50	–	ns
$t_{WH(XOUT)}$	XOUT input “H” width	24	–	ns
$t_{WL(XOUT)}$	XOUT input “L” width	24	–	ns
$t_{c(XCIN)}$	XCIN input cycle time	14	–	μs
$t_{WH(XCIN)}$	XCIN input “H” width	7	–	μs
$t_{WL(XCIN)}$	XCIN input “L” width	7	–	μs

**Figure 5.8 External Clock Input Timing Diagram when $V_{CC} = 5\text{ V}$** **Table 5.33 TRAIO Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	100	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	40	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	40	–	ns

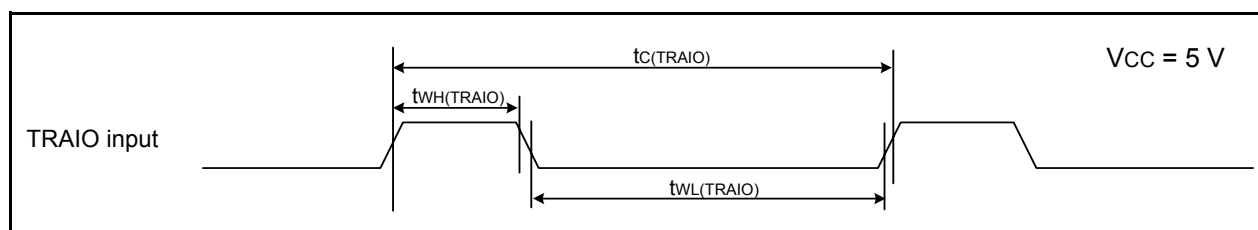
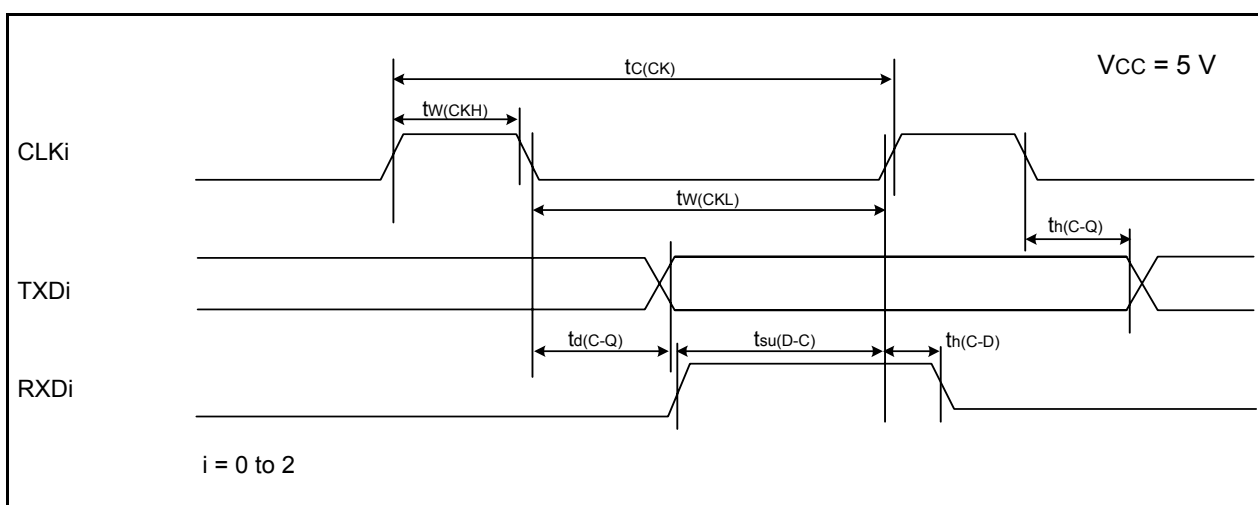
**Figure 5.9 TRAIO Input Timing Diagram when $V_{CC} = 5\text{ V}$**

Table 5.34 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200	—	ns
$t_{w(CKH)}$	CLKi input "H" width	100	—	ns
$t_{w(CKL)}$	CLKi input "L" width	100	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	50	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	50	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

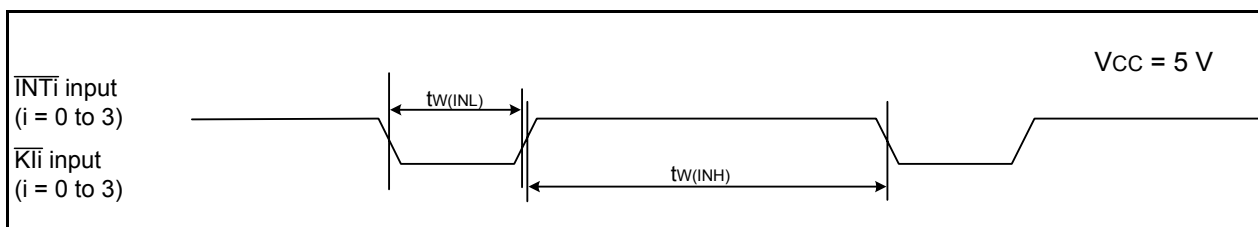
i = 0 to 2

**Figure 5.10 Serial Interface Timing Diagram when Vcc = 5 V****Table 5.35 External Interrupt $\overline{INTi}$ (i = 0 to 3) Input, Key Input Interrupt $\overline{Kli}$ (i = 0 to 3)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input "H" width, $\overline{Kli}$ input "H" width	250 (1)	—	ns
$t_{w(INL)}$	$\overline{INTi}$ input "L" width, $\overline{Kli}$ input "L" width	250 (2)	—	ns

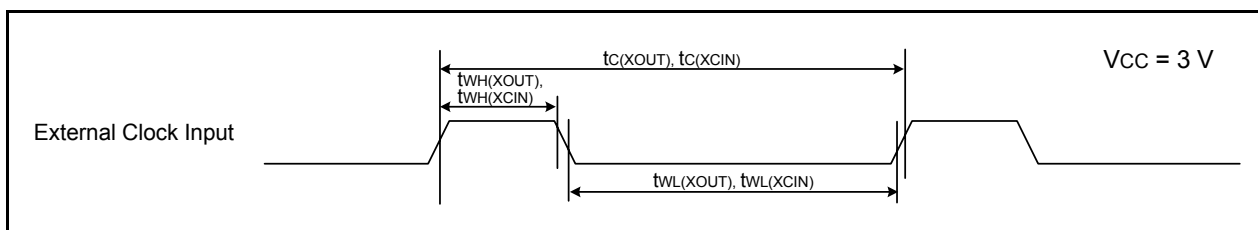
Notes:

1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency $\times$ 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency $\times$ 3) or the minimum value of standard, whichever is greater.

**Figure 5.11 Input Timing Diagram for External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{Kli}$ when Vcc = 5 V**

Timing Requirements(Unless Otherwise Specified: $V_{CC} = 3\text{ V}$, $V_{SS} = 0\text{ V}$ at $T_{op} = 25^{\circ}\text{C}$)**Table 5.38 External Clock Input (XOUT, XCIN)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XOUT)}$	XOUT input cycle time	50	–	ns
$t_{WH(XOUT)}$	XOUT input “H” width	24	–	ns
$t_{WL(XOUT)}$	XOUT input “L” width	24	–	ns
$t_{c(XCIN)}$	XCIN input cycle time	14	–	μs
$t_{WH(XCIN)}$	XCIN input “H” width	7	–	μs
$t_{WL(XCIN)}$	XCIN input “L” width	7	–	μs

**Figure 5.12 External Clock Input Timing Diagram when $V_{CC} = 3\text{ V}$** **Table 5.39 TRAIO Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	300	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	120	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	120	–	ns

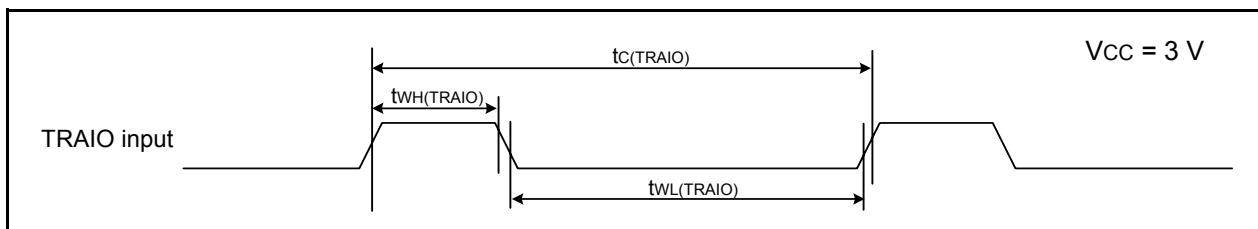
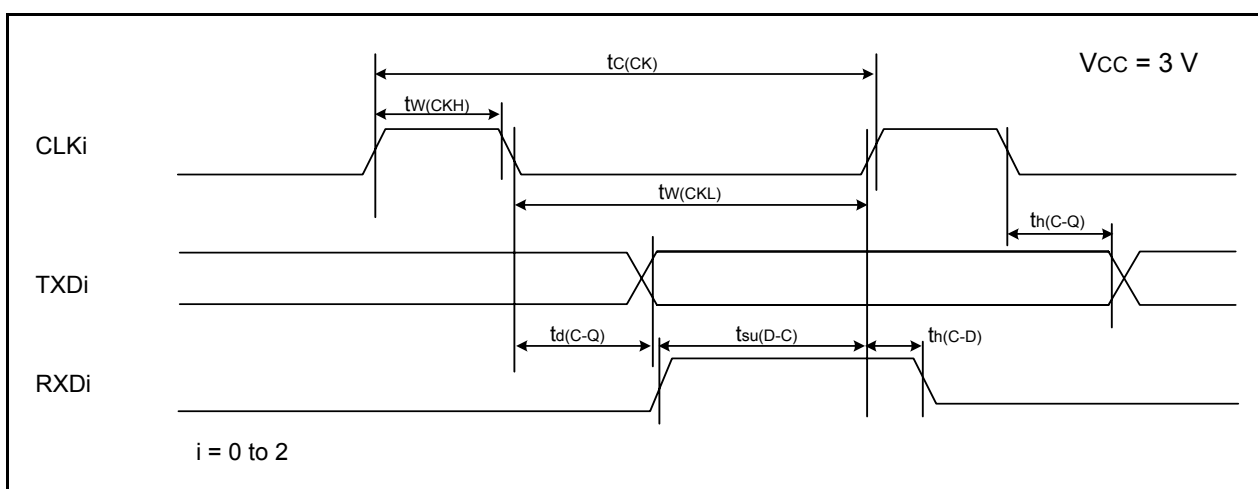
**Figure 5.13 TRAIO Input Timing Diagram when $V_{CC} = 3\text{ V}$**

Table 5.40 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300	—	ns
$t_{w(CKH)}$	CLKi input "H" width	150	—	ns
$t_{w(CKL)}$	CLKi Input "L" width	150	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	80	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	70	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

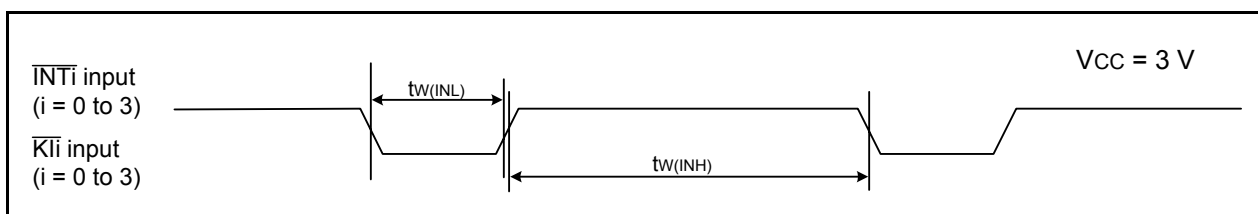
i = 0 to 2

**Figure 5.14 Serial Interface Timing Diagram when Vcc = 3 V****Table 5.41 External Interrupt $\overline{INTi}$ (i = 0 to 3) Input, Key Input Interrupt $\overline{Kli}$ (i = 0 to 3)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input "H" width, $\overline{Kli}$ input "H" width	380 (1)	—	ns
$t_{w(INL)}$	$\overline{INTi}$ input "L" width, $\overline{Kli}$ input "L" width	380 (2)	—	ns

Notes:

- When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
- When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

**Figure 5.15 Input Timing Diagram for External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{Kli}$ when Vcc = 3 V**

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

- The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.