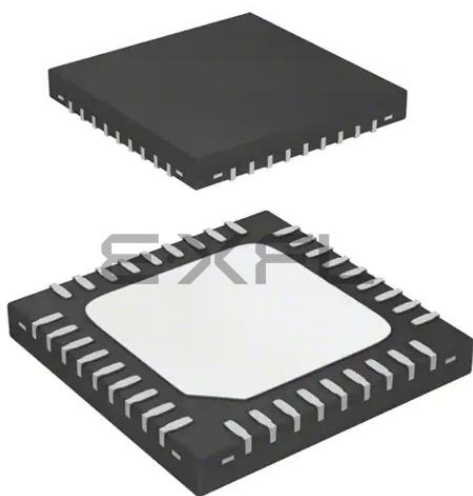




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Details

Product Status	Not For New Designs
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	31
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	2.5K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 10x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	36-WFQFN Exposed Pad
Supplier Device Package	36-HWQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f213j6cnp-w4

1.2 Product List

Table 1.3 lists Product List for R8C/3JC Group, and Figure 1.1 shows a Part Number, Memory Size, and Package of R8C/3JC Group.

Table 1.3 Product List for R8C/3JC Group

Current of May 2010

Part No.	ROM Capacity		RAM Capacity	Package Type	Remarks
	Program ROM	Data flash			
R5F213J2CNNP	8 Kbytes	1 Kbyte × 4	1 Kbyte	PWQN0036KA-B	N version
R5F213J4CNNP	16 Kbytes	1 Kbyte × 4	1.5 Kbytes	PWQN0036KA-B	
R5F213J5CNNP	24 Kbytes	1 Kbyte × 4	2 Kbytes	PWQN0036KA-B	
R5F213J6CNNP	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PWQN0036KA-B	

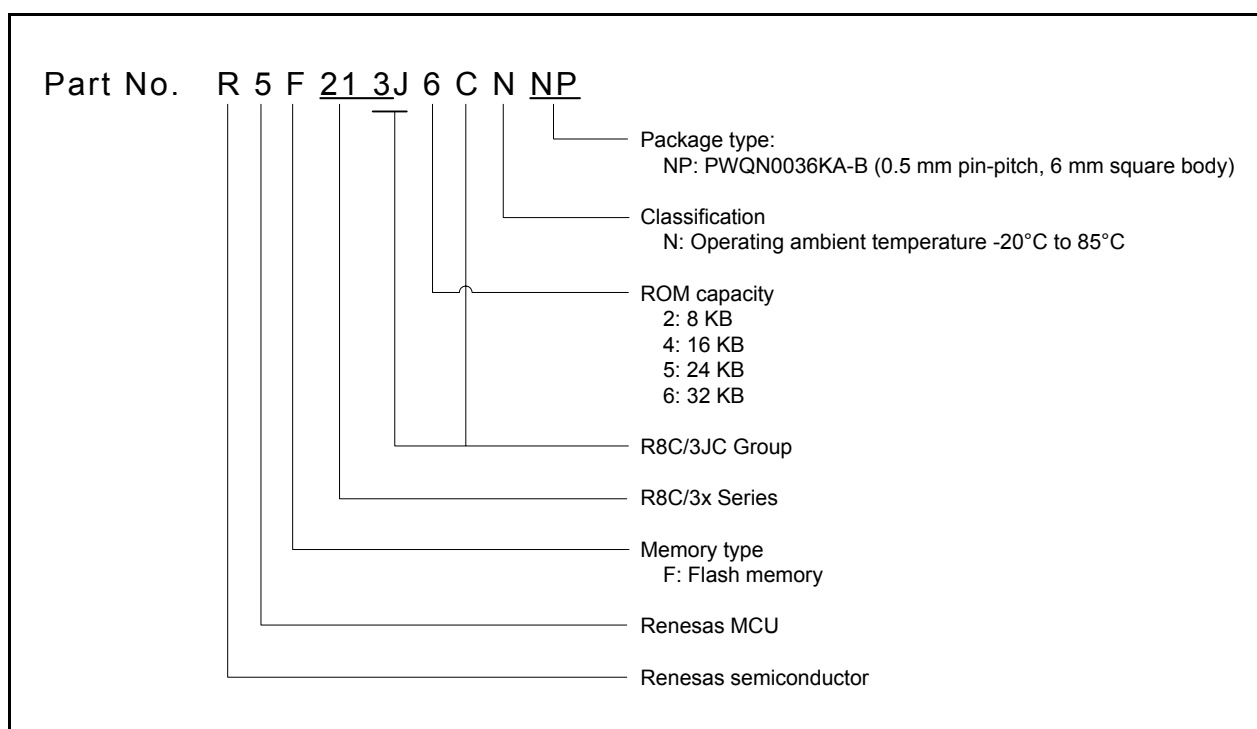


Figure 1.1 Part Number, Memory Size, and Package of R8C/3JC Group

1.4 Pin Assignment

Figure 1.3 shows Pin Assignment (Top View). Tables 1.4 and 1.5 outline the Pin Name Information by Pin Number.

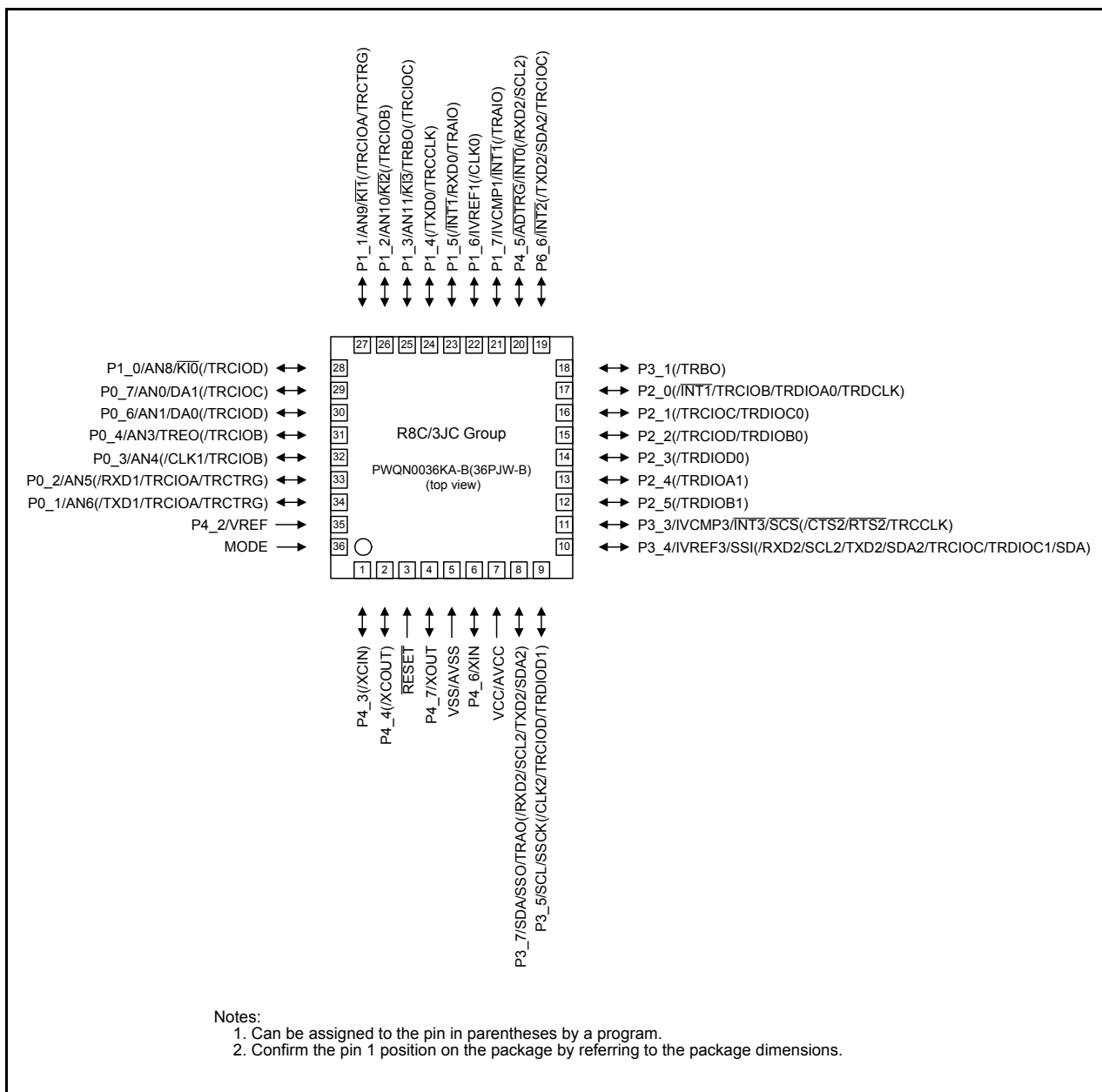


Figure 1.3 Pin Assignment (Top View)

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the starting address of an interrupt vector table.

2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.12 list the special function registers. Table 4.13 lists the ID Code Areas and Option Function Select Area.

Table 4.1 SFR Information (1) (1)

Address	Register	Symbol	After Reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	00101000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h	Module Standby Control Register	MSTCR	00h
0009h	System Clock Control Register 3	CM3	00h
000Ah	Protect Register	PRCR	00h
000Bh	Reset Source Determination Register	RSTFR	0XXXXXXb (2)
000Ch	Oscillation Stop Detection Register	OCD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDTC	00111111b
0010h			
0011h			
0012h			
0013h			
0014h			
0015h	High-Speed On-Chip Oscillator Control Register 7	FRA7	When shipping
0016h			
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h 10000000b (3)
001Dh			
001Eh			
001Fh			
0020h			
0021h			
0022h			
0023h	High-Speed On-Chip Oscillator Control Register 0	FRA0	00h
0024h	High-Speed On-Chip Oscillator Control Register 1	FRA1	When shipping
0025h	High-Speed On-Chip Oscillator Control Register 2	FRA2	00h
0026h	On-Chip Reference Voltage Control Register	OCVREFCR	00h
0027h			
0028h	Clock Prescaler Reset Flag	CPSRF	00h
0029h	High-Speed On-Chip Oscillator Control Register 4	FRA4	When Shipping
002Ah	High-Speed On-Chip Oscillator Control Register 5	FRA5	When Shipping
002Bh	High-Speed On-Chip Oscillator Control Register 6	FRA6	When Shipping
002Ch			
002Dh			
002Eh			
002Fh	High-Speed On-Chip Oscillator Control Register 3	FRA3	When shipping
0030h	Voltage Monitor Circuit Control Register	CMPA	00h
0031h	Voltage Monitor Circuit Edge Select Register	VCAC	00h
0032h			
0033h	Voltage Detect Register 1	VCA1	00001000b
0034h	Voltage Detect Register 2	VCA2	00h (4) 00100000b (5)
0035h			
0036h	Voltage Detection 1 Level Select Register	VD1LS	00000111b
0037h			
0038h	Voltage Monitor 0 Circuit Control Register	VW0C	1100X010b (4) 1100X011b (5)
0039h	Voltage Monitor 1 Circuit Control Register	VW1C	10001010b

X: Undefined

Notes:

1. The blank areas are reserved and cannot be accessed by users.
2. The CWR bit in the RSTFR register is set to 0 after power-on and voltage monitor 0 reset. Hardware reset, software reset, or watchdog timer reset does not affect this bit.
3. The CSPROINI bit in the OFS register is set to 0.
4. The LVDAS bit in the OFS register is set to 1.
5. The LVDAS bit in the OFS register is set to 0.

Table 4.4 SFR Information (4) (1)

Address	Register	Symbol	After Reset
00C0h	A/D Register 0	AD0	XXh
00C1h			000000XXb
00C2h	A/D Register 1	AD1	XXh
00C3h			000000XXb
00C4h	A/D Register 2	AD2	XXh
00C5h			000000XXb
00C6h	A/D Register 3	AD3	XXh
00C7h			000000XXb
00C8h	A/D Register 4	AD4	XXh
00C9h			000000XXb
00CAh	A/D Register 5	AD5	XXh
00CBh			000000XXb
00CCh	A/D Register 6	AD6	XXh
00CDh			000000XXb
00CEh	A/D Register 7	AD7	XXh
00CFh			000000XXb
00D0h			
00D1h			
00D2h			
00D3h			
00D4h	A/D Mode Register	ADMOD	00h
00D5h	A/D Input Select Register	ADINSEL	11000000b
00D6h	A/D Control Register 0	ADCON0	00h
00D7h	A/D Control Register 1	ADCON1	00h
00D8h	D/A0 Register	DA0	00h
00D9h	D/A1 Register	DA1	00h
00DAh			
00DBh			
00DCh	D/A Control Register	DACON	00h
00DDh			
00DEh			
00DFh			
00E0h	Port P0 Register	P0	XXh
00E1h	Port P1 Register	P1	XXh
00E2h	Port P0 Direction Register	PD0	00h
00E3h	Port P1 Direction Register	PD1	00h
00E4h	Port P2 Register	P2	XXh
00E5h	Port P3 Register	P3	XXh
00E6h	Port P2 Direction Register	PD2	00h
00E7h	Port P3 Direction Register	PD3	00h
00E8h	Port P4 Register	P4	XXh
00E9h			
00EAh	Port P4 Direction Register	PD4	00h
00EBh			
00ECh	Port P6 Register	P6	XXh
00EDh			
00EEh	Port P6 Direction Register	PD6	00h
00EFh			
00F0h			
00F1h			
00F2h			
00F3h			
00F4h			
00F5h			
00F6h			
00F7h			
00F8h			
00F9h			
00FAh			
00FBh			
00FCh			
00FDh			
00FEh			
00FFh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.6 SFR Information (6) (1)

Address	Register	Symbol	After Reset
0140h	Timer RD Control Register 0	TRDCR0	00h
0141h	Timer RD I/O Control Register A0	TRDIOA0	10001000b
0142h	Timer RD I/O Control Register C0	TRDIOCR0	10001000b
0143h	Timer RD Status Register 0	TRDSR0	11100000b
0144h	Timer RD Interrupt Enable Register 0	TRDIER0	11100000b
0145h	Timer RD PWM Mode Output Level Control Register 0	TRDPOCR0	11111000b
0146h	Timer RD Counter 0	TRD0	00h
0147h			00h
0148h	Timer RD General Register A0	TRDGRA0	FFh
0149h			FFh
014Ah	Timer RD General Register B0	TRDGRB0	FFh
014Bh			FFh
014Ch	Timer RD General Register C0	TRDGRC0	FFh
014Dh			FFh
014Eh	Timer RD General Register D0	TRDGRD0	FFh
014Fh			FFh
0150h	Timer RD Control Register 1	TRDCR1	00h
0151h	Timer RD I/O Control Register A1	TRDIOA1	10001000b
0152h	Timer RD I/O Control Register C1	TRDIOCR1	10001000b
0153h	Timer RD Status Register 1	TRDSR1	11000000b
0154h	Timer RD Interrupt Enable Register 1	TRDIER1	11100000b
0155h	Timer RD PWM Mode Output Level Control Register 1	TRDPOCR1	11111000b
0156h	Timer RD Counter 1	TRD1	00h
0157h			00h
0158h	Timer RD General Register A1	TRDGRA1	FFh
0159h			FFh
015Ah	Timer RD General Register B1	TRDGRB1	FFh
015Bh			FFh
015Ch	Timer RD General Register C1	TRDGRC1	FFh
015Dh			FFh
015Eh	Timer RD General Register D1	TRDGRD1	FFh
015Fh			FFh
0160h	UART1 Transmit/Receive Mode Register	U1MR	00h
0161h	UART1 Bit Rate Register	U1BRG	XXh
0162h	UART1 Transmit Buffer Register	U1TB	XXh
0163h			XXh
0164h	UART1 Transmit/Receive Control Register 0	U1C0	00001000b
0165h	UART1 Transmit/Receive Control Register 1	U1C1	00000010b
0166h	UART1 Receive Buffer Register	U1RB	XXh
0167h			XXh
0168h			
0169h			
016Ah			
016Bh			
016Ch			
016Dh			
016Eh			
016Fh			
0170h			
0171h			
0172h			
0173h			
0174h			
0175h			
0176h			
0177h			
0178h			
0179h			
017Ah			
017Bh			
017Ch			
017Dh			
017Eh			
017Fh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.10 SFR Information (10) (1)

Address	Register	Symbol	After Reset
2C70h	DTC Control Data 6	DTCD6	XXh
2C71h			XXh
2C72h			XXh
2C73h			XXh
2C74h			XXh
2C75h			XXh
2C76h			XXh
2C77h			XXh
2C78h	DTC Control Data 7	DTCD7	XXh
2C79h			XXh
2C7Ah			XXh
2C7Bh			XXh
2C7Ch			XXh
2C7Dh			XXh
2C7Eh			XXh
2C7Fh			XXh
2C80h	DTC Control Data 8	DTCD8	XXh
2C81h			XXh
2C82h			XXh
2C83h			XXh
2C84h			XXh
2C85h			XXh
2C86h			XXh
2C87h			XXh
2C88h	DTC Control Data 9	DTCD9	XXh
2C89h			XXh
2C8Ah			XXh
2C8Bh			XXh
2C8Ch			XXh
2C8Dh			XXh
2C8Eh			XXh
2C8Fh			XXh
2C90h	DTC Control Data 10	DTCD10	XXh
2C91h			XXh
2C92h			XXh
2C93h			XXh
2C94h			XXh
2C95h			XXh
2C96h			XXh
2C97h			XXh
2C98h	DTC Control Data 11	DTCD11	XXh
2C99h			XXh
2C9Ah			XXh
2C9Bh			XXh
2C9Ch			XXh
2C9Dh			XXh
2C9Eh			XXh
2C9Fh			XXh
2CA0h	DTC Control Data 12	DTCD12	XXh
2CA1h			XXh
2CA2h			XXh
2CA3h			XXh
2CA4h			XXh
2CA5h			XXh
2CA6h			XXh
2CA7h			XXh
2CA8h	DTC Control Data 13	DTCD13	XXh
2CA9h			XXh
2CAAh			XXh
2CABh			XXh
2CACH			XXh
2CADh			XXh
2CAEh			XXh
2CAFh			XXh

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.11 SFR Information (11) (1)

Address	Register	Symbol	After Reset
2CB0h	DTC Control Data 14	DTCD14	XXh
2CB1h			XXh
2CB2h			XXh
2CB3h			XXh
2CB4h			XXh
2CB5h			XXh
2CB6h			XXh
2CB7h			XXh
2CB8h	DTC Control Data 15	DTCD15	XXh
2CB9h			XXh
2CBAh			XXh
2CBBh			XXh
2CBCh			XXh
2CBDh			XXh
2CBEh			XXh
2CBFh			XXh
2CC0h	DTC Control Data 16	DTCD16	XXh
2CC1h			XXh
2CC2h			XXh
2CC3h			XXh
2CC4h			XXh
2CC5h			XXh
2CC6h			XXh
2CC7h			XXh
2CC8h	DTC Control Data 17	DTCD17	XXh
2CC9h			XXh
2CCAh			XXh
2CCBh			XXh
2CCCh			XXh
2CCDh			XXh
2CCEh			XXh
2CCFh			XXh
2CD0h	DTC Control Data 18	DTCD18	XXh
2CD1h			XXh
2CD2h			XXh
2CD3h			XXh
2CD4h			XXh
2CD5h			XXh
2CD6h			XXh
2CD7h			XXh
2CD8h	DTC Control Data 19	DTCD19	XXh
2CD9h			XXh
2CDAh			XXh
2CDBh			XXh
2CDCh			XXh
2CDDh			XXh
2CDEh			XXh
2CDFh			XXh
2CE0h	DTC Control Data 20	DTCD20	XXh
2CE1h			XXh
2CE2h			XXh
2CE3h			XXh
2CE4h			XXh
2CE5h			XXh
2CE6h			XXh
2CE7h			XXh
2CE8h	DTC Control Data 21	DTCD21	XXh
2CE9h			XXh
2CEAh			XXh
2CEBh			XXh
2CECh			XXh
2CEDh			XXh
2CEEh			XXh
2CEFh			XXh

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 5.16 A/D Converter Characteristics

Symbol	Parameter		Conditions		Standard			Unit
					Min.	Typ.	Max.	
–	Resolution		Vref = AVcc		–	–	10	Bit
–	Absolute accuracy	10-bit mode	Vref = AVcc = 5.0 V	AN0 to AN1 input, AN3 to AN6 input, AN8 to AN11 input	–	–	±3	LSB
			Vref = AVcc = 3.3 V	AN0 to AN1 input, AN3 to AN6 input, AN8 to AN11 input	–	–	±5	LSB
			Vref = AVcc = 3.0 V	AN0 to AN1 input, AN3 to AN6 input, AN8 to AN11 input	–	–	±5	LSB
			Vref = AVcc = 2.2 V	AN0 to AN1 input, AN3 to AN6 input, AN8 to AN11 input	–	–	±5	LSB
		8-bit mode	Vref = AVcc = 5.0 V	AN0 to AN1 input, AN3 to AN6 input, AN8 to AN11 input	–	–	±2	LSB
			Vref = AVcc = 3.3 V	AN0 to AN1 input, AN3 to AN6 input, AN8 to AN11 input	–	–	±2	LSB
			Vref = AVcc = 3.0 V	AN0 to AN1 input, AN3 to AN6 input, AN8 to AN11 input	–	–	±2	LSB
			Vref = AVcc = 2.2 V	AN0 to AN1 input, AN3 to AN6 input, AN8 to AN11 input	–	–	±2	LSB
φAD	A/D conversion clock		4.0 V ≤ Vref = AVcc ≤ 5.5 V ⁽²⁾		2	–	20	MHz
			3.2 V ≤ Vref = AVcc ≤ 5.5 V ⁽²⁾		2	–	16	MHz
			2.7 V ≤ Vref = AVcc ≤ 5.5 V ⁽²⁾		2	–	10	MHz
			2.2 V ≤ Vref = AVcc ≤ 5.5 V ⁽²⁾		2	–	5	MHz
–	Tolerance level impedance				–	3	–	kΩ
tCONV	Conversion time	10-bit mode	Vref = AVcc = 5.0 V, φAD = 20 MHz		2.15	–	–	μs
		8-bit mode	Vref = AVcc = 5.0 V, φAD = 20 MHz		2.15	–	–	μs
tsAMP	Sampling time		φAD = 20 MHz		0.75	–	–	μs
Ivref	Vref current		Vcc = 5 V, XIN = f1 = φAD = 20 MHz		–	45	–	μA
Vref	Reference voltage				2.2	–	AVcc	V
VIA	Analog input voltage ⁽³⁾				0	–	Vref	V
OCVREF	On-chip reference voltage		2 MHz ≤ φAD ≤ 4 MHz		1.19	1.34	1.49	V

Notes:

1. $V_{CC}/AV_{CC} = V_{ref} = 2.2$ to 5.5 V , $V_{SS} = 0\text{ V}$ and $T_{opr} = -20$ to 85°C (N version), unless otherwise specified.
2. The A/D conversion result will be undefined in wait mode, stop mode, when the flash memory stops, and in low-current-consumption mode. Do not perform A/D conversion in these states or transition to these states during A/D conversion.
3. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

Table 5.17 D/A Converter Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
—	Resolution		—	—	8	Bit
—	Absolute accuracy		—	—	2.5	LSB
t_{su}	Setup time		—	—	3	μs
R_o	Output resistor		—	6	—	$k\Omega$
I_{Vref}	Reference power input current	(Note 2)	—	—	1.5	mA

Notes:

1. $V_{CC}/AV_{CC} = V_{ref} = 2.7$ to 5.5 V and $T_{opr} = -20$ to $85^{\circ}C$ (N version), unless otherwise specified.
2. This applies when one D/A converter is used and the value of the DAI register ($i = 0$ or 1) for the unused D/A converter is 00h. The resistor ladder of the A/D converter is not included.

Table 5.18 Comparator B Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{ref}	IVREF1, IVREF3 input reference voltage		0	—	$V_{CC} - 1.4$	V
V_I	IVCMP1, IVCMP3 input voltage		-0.3	—	$V_{CC} + 0.3$	V
—	Offset		—	5	100	mV
t_d	Comparator output delay time ⁽²⁾	$V_I = V_{ref} \pm 100$ mV	—	0.1	—	μs
I_{CMP}	Comparator operating current	$V_{CC} = 5.0$ V	—	17.5	—	μA

Notes:

1. $V_{CC} = 2.7$ to 5.5 V, $T_{opr} = -20$ to $85^{\circ}C$ (N version), unless otherwise specified.
2. When the digital filter is disabled.

Table 5.23 Voltage Detection 2 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet2	Voltage detection level Vdet2_0	At the falling of Vcc	3.70	4.00	4.30	V
—	Hysteresis width at the rising of Vcc in voltage detection 2 circuit		—	0.10	—	V
—	Voltage detection 2 circuit response time ⁽²⁾	At the falling of Vcc from 5 V to (Vdet2_0 – 0.1) V	—	20	150	μs
—	Voltage detection circuit self power consumption	VCA27 = 1, Vcc = 5.0 V	—	1.7	—	μA
td(E-A)	Waiting time until voltage detection circuit operation starts ⁽³⁾		—	—	100	μs

Notes:

1. The measurement condition is Vcc = 1.8 V to 5.5 V and T_{opr} = –20 to 85°C (N version).
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes Vdet2.
3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

Table 5.24 Power-on Reset Circuit (2)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
trth	External power Vcc rise gradient	⁽¹⁾	0	—	50,000	mV/msec

Notes:

1. The measurement condition is T_{opr} = –20 to 85°C (N version), unless otherwise specified.
2. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.

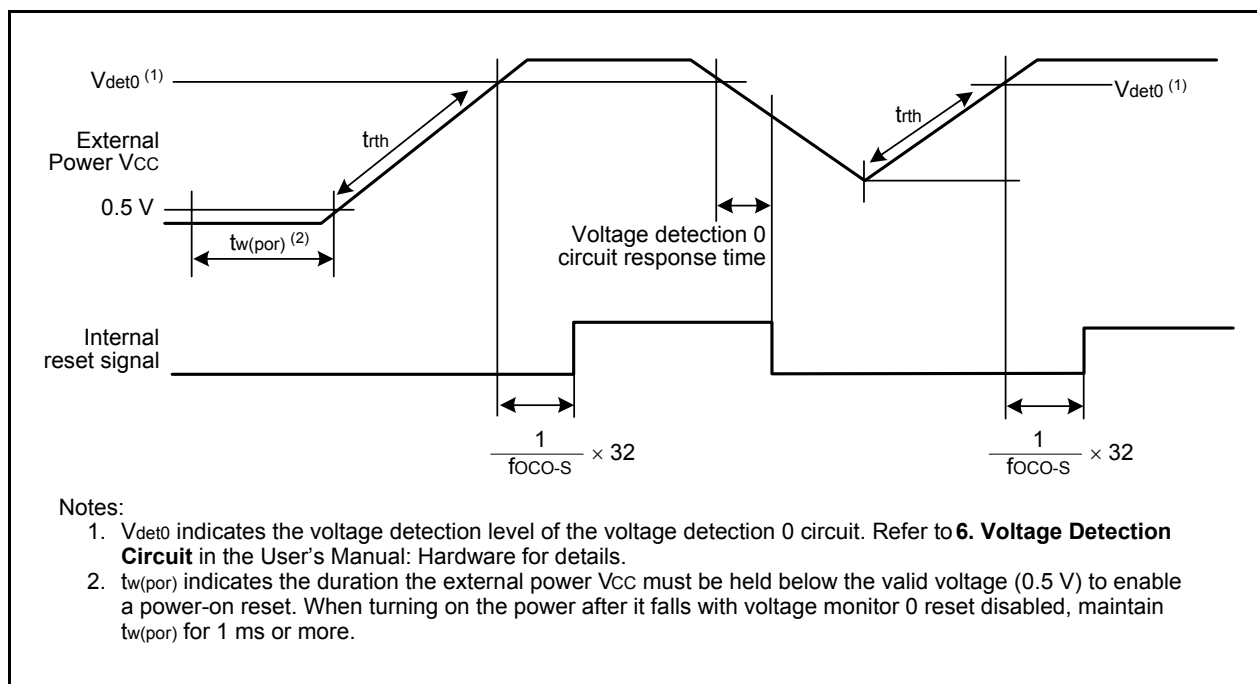
**Figure 5.3 Power-on Reset Circuit Electrical Characteristics**

Table 5.28 Timing Requirements of Synchronous Serial Communication Unit (SSU) (1)

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
tsucyc	SSCK clock cycle time			4	–	–	tcyc (2)
tHI	SSCK clock "H" width			0.4	–	0.6	tsucyc
tLO	SSCK clock "L" width			0.4	–	0.6	tsucyc
tRISE	SSCK clock rising time	Master		–	–	1	tcyc (2)
		Slave		–	–	1	μs
tFALL	SSCK clock falling time	Master		–	–	1	tcyc (2)
		Slave		–	–	1	μs
tsu	SSO, SSI data input setup time			100	–	–	ns
tH	SSO, SSI data input hold time			1	–	–	tcyc (2)
tLEAD	SCS setup time	Slave		1tcyc + 50	–	–	ns
tLAG	SCS hold time	Slave		1tcyc + 50	–	–	ns
tOD	SSO, SSI data output delay time			–	–	1	tcyc (2)
tsa	SSI slave access time		2.7 V ≤ Vcc ≤ 5.5 V	–	–	1.5tcyc + 100	ns
			1.8 V ≤ Vcc < 2.7 V	–	–	1.5tcyc + 200	ns
tor	SSI slave out open time		2.7 V ≤ Vcc ≤ 5.5 V	–	–	1.5tcyc + 100	ns
			1.8 V ≤ Vcc < 2.7 V	–	–	1.5tcyc + 200	ns

Notes:

1. Vcc = 1.8 to 5.5 V, Vss = 0 V and Topr = –20 to 85°C (N version), unless otherwise specified.
2. 1tcyc = 1/f1(s)

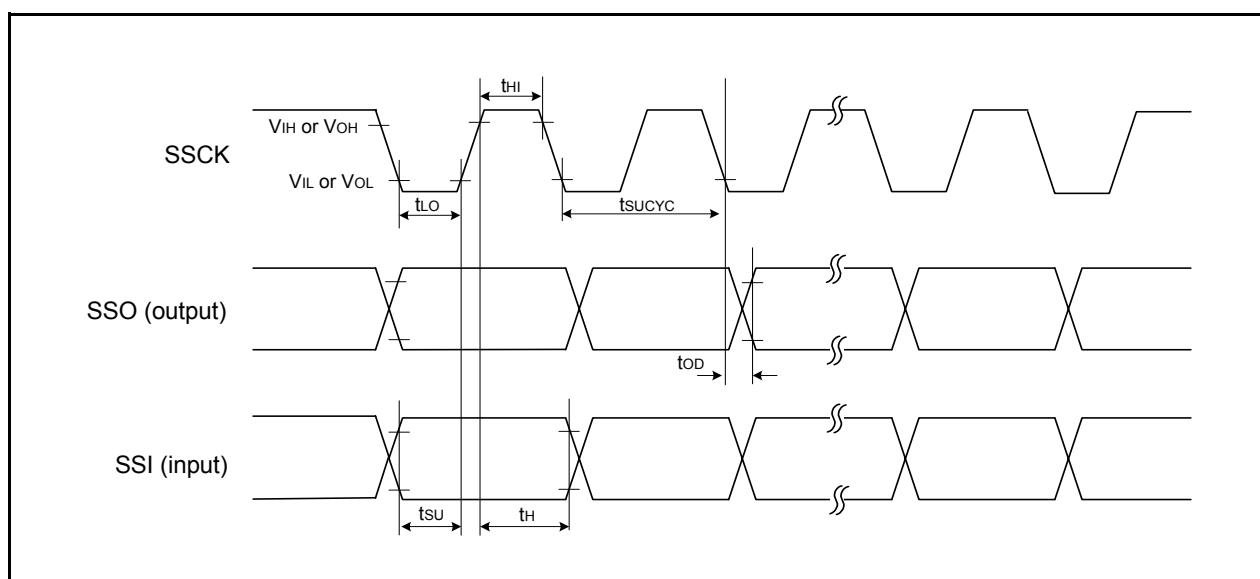
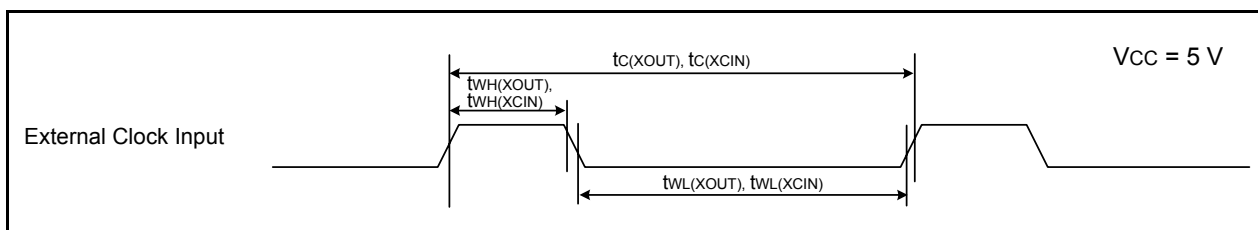


Figure 5.6 I/O Timing of Synchronous Serial Communication Unit (SSU) (Clock Synchronous Communication Mode)

Timing Requirements(Unless Otherwise Specified: $V_{CC} = 5\text{ V}$, $V_{SS} = 0\text{ V}$ at $T_{opr} = 25^\circ\text{C}$)**Table 5.32 External Clock Input (XOUT, XCIN)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XOUT)}$	XOUT input cycle time	50	–	ns
$t_{WH(XOUT)}$	XOUT input “H” width	24	–	ns
$t_{WL(XOUT)}$	XOUT input “L” width	24	–	ns
$t_{c(XCIN)}$	XCIN input cycle time	14	–	μs
$t_{WH(XCIN)}$	XCIN input “H” width	7	–	μs
$t_{WL(XCIN)}$	XCIN input “L” width	7	–	μs

**Figure 5.8 External Clock Input Timing Diagram when $V_{CC} = 5\text{ V}$** **Table 5.33 TRAIO Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	100	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	40	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	40	–	ns

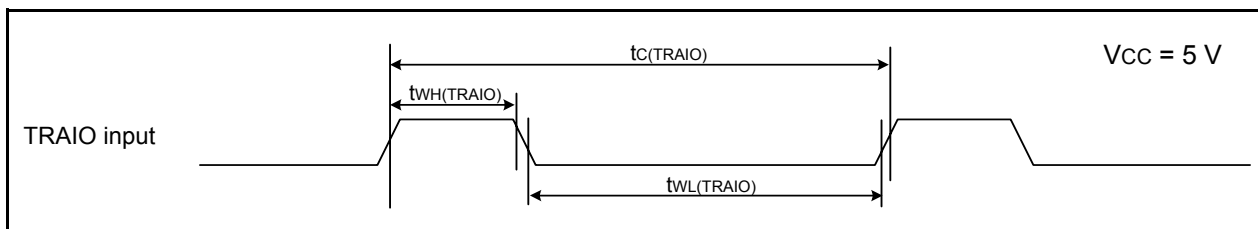
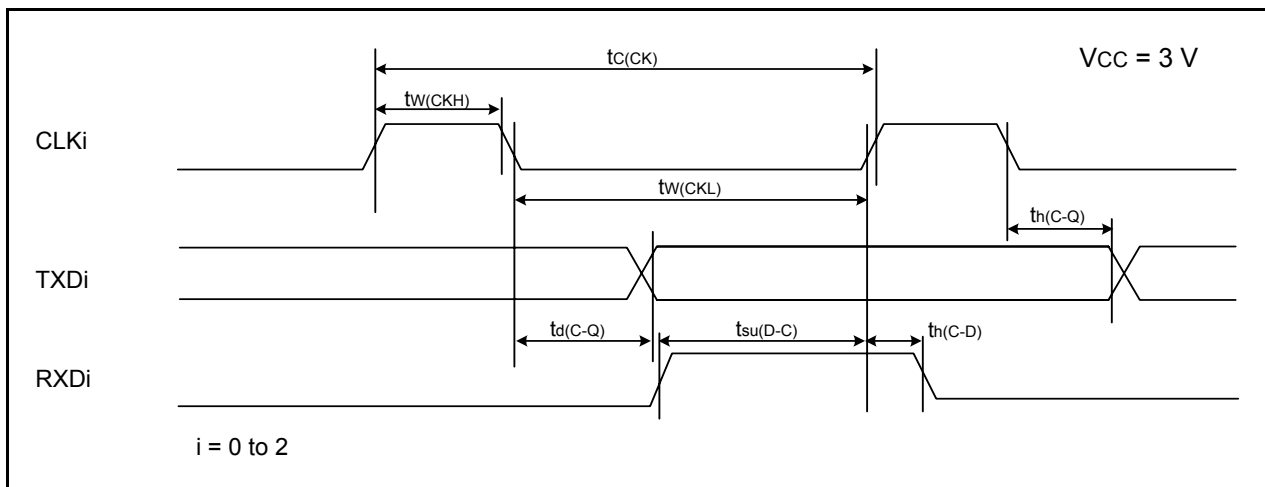
**Figure 5.9 TRAIO Input Timing Diagram when $V_{CC} = 5\text{ V}$**

Table 5.37 Electrical Characteristics (4) [$2.7\text{ V} \leq V_{CC} < 3.3\text{ V}$]
($T_{opr} = -20$ to 85°C (N version), unless otherwise specified.)

Symbol	Parameter		Condition	Standard			Unit
				Min.	Typ.	Max.	
I _{CC}	Power supply current (V _{CC} = 2.7 to 3.3 V) Single-chip mode, output pins are open, other pins are V _{SS}	High-speed clock mode	XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	3.5	10	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	1.5	7.5	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	7.0	15	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	3.0	–	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	4.0	–	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	1.5	–	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 4 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-16 MSTIIC = MSTTRD = MSTTRC = 1	–	1	–	mA
			Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	–	90	390
		Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division, FMR27 = 1, VCA20 = 0	–	80	400	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division, Program operation on RAM Flash memory off, FMSTP = 1, VCA20 = 0	–	40	–	μA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	–	15	90	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	–	4	80	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (peripheral clock off) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	–	3.5	–	μA
		Stop mode	XIN clock off, T _{opr} = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	2.0	5.0	μA
			XIN clock off, T _{opr} = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	5.0	–	μA

Table 5.40 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300	—	ns
$t_{w(CKH)}$	CLKi input "H" width	150	—	ns
$t_{w(CKL)}$	CLKi Input "L" width	150	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	80	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	70	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

 $i = 0 \text{ to } 2$ **Figure 5.14 Serial Interface Timing Diagram when Vcc = 3 V****Table 5.41 External Interrupt $\overline{INTi}$ ($i = 0 \text{ to } 3$) Input, Key Input Interrupt $\overline{Kli}$ ($i = 0 \text{ to } 3$)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input "H" width, $\overline{Kli}$ input "H" width	380 (1)	—	ns
$t_{w(INL)}$	$\overline{INTi}$ input "L" width, $\overline{Kli}$ input "L" width	380 (2)	—	ns

Notes:

- When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency $\times$ 3) or the minimum value of standard, whichever is greater.
- When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency $\times$ 3) or the minimum value of standard, whichever is greater.

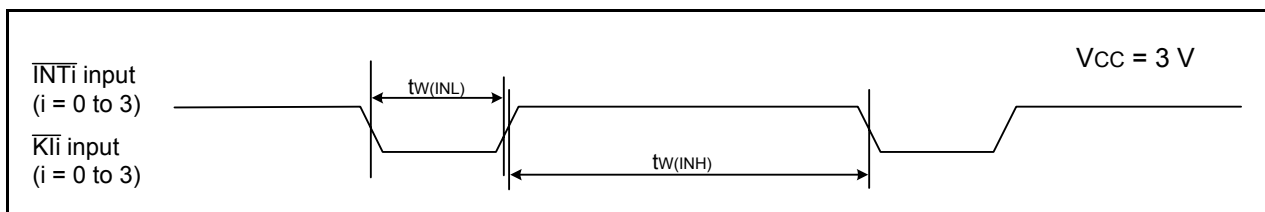
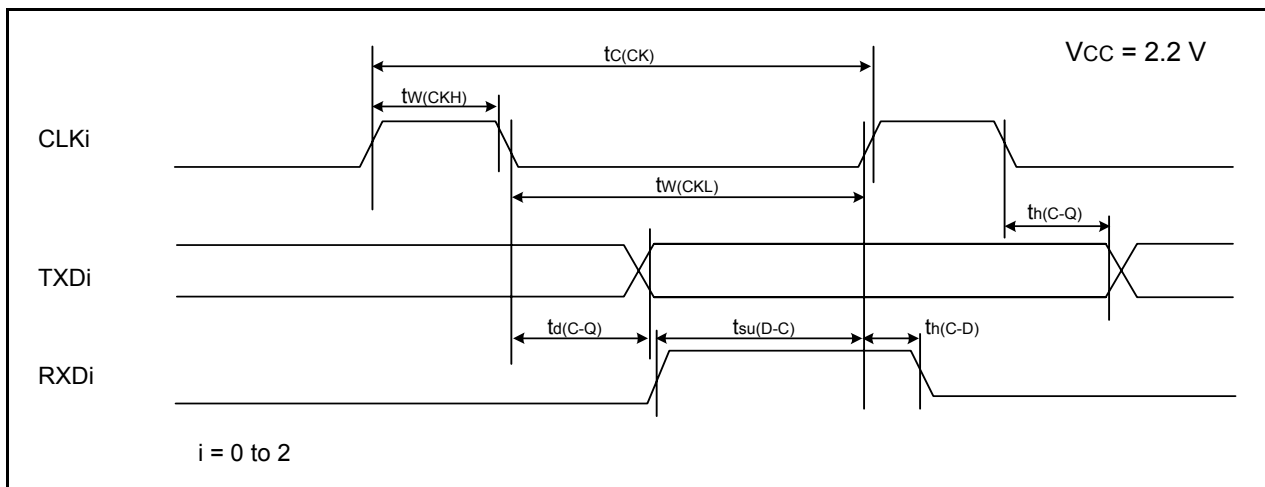
**Figure 5.15 Input Timing Diagram for External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{Kli}$ when Vcc = 3 V**

Table 5.46 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	800	—	ns
$t_{w(CKH)}$	CLKi input "H" width	400	—	ns
$t_{w(CKL)}$	CLKi input "L" width	400	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	200	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	150	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

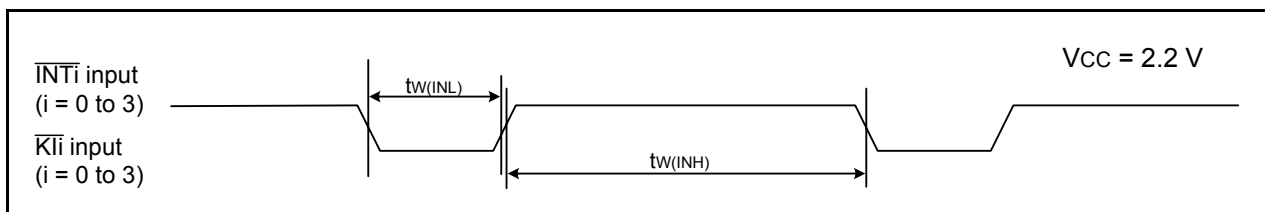
i = 0 to 2

**Figure 5.18 Serial Interface Timing Diagram when Vcc = 2.2 V****Table 5.47 External Interrupt $\overline{INTi}$ (i = 0 to 3) Input, Key Input Interrupt $\overline{Kli}$ (i = 0 to 3)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input "H" width, $\overline{Kli}$ input "H" width	1000 (1)	—	ns
$t_{w(INL)}$	$\overline{INTi}$ input "L" width, $\overline{Kli}$ input "L" width	1000 (2)	—	ns

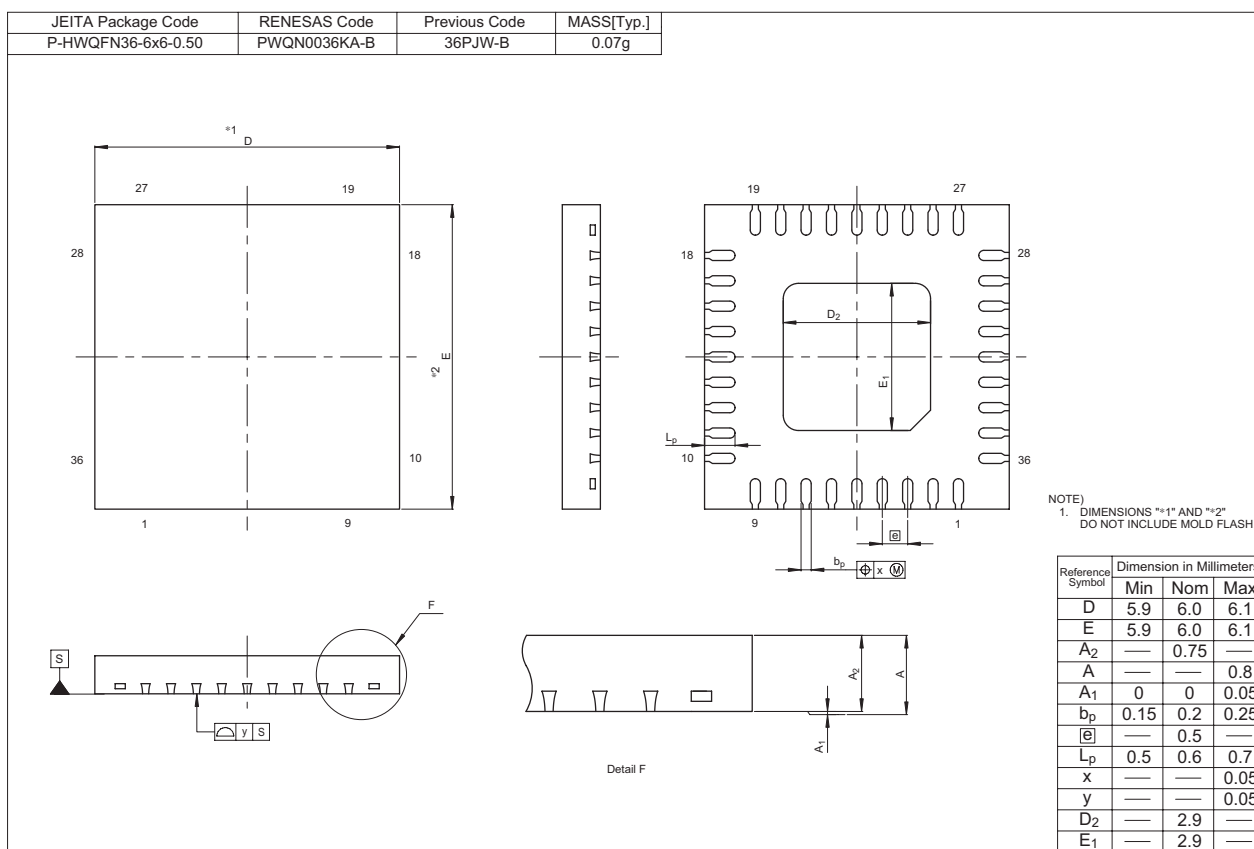
Notes:

- When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency $\times$ 3) or the minimum value of standard, whichever is greater.
- When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency $\times$ 3) or the minimum value of standard, whichever is greater.

**Figure 5.19 Input Timing Diagram for External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{Kli}$ when Vcc = 2.2 V**

Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Electronics website.



REVISION HISTORY	R8C/3JC Group User's Manual: Hardware
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Rev.	Date	Description	
		Page	Summary
0.01	Oct. 30, 2009	—	First Edition issued
1.00	May 25, 2010	—	"Preliminary" and "Under development" deleted
		3	Table 1.2 Operating Ambient Temperature: D version deleted, Note 1 deleted
		4	Table 1.3 D version deleted, (D) deleted
			Figure 1.1 D deleted
		14	Figure 3.1 D version deleted
		27 to 53	"5. Electrical Characteristics" added
		54	Package Dimensions changed

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

- The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.