Infineon Technologies - MB91F463NCPMC-GSE1 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	FR60 RISC
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, WDT
Number of I/O	48
Program Memory Size	288KB (288K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	14K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f463ncpmc-gse1

Part Number / Parameter	CY91V460A	CY91F463NA CY91F463NC
16-bit PFM	1 channel	No
Sound Generator	1 channel	No
8/16-bit up/down counter	4 channels (8-bit) / 2 channels (16-bit)	2 channels (8-bit) /1 channel (16-bit)
C_CAN	6 channels (128 message buffers)	2 channels (32 message buffers)
LIN-USART	4 channels + 4 channels (FIFO) + 8 channels	4 channels
I^2C (400 kbps)	4 channels	2 channels
FR external bus	Yes (32-bit address, 32-bit data)	No
External interrupt	16 channels	10 channels
NMI interrupts	Yes	No
Stepping motor controller (SMC)	6 channels	No
LCD controller (40 4)	1 channel	No
10-bit A/D converter	32 channels	8 channels
Alarm comparator	2 channels	No
Clock supervisor	Yes	No
Main clock oscillator	4 MHz	
Sub clock oscillator	32 kHz	-
CR oscillator	100 kHz	100 kHz / 2 MHz
PLL	× 20	
DSU4	Yes	No
EDSU	Yes (32 BP) [1]	Yes (8 BP)[1]
Power supply voltage	3 V / 5 V	
Regulator	Yes	
Power consumption	n.a.	< 700 mW
Temperature range (T_A)	0 °C to +70°C	− 40 °C to + 105°C
Package	BGA-660	LQFP-64

1. MPU channels use EDSU breakpoint registers (shared operation between MPU and EDSU).

5. Precautions for Handling The Devices

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

5.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

■ Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ Recommended Operating Conditions

The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges. Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their Cypress representatives beforehand.

■ Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

1. Preventing Over-Voltage and Over-Current Conditions
Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such over voltage or over-current conditions at the design stage.
2. Protection of Output Pins
Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device. Therefore, avoid this type of connection.
3. Handling of Unused Input Pins
Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

■ Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

Note:

The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:
(a) Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
(b) Be sure that abnormal current flows do not occur during the power-on sequence.

■ Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

■ Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

5.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.
For reliable performance, do the following:

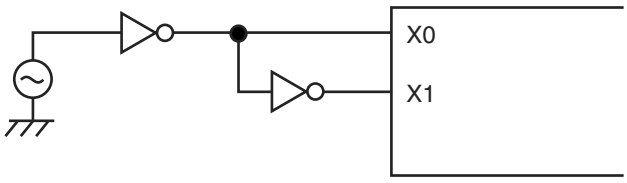
1. Humidity
   Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.
2. Discharge of Static Electricity
   When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.
3. Corrosive Gases, Dust, or Oil
   Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.
4. Radiation, Including Cosmic Radiation
   Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.
5. Smoke, Flame
   Note: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with Cypress sales representatives.

■ Notes on using external clock

When using the external clock, as a general rule you should simultaneously supply X0 and X1 pins. And also, the clock signal to X0 should be supplied a clock signal with the reverse phase to X1 pins. However, in this case the stop mode (oscillation stop mode) must not be used.

Example of using external clock (normal)



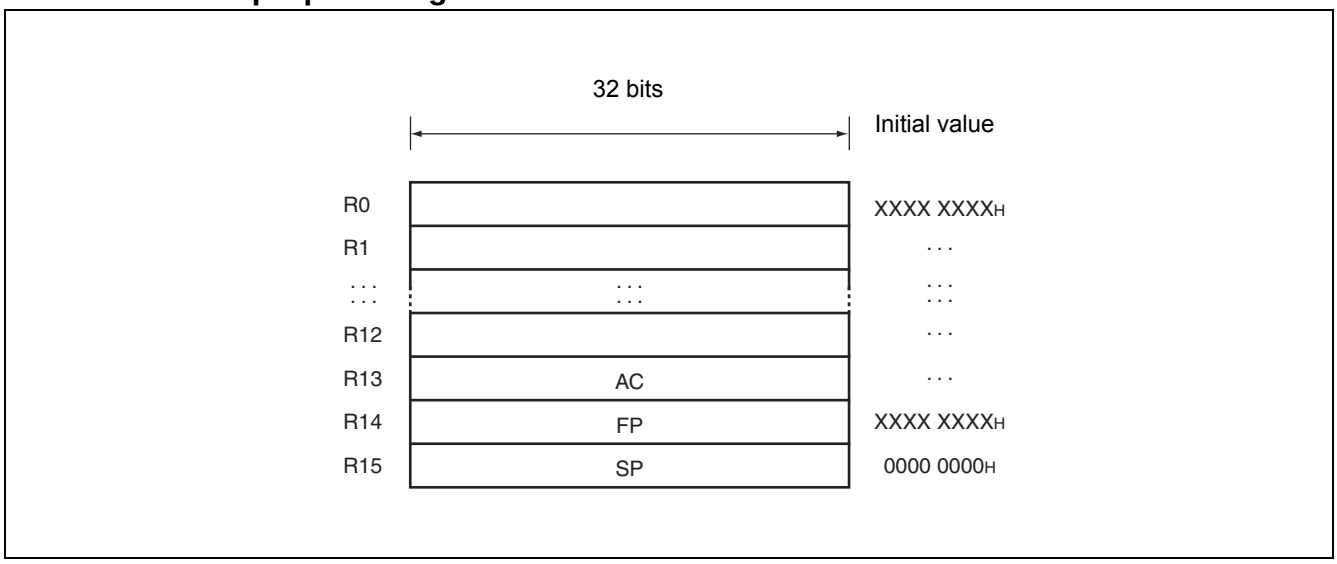
Note: Stop mode (oscillation stop mode) cannot be used.

■ Notes on operating in PLL clock mode

If the oscillator is disconnected or the clock input stops when the PLL clock is selected, the microcontroller may continue to operate at the free-running frequency of the self-oscillating circuit of the PLL. However, this self-running operation cannot be guaranteed.

9.4 Registers

9.4.1 General-purpose Register



Registers R0 to R15 are general-purpose registers. These registers can be used as accumulators for computation operations and as pointers for memory access.

Enhanced commands are provided for some of the 16 registers to enable their use for particular applications.

R13 : Virtual accumulator

R14 : Frame pointer

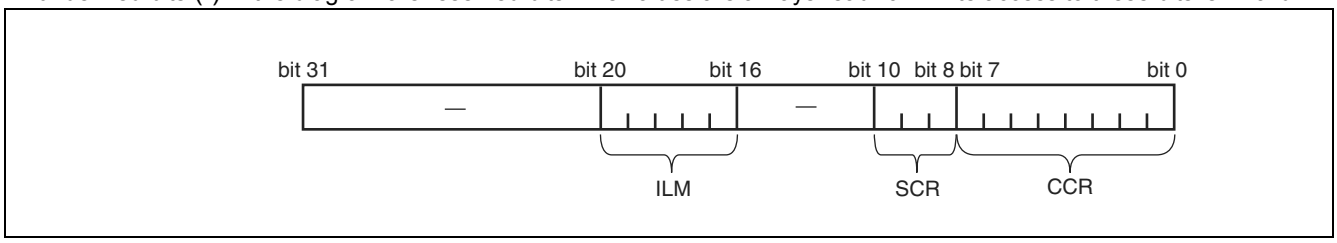
R15 : Stack pointer

Initial values at reset are undefined for R0 to R14. The value for R15 is 00000000_H (SSP value).

9.4.2 PS (Program Status)

This register holds the program status, and is divided into three parts, ILM, SCR, and CCR.

All undefined bits (-) in the diagram are reserved bits. The values are always read "0". Write access to these bits is invalid.



10. Mode Setting

In the FR family, the mode pins (MD2, MD1, MD0) and the mode register (MODR) are used to set the operating mode.

10.1 Mode Pins

The three pins MD2, MD1, MD0 are used to specify the mode vector fetch.

Settings other than shown in the table are prohibited.

Mode Pins[1]			Mode Name	Reset Vector Access Area	Remarks
MD2	MD1	MD0			
0	0	0	Internal ROM mode vector	Internal	
0	0	1	External ROM mode vector	External	Not allowed

1. Always use MD3 with “0”.

10.2 Mode Register (MODR)

The data written to the mode register using mode vector fetch is called mode data.

After the mode register (MODR) is set, the device operates according to the operation mode set in this register.

The mode register is set by all reset sources. User programs cannot write data to the mode register.

Rewriting is allowed in the emulator mode. In this case, use an 8-bit length data transfer instruction.

Data cannot be written by the transfer instruction of the 16/32-bit length.

Be sure to set these bits to “00000111_B”.

Operation is not guaranteed when any value other than “00000111_B” is set.

Note: The mode data needs to be allocated in $000FFFF8_H$ as byte data. The mode data (00000111_B) must be allocated in bit 31 to bit 24, as the FR family uses the big endian architecture.

11. Recommended Setting

11.1 Setting of PLL and Clock Gear

Table 1. Recommended Setting of PLL Division and Clock Gear

Clock Input [MHz]	PLL Multiplied Setting		Clock Gear Setting		PLL (vco) Output (X) [MHz]	Base Clock [MHz]
	DIVM	DIVN	DIVG	MULG		
4	2	20	16	20	160	80
4	2	19	16	20	152	76
4	2	18	16	20	144	72
4	2	17	16	16	136	68
4	2	16	16	16	128	64
4	2	15	16	16	120	60
4	2	14	16	16	112	56
4	2	13	16	12	104	52
4	2	12	16	12	96	48
4	2	11	16	12	88	44
4	4	10	16	24	160	40
4	4	9	16	24	144	36
4	4	8	16	24	128	32
4	4	7	16	24	112	28
4	6	6	16	24	144	24
4	8	5	16	28	160	20
4	10	4	16	32	160	16
4	12	3	16	32	144	12

11.2 Setting of Flash Memory Controller

11.2.1 Setting of Flash Access Timing

For executing programs with a Flash memory, follow the settings below according to the frequency of CPU clock (CLKB). This setting is the most suitable for a high-speed access to the Flash memory.

Table 2. Flash Memory Read Operating

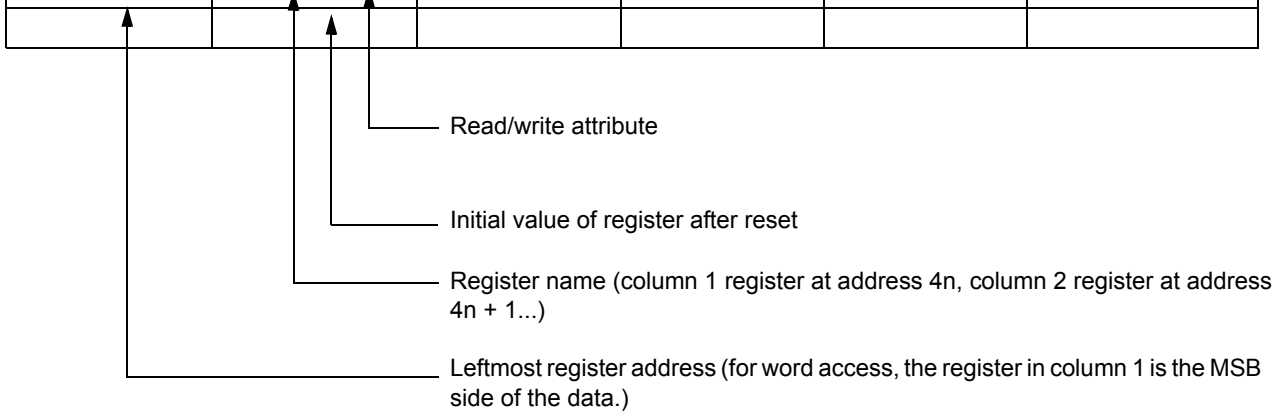
CPU Clock (CLKB)	ATD	ALEH	EQ	WEXH	WTC
To 24 MHz	0	0	0	0	1
To 48 MHz	0	0	1	0	2
To 80 MHz	1	1	3	0	4

Table 3. Flash Memory Write Operating

CPU Clock (CLKB)	ATD	ALEH	EQ	WEXH	WTC
To 32 MHz	1	0	1	0	4
To 48 MHz	1	0	3	0	5
To 64 MHz	1	1	3	0	6
To 80 MHz	1	1	3	0	7

13. I/O Map

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000000_H	PDR0 [R/W] XXXXXXXX	PDR1 [R/W] XXXXXXXX	PDR2 [R/W] XXXXXXXX	PDR3 [R/W] XXXXXXXX	T-unit port data register



Note: Initial values of register bits are represented as follows:
" 1 ": Initial value " 1 "
" 0 ": Initial value " 0 "
" X ": Initial value " undefined "
" - ": No physical register at this location
Access is prohibited to areas where the data access attributes are undefined.

Address	Register				Block
	+0	+1	+2	+3	
000060_H to $00007C_H$	Reserved				Reserved
000080_H	BGR100 [R/W] 00000000	BGR000 [R/W] 00000000	BGR101 [R/W] 00000000	BGR001 [R/W] 00000000	Baud rate Generator LIN-USART0 to 3
000084_H	BGR102 [R/W] 00000000	BGR002 [R/W] 00000000	BGR103 [R/W] 00000000	BGR003 [R/W] 00000000	
000088_H, $00008C_H$	Reserved				
000090_H to $0000FC_H$	Reserved				Reserved
000100_H	GCN10 [R/W] 00110010 00010000		Reserved	GCN20 [R/W] - - - - 0000	PPG Control 0 to 3
000104_H	GCN11 [R/W] 00110010 00010000		Reserved	GCN21 [R/W] - - - - 0000	PPG Control 4 to 7
000108_H	Reserved				Reserved
000110_H	PTMR00 [R] 11111111 11111111		PCSR00 [W] XXXXXXXX XXXXXXXX		PPG 0
000114_H	PDUT00 [W] XXXXXXXX XXXXXXXX		PCNH00 [R/W] 0000000 -	PCNL00 [R/W] 000000 - 0	
000118_H	PTMR01 [R] 11111111 11111111		PCSR01 [W] XXXXXXXX XXXXXXXX		PPG 1
$00011C_H$	PDUT01 [W] XXXXXXXX XXXXXXXX		PCNH01 [R/W] 0000000 -	PCNL01 [R/W] 000000 - 0	
000120_H	PTMR02 [R] 11111111 11111111		PCSR02 [W] XXXXXXXX XXXXXXXX		PPG 2
000124_H	PDUT02 [W] XXXXXXXX XXXXXXXX		PCNH02 [R/W] 0000000 -	PCNL02 [R/W] 000000 - 0	
000128_H	PTMR03 [R] 11111111 11111111		PCSR03 [W] XXXXXXXX XXXXXXXX		PPG 3
$00012C_H$	PDUT03 [W] XXXXXXXX XXXXXXXX		PCNH03 [R/W] 0000000 -	PCNL03 [R/W] 000000 - 0	
000130_H	PTMR04 [R] 11111111 11111111		PCSR04 [W] XXXXXXXX XXXXXXXX		PPG 4
000134_H	PDUT04 [W] XXXXXXXX XXXXXXXX		PCNH04 [R/W] 0000000 -	PCNL04 [R/W] 000000 - 0	
000138_H	PTMR05 [R] 11111111 11111111		PCSR05 [W] XXXXXXXX XXXXXXXX		PPG 5
$00013C_H$	PDUT05 [W] XXXXXXXX XXXXXXXX		PCNH05 [R/W] 0000000 -	PCNL05 [R/W] 000000 - 0	
000140_H	PTMR06 [R] 11111111 11111111		PCSR06 [W] XXXXXXXX XXXXXXXX		PPG 6
000144_H	PDUT06 [W] XXXXXXXX XXXXXXXX		PCNH06 [R/W] 0000000 -	PCNL06 [R/W] 000000 - 0	
000148_H	PTMR07 [R] 11111111 11111111		PCSR07 [W] XXXXXXXX XXXXXXXX		PPG 7
$00014C_H$	PDUT07 [W] XXXXXXXX XXXXXXXX		PCNH07 [R/W] 0000000 -	PCNL07 [R/W] 000000 - 0	

Address	Register				Block
	+0	+1	+2	+3	
000150_H to $00017C_H$	Reserved				Reserved
000180_H	Reserved	ICS01 [R/W] 00000000	Reserved	ICS23 [R/W] 00000000	Input Capture 0 to 3
000184_H	IPCP0 [R] XXXXXXXX XXXXXXXX		IPCP1 [R] XXXXXXXX XXXXXXXX		
000188_H	IPCP2 [R] XXXXXXXX XXXXXXXX		IPCP3 [R] XXXXXXXX XXXXXXXX		
$00018C_H$	OCS01 [R/W] - - - 0 - - 00 0000 - - 00		OCS23 [R/W] - - - 0 - - 00 0000 - - 00		Output Compare 0 to 3
000190_H	OCCP0 [R/W] XXXXXXXX XXXXXXXX		OCCP1 [R/W] XXXXXXXX XXXXXXXX		
000194_H	OCCP2 [R/W] XXXXXXXX XXXXXXXX		OCCP3 [R/W] XXXXXXXX XXXXXXXX		
000198_H, $00019C_H$	Reserved				Reserved
$0001A0_H$	Reserved			ADERL [R/W] 00000000	A/D Converter
$0001A4_H$	ADCS1 [R/W] 00000000	ADCS0 [R/W] 00000000	ADCR1 [R] 000000XX	ADCR0 [R] XXXXXXXX	
$0001A8_H$	ADCT1 [R/W] 00010000	ADCT0 [R/W] 00101100	ADSCH [R/W] - - - 00000	ADECH [R/W] - - - 00000	
$0001AC_H$	Reserved				Reserved
$0001B0_H$	TMRLR0 [W] XXXXXXXX XXXXXXXX		TMR0 [R] XXXXXXXX XXXXXXXX		Reload Timer 0 (PPG0, PPG1)
$0001B4_H$	Reserved		TMCSRH0 [R/W] - - - 00000	TMCSRL0 [R/W] 0 - 000000	
$0001B8_H$	TMRLR1 [W] XXXXXXXX XXXXXXXX		TMR1 [R] XXXXXXXX XXXXXXXX		Reload Timer 1 (PPG2, PPG3)
$0001BC_H$	Reserved		TMCSRH1 [R/W] - - - 00000	TMCSRL1 [R/W] 0 - 000000	
$0001C0_H$	TMRLR2 [W] XXXXXXXX XXXXXXXX		TMR2 [R] XXXXXXXX XXXXXXXX		Reload Timer 2 (PPG4, PPG5)
$0001C4_H$	Reserved		TMCSRH2 [R/W] - - - 00000	TMCSRL2 [R/W] 0 - 000000	
$0001C8_H$	TMRLR3 [W] XXXXXXXX XXXXXXXX		TMR3 [R] XXXXXXXX XXXXXXXX		Reload Timer 3 (PPG6, PPG7)
$0001CC_H$	Reserved		TMCSRH3 [R/W] - - - 00000	TMCSRL3 [R/W] 0 - 000000	
$0001D0_H$ to $0001E7_H$	Reserved				Reserved

Address	Register				Block
	+0	+1	+2	+3	
$0001E8_H$	TMRLR7 [W] XXXXXXXX XXXXXXXX		TMR7 [R] XXXXXXXX XXXXXXXX		Reload Timer 7 (A/D converter)
$0001EC_H$	Reserved		TMCSRH7 [R/W] - - - 00000	TMCSRL7 [R/W] 0 - 000000	
$0001F0_H$	TCDT0 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS0 [R/W] 00000000	Free-run Timer 0 (ICU0, ICU1)
$0001F4_H$	TCDT1 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS1 [R/W] 00000000	Free-run Timer 1 (ICU2, ICU3)
$0001F8_H$	TCDT2 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS2 [R/W] 00000000	Free-run Timer 2 (OCU0, OCU1)
$0001FC_H$	TCDT3 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS3 [R/W] 00000000	Free-run Timer 3 (OCU2, OCU3)
000200_H	DMACA0 [R/W] * 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC
000204_H	DMACB0 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000208_H	DMACA1 [R/W] * 00000000 0000XXXX XXXXXXXX XXXXXXXX				
$00020C_H$	DMACB1 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000210_H	DMACA2 [R/W] * 00000000 0000XXXX XXXXXXXX XXXXXXXX				
000214_H	DMACB2 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000218_H	DMACA3 [R/W] * 00000000 0000XXXX XXXXXXXX XXXXXXXX				
$00021C_H$	DMACB3 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000220_H	DMACA4 [R/W] * 00000000 0000XXXX XXXXXXXX XXXXXXXX				
000224_H	DMACB4 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000228_H to $00023C_H$	Reserved				
000240_H	DMACR [R/W] 0- - - 0000	Reserved			
000244_H to $0002FC_H$	Reserved				Reserved
000300_H	UDRC1 [W] 00000000	UDRC0 [W] 00000000	UDCR1 [R] 00000000	UDCR0 [R] 00000000	Up/Down Counter 0, 1
000304_H	UDCCH0 [R/W] 00000000	UDCCL0 [R/W] 00001000	Reserved	UDCS0 [R/W] 00000000	
000308_H	UDCCH1 [R/W] 00000000	UDCCL1 [R/W] 00001000	Reserved	UDCS1 [R/W] 00000000	

Address	Register				Block
	+0	+1	+2	+3	
$000D40_H$ to $000D48_H$	Reserved				R-bus Port Direction Register
$000D4C_H$	Reserved		DDR14 [R/W] - - - - 0000	DDR15 [R/W] - - - - 0000	
$000D50_H$	Reserved	DDR17 [R/W] 00000000	Reserved		
$000D54_H$	DDR20 [R/W] -000- 000	DDR21 [R/W] -000- 000	DDR22 [R/W] - - - - 0000	Reserved	
$000D58_H$	DDR24 [R/W] 00000000	Reserved			
$000D5C_H$	Reserved	DDR29 [R/W] 00000000	Reserved		
$000D60_H$	Reserved				
$000D64_H$ to $000D7C_H$	Reserved				Reserved
$000D80_H$ to $000D88_H$	Reserved				R-bus Port Function Register
$000D8C_H$	Reserved		PFR14 [R/W] - - - - 0000	PFR15 [R/W] - - - - 0000	
$000D90_H$	Reserved	PFR17 [R/W] 00000000	Reserved		
$000D94_H$	PFR20 [R/W] -000- 000	PFR21 [R/W] -000- 000	PFR22 [R/W] - - - - 0000	Reserved	
$000D98_H$	PFR24 [R/W] 00000000	Reserved			
$000D9C_H$	Reserved	PFR29 [R/W] 00000000	Reserved		
$000DA0_H$	Reserved				
$000DA4_H$ to $000DBC_H$	Reserved				Reserved
$000DC0_H$ to $000DC8_H$	Reserved				R-bus Extension Port Function Register
$000DCC_H$	Reserved		EPFR14 [R/W] - - - - 0000	EPFR15 [R/W] - - - - 0000	
$000DD0_H$	Reserved				R-bus Extension Port Function Register
$000DD4_H$	EPFR20 [R/W] - 000- 000	EPFR21 [R/W] - 0- - - 0- -	Reserved		
$000DD8_H$	Reserved				
$000DDC_H$	Reserved				
$000DE0_H$	Reserved				
$000DE4_H$ to $000DFC_H$	Reserved				Reserved

Address	Register				Block
	+0	+1	+2	+3	
001000_H	DMASA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMAC
001004_H	DMADA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001008_H	DMASA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00100C_H$	DMADA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001010_H	DMASA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001014_H	DMADA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001018_H	DMASA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00101C_H$	DMADA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001020_H	DMASA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001024_H	DMADA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001028_H to $006FFC_H$	Reserved				Reserved
007000_H	FMCS [R/W] 01101000	FMCR [R/W] - - - -0000	FCHCR [R/W] - - - - - - 00 10000011		Flash Memory/ I-Cache Control Register
007004_H	FMWT [R/W] 11111111 01011101		FMWT2 [R/W] - 101 - - - -	FMPS [R/W] - - - - - 000	
007008_H	FMAC [R] - - - - - - - - - - - - 00000 00000000 00000000				
$00700C_H$	FCHA0 [R/W] - - - - - - - - - 0000000 00000000 00000000				I-Cache Non-cacheable area setting Register
007010_H	FCHA1 [R/W] - - - - - - - - - 0000000 00000000 00000000				
007014_H to $00AFFC_H$	Reserved				Reserved
$00B000_H$ to $00BFFC_H$	BI-ROM size is 4 Kbytes : $00B000_H$ to $00BFFF_H$				BI-ROM 4 Kbytes
$00C000_H$ to $00C3FC_H$	Reserved				Reserved

14. Interrupt Source Table

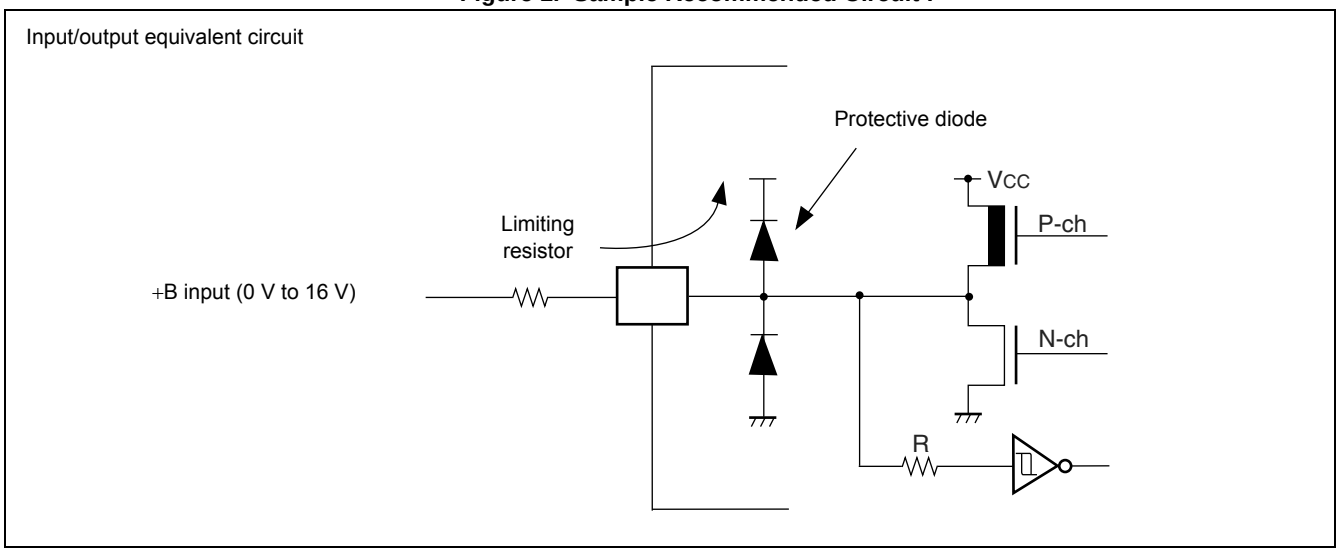
Interrupt source	Interrupt number		Interrupt level		Interrupt vector		Resource number[1]
	Decimal	Hexa-decimal	Setting register	Register address	Offset	Default vector address	
Reset	0	00	-	-	$3FC_H$	$000FFFFC_H$	-
Mode vector	1	01	-	-	$3F8_H$	$000FFFF8_H$	-
System reserved	2	02	-	-	$3F4_H$	$000FFFF4_H$	-
System reserved	3	03	-	-	$3F0_H$	$000FFFF0_H$	-
System reserved	4	04	-	-	$3EC_H$	$000FFFEC_H$	-
CPU supervisor mode (INT #5 instruction) [2]	5	05	-	-	$3E8_H$	$000FFFE8_H$	-
Memory protection exception [2]	6	06	-	-	$3E4_H$	$000FFFE4_H$	-
System reserved	7	07	-	-	$3E0_H$	$000FFFE0_H$	-
System reserved	8	08	-	-	$3DC_H$	$000FFFDC_H$	-
System reserved	9	09	-	-	$3D8_H$	$000FFFD8_H$	-
System reserved	10	0A	-	-	$3D4_H$	$000FFFD4_H$	-
System reserved	11	0B	-	-	$3D0_H$	$000FFFD0_H$	-
System reserved	12	0C	-	-	$3CC_H$	$000FFFCC_H$	-
System reserved	13	0D	-	-	$3C8_H$	$000FFFC8_H$	-
Undefined instruction exception	14	0E	-	-	$3C4_H$	$000FFFC4_H$	-
NMI request	15	0F	F_H fixed		$3C0_H$	$000FFFC0_H$	-
External interrupt 0	16	10	ICR00	440_H	$3BC_H$	$000FFFBC_H$	0, 16
External interrupt 1	17	11			$3B8_H$	$000FFFB8_H$	1, 17
External interrupt 2	18	12	ICR01	441_H	$3B4_H$	$000FFFB4_H$	2, 18
External interrupt 3	19	13			$3B0_H$	$000FFFB0_H$	3, 19
External interrupt 4	20	14	ICR02	442_H	$3AC_H$	$000FFFAC_H$	20
External interrupt 5	21	15			$3A8_H$	$000FFFA8_H$	21
External interrupt 6	22	16	ICR03	443_H	$3A4_H$	$000FFFA4_H$	22
External interrupt 7	23	17			$3A0_H$	$000FFFA0_H$	23
System reserved	24	18	ICR04	444_H	$39C_H$	$000FFF9C_H$	-
System reserved	25	19			398_H	$000FFF98_H$	-
System reserved	26	1A	ICR05	445_H	394_H	$000FFF94_H$	-
System reserved	27	1B			390_H	$000FFF90_H$	-
External interrupt 12	28	1C	ICR06	446_H	$38C_H$	$000FFF8C_H$	-
External interrupt 13	29	1D			388_H	$000FFF88_H$	-
System reserved	30	1E	ICR07	447_H	384_H	$000FFF84_H$	-
System reserved	31	1F			380_H	$000FFF80_H$	-
Reload timer 0	32	20	ICR08	448_H	$37C_H$	$000FFF7C_H$	4, 32
Reload timer 1	33	21			378_H	$000FFF78_H$	5, 33
Reload timer 2	34	22	ICR09	449_H	374_H	$000FFF74_H$	34
Reload timer 3	35	23			370_H	$000FFF70_H$	35
System reserved	36	24	ICR10	$44A_H$	$36C_H$	$000FFF6C_H$	36
System reserved	37	25			368_H	$000FFF68_H$	37

4.

- Corresponding pins: Pin name P29_0 to P29_7, P24_0 to P24_7, P22_0 to P22_3, P20_0 to P20_2, P20_4 to P20_6, P15_0 to P15_3, P17_0 to P17_7, P21_0 to P21_2, P21_4 to P21_6, P14_0 to P14_3
- Use within recommended operating conditions.
- Use at DC voltage (current).
- The + B signal is an input signal exceeding V_{CC} voltage. The + B signal should always be applied by connecting a limiting resistor between the + B signal and the microcontroller.
- The value of the limiting resistor should be set so that the current input to the microcontroller pin does not exceed rated values at any time regardless of instantaneously or constantly when the + B signal is input.
- Note that when the microcontroller drive current is low, such as in the low power consumption modes, the + B input potential can increase the potential at the VCC pin via a protective diode, possibly affecting other devices.
- Note that if the + B signal is input when the microcontroller is off (not fixed at 0 V), since the power is supplied through the pin, the microcontroller may operate incompletely.
- Note that if the + B signal is input at power-on, since the power is supplied through the pin, the power supply voltage may become the voltage at which a power-on reset does not work.
- Do not leave + B input pins open.
  ″Note that analog input/output pins can input the + B signal only at using as a port.

5. Maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.
6. Average output current is defined as the value of the average current flowing through any one of the corresponding pins for a 100 ms period.
7. Total average output current is defined as the value of the average current flowing through all of the corresponding pins for a 100 ms period.

Figure 1. Sample Recommended Circuit :



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

15.3 DC Characteristics

(V_{CC} = 3.0 V to 3.6 V/ 4.5 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, T_A = –40°C to + 105°C/–40°C to + 85°C)

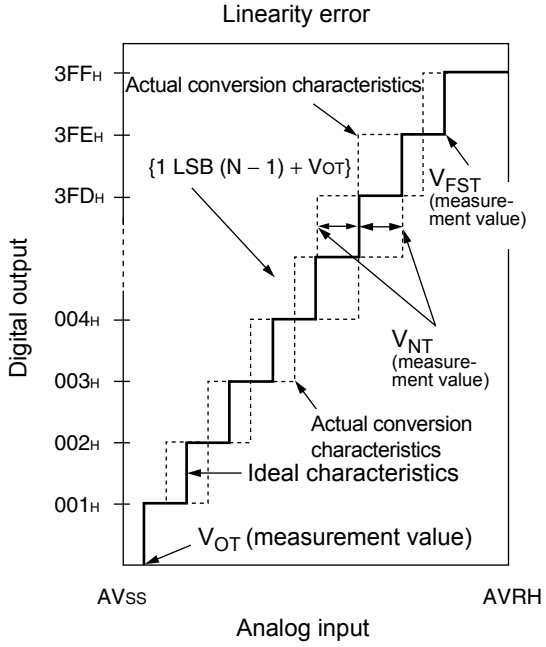
Parameter	Symbol	Pin Name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IHS}	Port pin	When CMOS hysteresis input type1 are selected	0.7 × V_{CC}	-	V_{CC} + 0.3	V	
	V_{IHC}	Port pin	When CMOS hysteresis input type2 are selected	0.8 × V_{CC}	-	V_{CC} + 0.3	V	
	V_{IHA}	Port pin	When Automotive inputs are selected	0.8 × V_{CC}	-	V_{CC} + 0.3	V	
	V_{IHT}	Port pin	When TTL input levels are selected	2.0	-	V_{CC} + 0.3	V	
	V_{IH1}	MD2 to MD0	CMOS level input	0.7 × V_{CC}	-	V_{CC} + 0.3	V	
	V_{IH2}	MD3, INITX	CMOS hysteresis input	0.7 × V_{CC}	-	V_{CC} + 0.3	V	
"L" level input voltage	V_{ILS}	Port pin	When CMOS hysteresis input type1 are selected	V_{SS} − 0.3	-	0.3 × V_{CC}	V	
	V_{ILC}	Port pin	When CMOS hysteresis input type2 are selected	V_{SS} − 0.3	-	0.2 × V_{CC}	V	
	V_{ILA}	Port pin	When Automotive inputs are selected	V_{SS} − 0.3	-	0.5 × V_{CC}	V	
	V_{ILT}	Port pin	When TTL input levels are selected	V_{SS} − 0.3	-	0.8	V	
	V_{IL1}	MD2 to MD0	CMOS level input	V_{SS} − 0.3	-	0.3 × V_{CC}	V	
	V_{IL2}	MD3, INITX	CMOS hysteresis input	V_{SS} − 0.3	-	0.3 × V_{CC}	V	
"H" level output voltage	V_{OH1}	Port pin	V_{CC} = 5.0 V, I_{OH} = –2.0 mA/ V_{CC} = 3.3 V, I_{OH} = –1.0 mA	V_{CC} − 0.5	-	-	V	[1]
	V_{OH2}	I^2C common port pin	V_{CC} = 5.0 V, I_{OH} = –3.0 mA/ V_{CC} = 3.3 V, I_{OH} = –3.0 mA	V_{CC} − 0.5	-	-	V	
	V_{OH3}	Port pin	V_{CC} = 5.0 V, I_{OH} = –5.0 mA/ V_{CC} = 3.3 V, I_{OH} = –3.0 mA	V_{CC} − 0.5	-	-	V	[1]

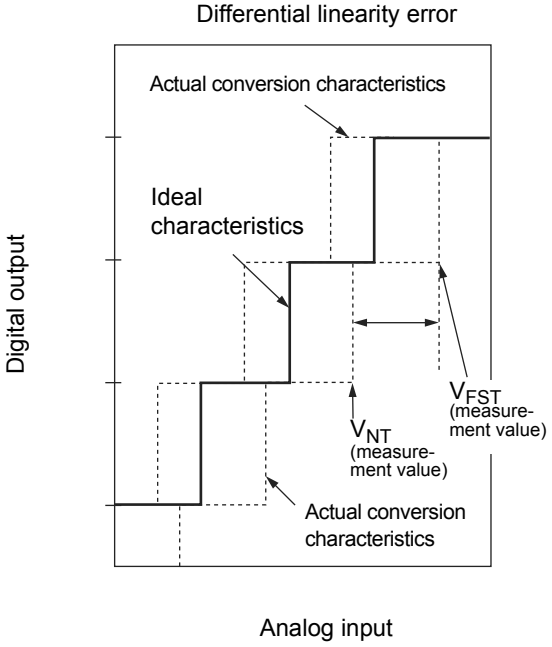
15.5 Electrical Characteristics for A/D Converter

(V_{CC} = 3.0 V to 3.6 V/ 4.5 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, T_A = –40 °C to + 105 °C/–40 °C to + 85 °C)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	–	–	–	–	10	bit	
Total error[1]	–	–	–	–	± 3	LSB	
Linearity error[1]	–	–	–	–	± 2.5	LSB	
Differential linearity error[1]	–	–	–	–	± 1.9	LSB	
Zero transition voltage[1]	V_{OT}	AN0 to AN7	AV_{SS}–1.5 LSB	AV_{SS}–0.5 LSB	AV_{SS}–2.5 LSB	V	
Full scale transition voltage[1]	V_{FST}	AN0 to AN7	AVRH–3.5 LSB	AVRH–1.5 LSB	AVRH–0.5 LSB	V	
Conversion time	–	–	1 [2]	–	–	µs	Using at 5 V
			3 [2]	–	–	µs	Using at 3.3 V
Analog port input current	I_{AIN}	AN0 to AN7	–	–	10	µA	
Analog input voltage	V_{AIN}	AN0 to AN7	AV_{SS}	–	AVRH	V	
Reference voltage	–	AVRH	AV_{SS}	–	AV_{CC}	V	
Analog power supply current (analog + digital)	I_A	AVCC	–	2.4	4.7	mA	Including reference supply
Reference voltage supply current	I_R	AVRH	–	0.65	1.0	mA	
Analog input equivalent capacitance	Cin	AN0 to AN7	–	–	8.5	pF	
Analog input equivalent resistance	Rin	AN0 to AN7	–	–	2.6	kΩ	AVcc ? 4.5 V
			–	–	12.1	kΩ	AVcc ? 3.0 V
Output impedance of analog signal source	Rext	–	–	–	4.2	kΩ	

1. Measured in the CPU sleep state
2. Set no shorter than this time period in the peripheral clock and conversion setting register





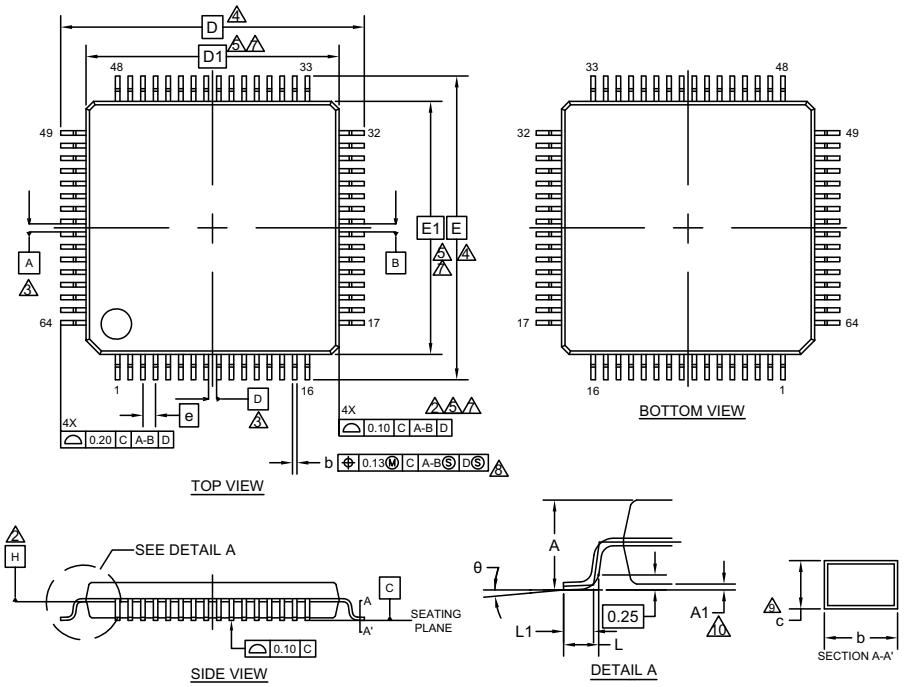
$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1\text{LSB} \quad (N - 1) + V_{OT}\}}{1\text{LSB}} [\text{LSB}]$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\text{LSB}} [\text{LSB}]$$

$$1\text{LSB} = \frac{V_{FST} - V_{OT}}{1022} [\text{V}]$$

N: A/D converter digital output value
V_{OT} : A voltage at which digital output transits from 000_H to 001_H.
V_{FST} : A voltage at which digital output transits from $3FE_H$ to $3FF_H$.

17. Package Dimension



SYMBOL	DIMENSION		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.00	—	0.20
b	0.27	0.32	0.37
c	0.09	—	0.20
D	14.00 BSC		
D1	12.00 BSC		
e	0.65 BSC		
E	14.00 BSC		
E1	12.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
θ	0°	—	8°

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-13881 **

PACKAGE OUTLINE, 64 LEAD LQFP
12.0X12.0X1.7 MM LQG064 REV**

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