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Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

What Are Embedded - Microcontrollers - Application Specific?

Application specific microcontrollers are engineered to

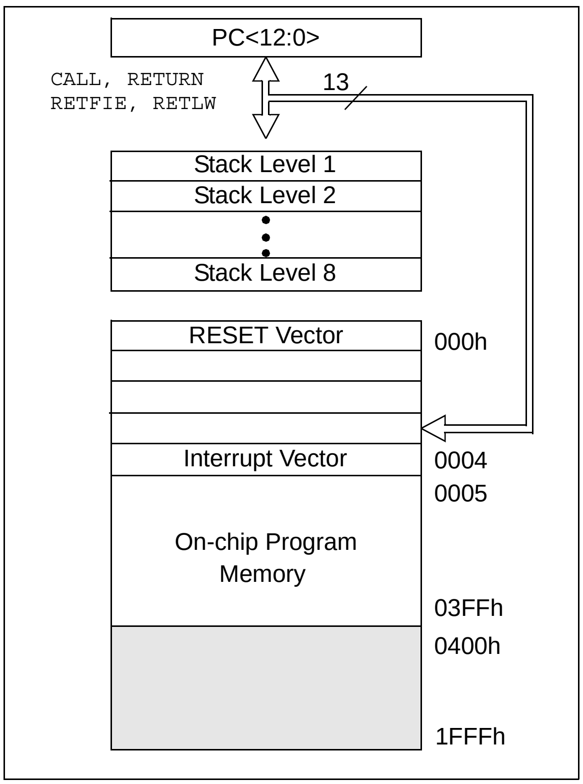
Details	
Product Status	Obsolete
Applications	RKE, Security Systems
Core Processor	PIC
Program Memory Type	FLASH (1.75kB)
Controller Series	rfPIC™
RAM Size	64 x 8
Interface	-
Number of I/O	6
Voltage - Supply	2V ~ 5.5V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/rfpic12f675f-i-ss

2.0 MEMORY ORGANIZATION

2.1 Program Memory Organization

The rfPIC12F675 devices have a 13-bit program counter capable of addressing an 8K x 14 program memory space. Only the first 1K x 14 (0000h - 03FFh) for the rfPIC12F675 devices is physically implemented. Accessing a location above these boundaries will cause a wrap around within the first 1K x 14 space. The RESET vector is at 0000h and the interrupt vector is at 0004h (see Figure 2-1).

FIGURE 2-1: PROGRAM MEMORY MAP AND STACK FOR THE rfPIC12F675



2.2 Data Memory Organization

The data memory (see Figure 2-2) is partitioned into two banks, which contain the General Purpose registers and the Special Function registers. The Special Function registers are located in the first 32 locations of each bank. Register locations 20h-5Fh are General Purpose registers, implemented as static RAM and are mapped across both banks. All other RAM is unimplemented and returns ‘0’ when read. RP0 (STATUS<5>) is the bank select bit.

- RP0 = 0 Bank 0 is selected
- RP0 = 1 Bank 1 is selected

Note:	The IRP and RP1 bits STATUS<7:6> are reserved and should always be maintained as ‘0’s.

2.2.1 GENERAL PURPOSE REGISTER FILE

The register file is organized as 64 x 8 in the rfPIC12F675 devices. Each register is accessed, either directly or indirectly, through the File Select Register FSR (see Section 2.4).

REGISTER 3-2: TRISIO — GPIO TRISTATE REGISTER (ADDRESS: 85h)

U-0	U-0	R/W-x	R/W-x	R-1	R/W-x	R/W-x	R/W-x
—	—	TRISIO5	TRISIO4	TRISIO3	TRISIO2	TRISIO1	TRISIO0
bit 7							bit 0

bit 7-6: **Unimplemented**: Read as '0'

bit 5-0: **TRISIO<5:0>**: General Purpose I/O Tri-State Control bit
1 = GPIO pin configured as an input (tri-stated)
0 = GPIO pin configured as an output.

Note: TRISIO<3> always reads 1.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

REGISTER 3-3: WPU — WEAK PULL-UP REGISTER (ADDRESS: 95h)

U-0	U-0	R/W-1	R/W-1	U-0	R/W-1	R/W-1	R/W-1
—	—	WPU5	WPU4	—	WPU2	WPU1	WPU0
bit 7							bit 0

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **WPU<5:4>:** Weak Pull-up Register bit
1 = Pull-up enabled
0 = Pull-up disabled

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **WPU<2:0>:** Weak Pull-up Register bit
1 = Pull-up enabled
0 = Pull-up disabled

Note 1: Global $\overline{\text{GPPU}}$ must be enabled for individual pull-ups to be enabled.
2: The weak pull-up device is automatically disabled if the pin is in Output mode (TRISIO = 0).

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

REGISTER 5-1: T1CON — TIMER1 CONTROL REGISTER (ADDRESS: 10h)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON
bit 7							bit 0

bit 7 **Unimplemented:** Read as ‘0’

bit 6 **TMR1GE:** Timer1 Gate Enable bit
If TMR1ON = 0:
This bit is ignored
If TMR1ON = 1:
1 = Timer1 is on if $\overline{\text{T1G}}$ pin is low
0 = Timer1 is on

bit 5-4 **T1CKPS1:T1CKPS0:** Timer1 Input Clock Prescale Select bits
11 = 1:8 Prescale Value
10 = 1:4 Prescale Value
01 = 1:2 Prescale Value
00 = 1:1 Prescale Value

bit 3 **T1OSCEN:** LP Oscillator Enable Control bit
If INTOSC without CLKOUT oscillator is active:
1 = LP oscillator is enabled for Timer1 clock
0 = LP oscillator is off
Else:
This bit is ignored

bit 2 **$\overline{\text{T1SYNC}}$:** Timer1 External Clock Input Synchronization Control bit
TMR1CS = 1:
1 = Do not synchronize external clock input
0 = Synchronize external clock input
TMR1CS = 0:
This bit is ignored. Timer1 uses the internal clock.

bit 1 **TMR1CS:** Timer1 Clock Source Select bit
1 = External clock from T1OSO/T1CKI pin (on the rising edge)
0 = Internal clock (FOSC/4)

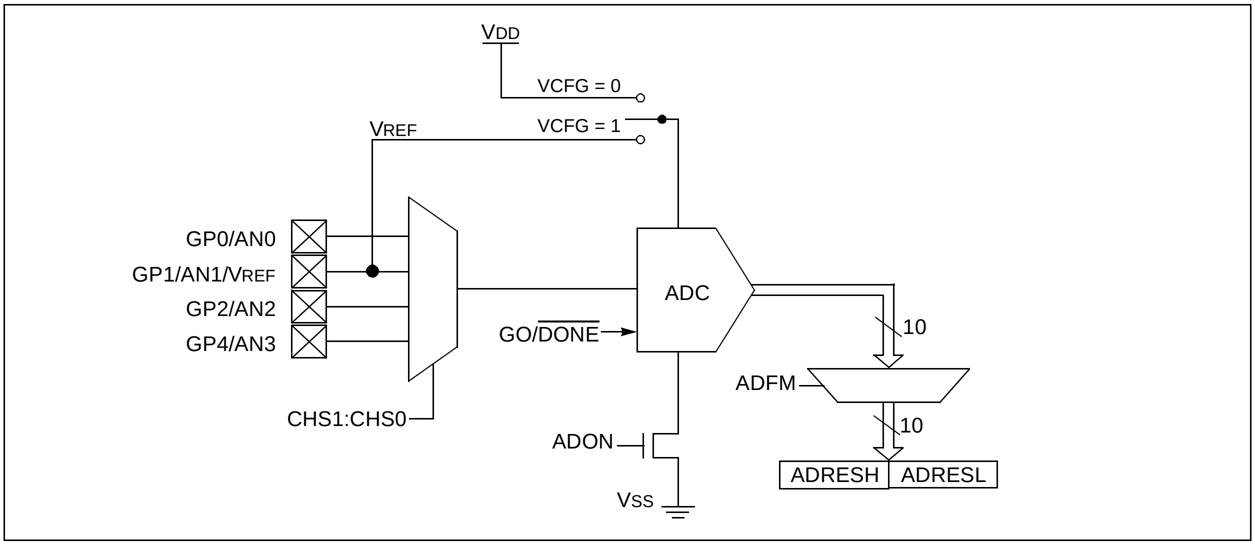
bit 0 **TMR1ON:** Timer1 On bit
1 = Enables Timer1
0 = Stops Timer1

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
- n = Value at POR	’1’ = Bit is set	’0’ = Bit is cleared	x = Bit is unknown

7.0 ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE

The analog-to-digital converter (A/D) allows conversion of an analog input signal to a 10-bit binary representation of that signal. The rfPIC12F675 has four analog inputs, multiplexed into one sample and hold circuit. The output of the sample and hold is connected to the input of the converter. The converter generates a binary result via successive approximation and stores the result in a 10-bit register. The voltage reference used in the conversion is software selectable to either VDD or a voltage applied by the VREF pin. Figure 7-1 shows the block diagram of the A/D.

FIGURE 7-1: A/D BLOCK DIAGRAM



7.1 A/D Configuration and Operation

There are two registers available to control the functionality of the A/D module:

1. ADCON0 (Register 7-1)
2. ANSEL (Register 7-2)

7.1.1 ANALOG PORT PINS

The ANS3:ANS0 bits (ANSEL<3:0>) and the TRISIO bits control the operation of the A/D port pins. Set the corresponding TRISIO bits to set the pin output driver to its high impedance state. Likewise, set the corresponding ANS bit to disable the digital input buffer.

Note:	Analog voltages on any pin that is defined as a digital input may cause the input buffer to conduct excess current.

7.1.2 CHANNEL SELECTION

There are four analog channels, AN0 through AN3. The CHS1:CHS0 bits (ADCON0<3:2>) control which channel is connected to the sample and hold circuit.

7.1.3 VOLTAGE REFERENCE

There are two options for the voltage reference to the A/D converter: either VDD is used, or an analog voltage applied to VREF is used. The VCFG bit (ADCON0<6>) controls the voltage reference selection. If VCFG is set, then the voltage on the VREF pin is the reference; otherwise, VDD is the reference.

7.1.4 CONVERSION CLOCK

The A/D conversion cycle requires 11 TAD. The source of the conversion clock is software selectable via the ADCS bits (ANSEL<6:4>). There are seven possible clock options:

- FOSC/2
- FOSC/4
- FOSC/8
- FOSC/16
- FOSC/32
- FOSC/64
- FRC (dedicated internal RC oscillator)

For correct conversion, the A/D conversion clock (1/TAD) must be selected to ensure a minimum TAD of 1.6 µs. Table 7-1 shows a few TAD calculations for selected frequencies.

9.5 FSK Modulation

In FSK modulation the transmit data is sent by varying the output frequency. This is done by loading the reference crystal with extra capacitance to pull it to a slightly lower frequency which the PLL then tracks. Switching the capacitance in and out with the data signal toggles the transmitter between two frequencies. These two crystal based frequencies are then multiplied by 32 for the RF transmit frequency.

Unlike the ASK transmit frequency the FSK center frequency is not actually transmitted. It is the artificial point half way between the two transmitted frequencies, calculated with this formula.

$$f_c = \frac{f_{max} + f_{min}}{2}$$

The other important parameter in FSK is the frequency deviation of the transmit frequency. This measures how far the frequency will swing from the center frequency. Single ended deviation is calculated with this formula.

$$\Delta f = \frac{f_{max} - f_{min}}{2}$$

An FSK receiver will specify its optimal value of deviation. The single ended deviation must be greater than data rate/4. The minimum deviation is usually limited by the frequency accuracy of the transmitter and receiver components. The maximum deviation is usually limited by the pulling characteristics of the transmitter crystal.

An extra capacitor and the internal switch are added to the ASK design to build an FSK transmitter as shown in Figure 9-3. The C1 capacitor in series with the crystal determines the maximum frequency.

With the DATAFSK pin high the FSKOUT pin is open and the C2 capacitor does not affect the frequency. When the DATAFSK pin goes low, FSKOUT shorts to ground, and the C2 is thrown in parallel with C1. The sum of the two caps pulls the oscillation frequency lower as shown in Figure 9-4.

In FSK mode the DATAASK pin should be tied high to enable the PA. The FSK circuit is shown in Figure 9-6. Use accurate crystals for narrow bandwidth systems and large values for C1 to reduce frequency drift.

FIGURE 9-3: FSK CRYSTAL CIRCUIT

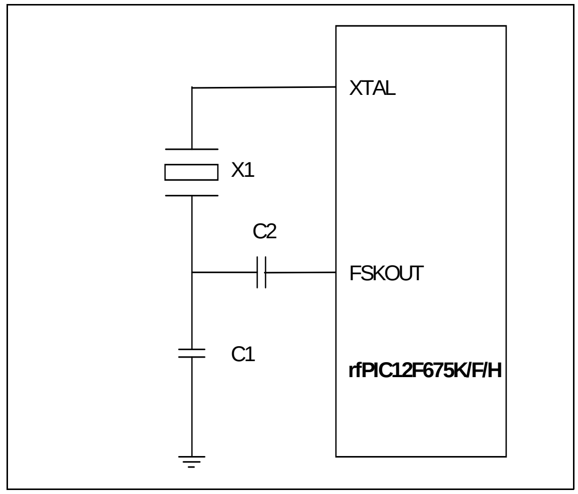


FIGURE 9-4: FREQUENCY PULLING

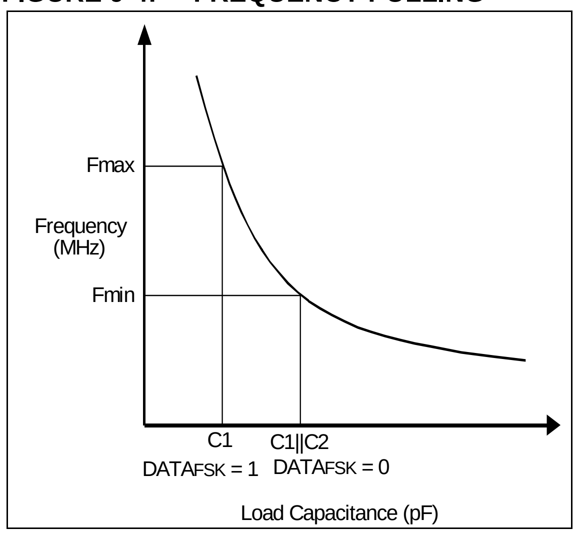


TABLE 9-3: TYPICAL TRANSMIT CENTER FREQUENCY AND DEVIATION (FSK MODE) (1)

	C2 = 1000 pF	C2 = 100 pF	C2 = 47 pF
C1 (pF)	**Freq (MHz) / Dev (kHz)**	**Freq (MHz) / Dev (kHz)**	**Freq (MHz) / Dev (kHz)**
22	433.612 / 34	433.619 / 27	433.625 / 21
33	433.604 / 25	433.610 / 19	433.614 / 14
39	433.598 / 20	433.604 / 14	433.608 / 10
47	433.596 / 17	433.601 / 11.5	433.604 / 8
68	433.593 / 13	433.598 / 9	433.600 / 5.5
100	433.587 / 8	—	—

Note 1: Standard Operating Conditions, T_A = 25°C, RF_{EN} = 1, V_{DDRF} = 3V, f_{XTAL} = 13.55 MHz

FIGURE 9-5: TYPICAL ASK TRANSMITTER SCHEMATIC

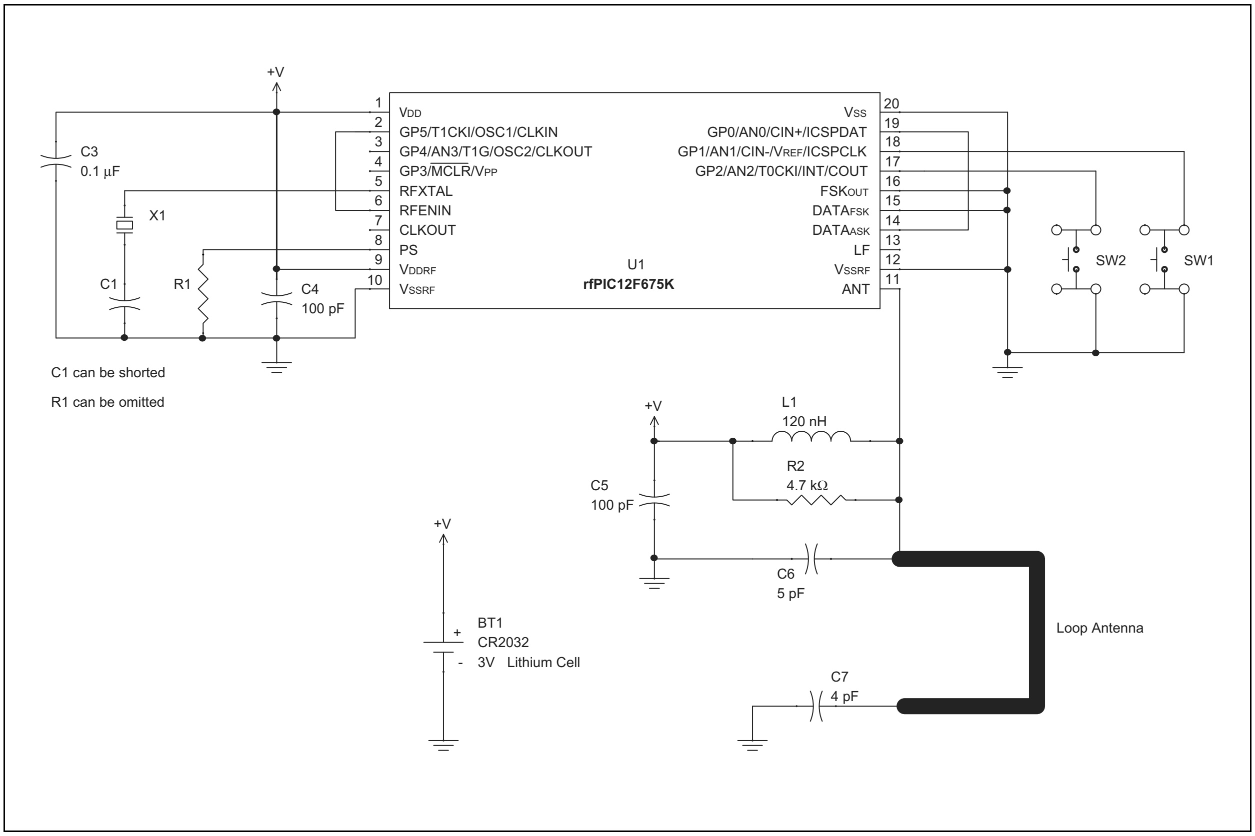
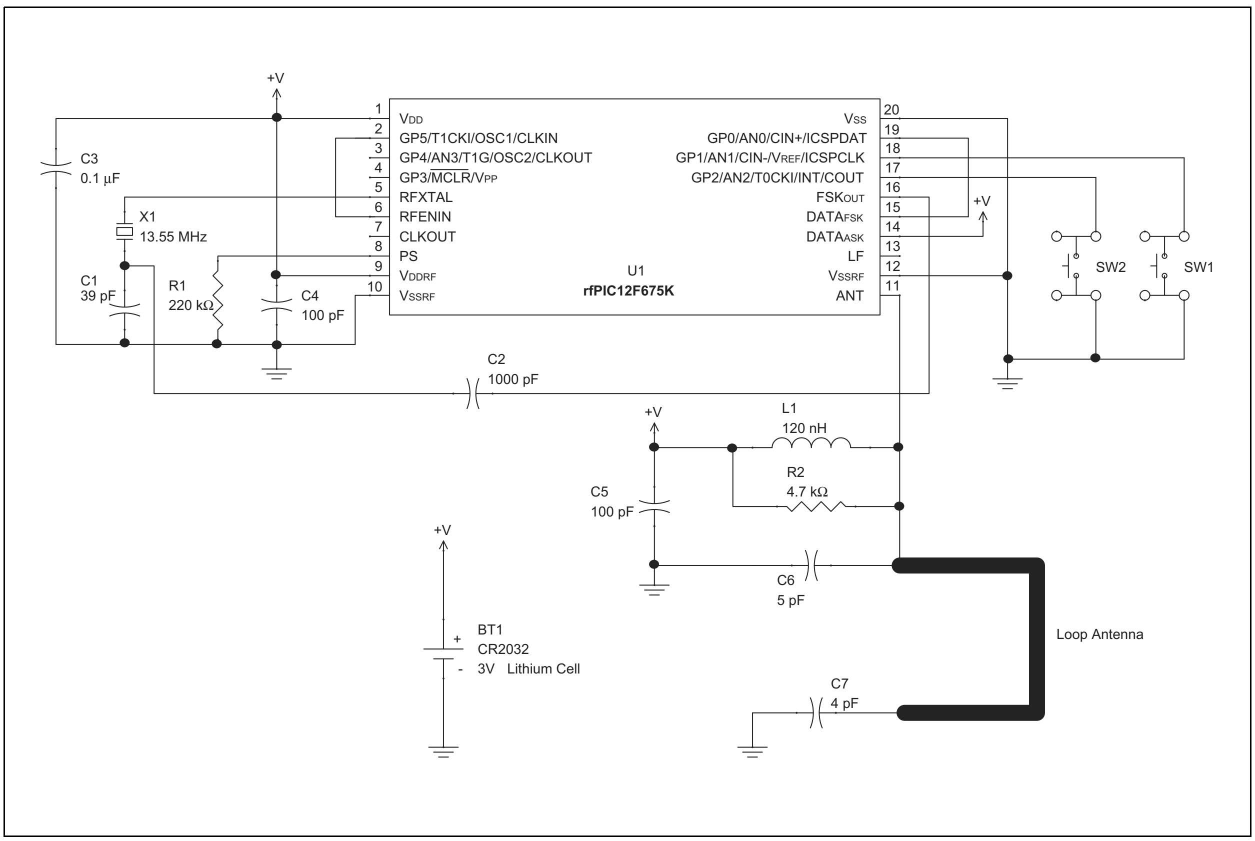


FIGURE 9-6: TYPICAL FSK TRANSMITTER SCHEMATIC



 Preliminary

10.3.1 MCLR

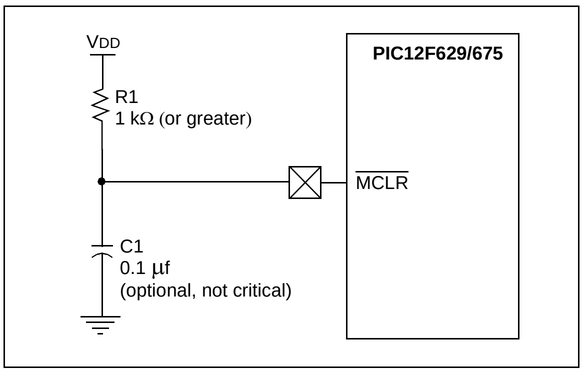
The rfPIC12F675 devices have a noise filter in the MCLR Reset path. The filter will detect and ignore small pulses.

It should be noted that a WDT Reset does not drive MCLR pin low.

The behavior of the ESD protection on the MCLR pin has been altered from previous devices of this family. Voltages applied to the pin that exceed its specification can result in both MCLR Resets and excessive current beyond the device specification during the ESD event. For this reason, Microchip recommends that the MCLR pin no longer be tied directly to V_{DD}. The use of an RC network, as shown in Figure 10-5, is suggested.

An internal MCLR option is enabled by setting the MCLRE bit in the configuration word. When enabled, MCLR is internally tied to V_{DD}. No internal pull-up option is available for the MCLR pin.

FIGURE 10-5: RECOMMENDED MCLR CIRCUIT



10.3.2 POWER-ON RESET (POR)

The on-chip POR circuit holds the chip in RESET until V_{DD} has reached a high enough level for proper operation. To take advantage of the POR, simply tie the MCLR pin through a resistor to V_{DD}. This will eliminate external RC components usually needed to create Power-on Reset. A maximum rise time for V_{DD} is required. See Electrical Specifications for details (see Section 13.0).

Note:	The POR circuit does not produce an internal RESET when V_{DD} declines.

When the device starts normal operation (exits the RESET condition), device operating parameters (i.e., voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in RESET until the operating conditions are met.

For additional information, refer to Application Note *AN607 "Power-up Trouble Shooting"*.

10.3.3 POWER-UP TIMER (PWRT)

The Power-up Timer provides a fixed 72 ms (nominal) time-out on power-up only, from POR or Brown-out Detect. The Power-up Timer operates on an internal RC oscillator. The chip is kept in RESET as long as PWRT is active. The PWRT delay allows the V_{DD} to rise to an acceptable level. A configuration bit, PWRTE can disable (if set) or enable (if cleared or programmed) the Power-up Timer. The Power-up Timer should always be enabled when Brown-out Detect is enabled.

The Power-up Time delay will vary from chip to chip and due to:

- V_{DD} variation
- Temperature variation
- Process variation

See DC parameters for details (Section 13.0).

10.3.4 OSCILLATOR START-UP TIMER (OST)

The Oscillator Start-up Timer (OST) provides a 1024 oscillator cycle (from OSC1 input) delay after the PWRT delay is over. This ensures that the crystal oscillator or resonator has started and stabilized.

The OST time-out is invoked only for XT, LP and HS modes and only on Power-on Reset or wake-up from SLEEP.

 Preliminary

11.0 INSTRUCTION SET SUMMARY

The rfPIC12F675 instruction set is highly orthogonal and is comprised of three basic categories:

- **Byte-oriented** operations
- **Bit-oriented** operations
- **Literal and control** operations

Each rfPIC12F675 instruction is a 14-bit word divided into an **opcode,** which specifies the instruction type, and one or more **operands,** which further specify the operation of the instruction. The formats for each of the categories is presented in Figure 11-1, while the various opcode fields are summarized in Table 11-1.

Table 11-2 lists the instructions recognized by the MPASM™ assembler. A complete description of each instruction is also available in the PIC *Mid-Range Reference Manual* (DS33023).

For **byte-oriented** instructions, ‘`f`’ represents a file register designator and ‘`d`’ represents a destination designator. The file register designator specifies which file register is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If ‘`d`’ is zero, the result is placed in the W register. If ‘`d`’ is one, the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, ‘`b`’ represents a bit field designator, which selects the bit affected by the operation, while ‘`f`’ represents the address of the file in which the bit is located.

For **literal and control** operations, ‘`k`’ represents an 8-bit or 11-bit constant, or literal value.

One instruction cycle consists of four oscillator periods; for an oscillator frequency of 4 MHz, this gives a normal instruction execution time of 1 μs. All instructions are executed within a single instruction cycle, unless a conditional test is true, or the program counter is changed as a result of an instruction. When this occurs, the execution takes two instruction cycles, with the second cycle executed as a `NOP`.

Note:	To maintain upward compatibility with future products, do not use the `OPTION` and `TRISIO` instructions.

All instruction examples use the format ‘`0xhh`’ to represent a hexadecimal number, where ‘`h`’ signifies a hexadecimal digit.

11.1 READ-MODIFY-WRITE OPERATIONS

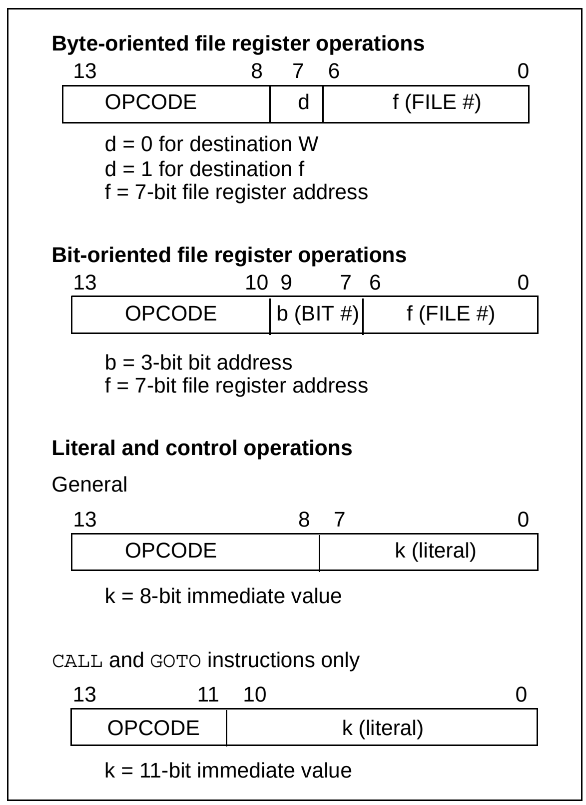
Any instruction that specifies a file register as part of the instruction performs a Read-Modify-Write (R-M-W) operation. The register is read, the data is modified, and the result is stored according to either the instruction, or the destination designator ‘d’. A read operation is performed on a register even if the instruction writes to that register.

For example, a `CLRF GPIO` instruction will read GPIO, clear all the data bits, then write the result back to GPIO. This example would have the unintended result that the condition that sets the GPIF flag would be cleared.

TABLE 11-1: OPCODE FIELD DESCRIPTIONS

Field	Description
`f`	Register file address (0x00 to 0x7F)
`W`	Working register (accumulator)
`b`	Bit address within an 8-bit file register
`k`	Literal field, constant data or label
`x`	Don't care location (= `0` or `1`). The assembler will generate code with x = `0`. It is the recommended form of use for compatibility with all Microchip software tools.
`d`	Destination select; d = `0`: store result in W, d = 1: store result in file register f. Default is d = `1`.
`PC`	Program Counter
`TO`	Time-out bit
`PD`	Power-down bit

FIGURE 11-1: GENERAL FORMAT FOR INSTRUCTIONS



DECFSZ	Decrement f, Skip if 0
Syntax:	[*label*] DECFSZ f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(f) - 1 $\rightarrow$ (destination); skip if result = 0
Status Affected:	None
Description:	The contents of register 'f' are decremented. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'. If the result is 1, the next instruction is executed. If the result is 0, then a `NOP` is executed instead, making it a 2TCY instruction.

GOTO	Unconditional Branch
Syntax:	[*label*] GOTO k
Operands:	$0 \le k \le 2047$
Operation:	k $\rightarrow$ PC<10:0> PCLATH<4:3> $\rightarrow$ PC<12:11>
Status Affected:	None
Description:	`GOTO` is an unconditional branch. The eleven-bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH<4:3>. `GOTO` is a two-cycle instruction.

INCF	Increment f
Syntax:	[*label*] INCF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(f) + 1 $\rightarrow$ (destination)
Status Affected:	Z
Description:	The contents of register 'f' are incremented. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'.

INCFSZ	Increment f, Skip if 0
Syntax:	[*label*] INCFSZ f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(f) + 1 $\rightarrow$ (destination), skip if result = 0
Status Affected:	None
Description:	The contents of register 'f' are incremented. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'. If the result is 1, the next instruction is executed. If the result is 0, a `NOP` is executed instead, making it a 2TCY instruction.

IORLW	Inclusive OR Literal with W
Syntax:	[*label*] IORLW k
Operands:	$0 \le k \le 255$
Operation:	(W) .OR. k $\rightarrow$ (W)
Status Affected:	Z
Description:	The contents of the W register are OR'ed with the eight-bit literal 'k'. The result is placed in the W register.

IORWF	Inclusive OR W with f
Syntax:	[*label*] IORWF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(W) .OR. (f) $\rightarrow$ (destination)
Status Affected:	Z
Description:	Inclusive OR the W register with register 'f'. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'.

SWAPF	**Swap Nibbles in f**
Syntax:	[*label*] SWAPF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	(f<3:0>) → (destination<7:4>), (f<7:4>) → (destination<3:0>)
Status Affected:	None
Description:	The upper and lower nibbles of register 'f' are exchanged. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed in register 'f'.

XORLW	**Exclusive OR Literal with W**
Syntax:	[*label*] XORLW k
Operands:	$0 \leq k \leq 255$
Operation:	(W) .XOR. k → (W)
Status Affected:	Z
Description:	The contents of the W register are XOR'ed with the eight-bit literal 'k'. The result is placed in the W register.

XORWF	**Exclusive OR W with f**
Syntax:	[*label*] XORWF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	(W) .XOR. (f) → (destination)
Status Affected:	Z
Description:	Exclusive OR the contents of the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

12.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers are supported with a full range of hardware and software development tools:

- Integrated Development Environment
  - MPLAB® IDE Software
- Assemblers/Compilers/Linkers
  - MPASM™ Assembler
  - MPLAB C17 and MPLAB C18 C Compilers
  - MPLINK™ Object Linker/ MPLIB™ Object Librarian
  - MPLAB C30 C Compiler
  - MPLAB ASM30 Assembler/Linker/Library
- Simulators
  - MPLAB SIM Software Simulator
  - MPLAB dsPIC30 Software Simulator
- Emulators
  - MPLAB ICE 2000 In-Circuit Emulator
  - MPLAB ICE 4000 In-Circuit Emulator
- In-Circuit Debugger
  - MPLAB ICD 2
- Device Programmers
  - PRO MATE® II Universal Device Programmer
  - PICSTART® Plus Development Programmer
- Low Cost Demonstration Boards
  - PICDEM™ 1 Demonstration Board
  - PICDEM.net™ Demonstration Board
  - PICDEM 2 Plus Demonstration Board
  - PICDEM 3 Demonstration Board
  - PICDEM 4 Demonstration Board
  - PICDEM 17 Demonstration Board
  - PICDEM 18R Demonstration Board
  - PICDEM LIN Demonstration Board
  - PICDEM USB Demonstration Board
- Evaluation Kits
  - KEELOQ®
  - PICDEM MSC
  - microID®
  - CAN
  - PowerSmart®
  - Analog

12.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8/16-bit microcontroller market. The MPLAB IDE is a Windows® based application that contains:

- An interface to debugging tools
  - simulator
  - programmer (sold separately)
  - emulator (sold separately)
  - in-circuit debugger (sold separately)
- A full-featured editor with color coded context
- A multiple project manager
- Customizable data windows with direct edit of contents
- High level source code debugging
- Mouse over variable inspection
- Extensive on-line help

The MPLAB IDE allows you to:

- Edit your source files (either assembly or C)
- One touch assemble (or compile) and download to PIC MCU emulator and simulator tools (automatically updates all project information)
- Debug using:
  - source files (assembly or C)
  - absolute listing file (mixed assembly and C)
  - machine code

MPLAB IDE supports multiple debugging tools in a single development paradigm, from the cost effective simulators, through low cost in-circuit debuggers, to full-featured emulators. This eliminates the learning curve when upgrading to tools with increasing flexibility and power.

12.2 MPASM Assembler

The MPASM assembler is a full-featured, universal macro assembler for all PIC MCUs.

The MPASM assembler generates relocatable object files for the MPLINK object linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code and COFF files for debugging.

The MPASM assembler features include:

- Integration into MPLAB IDE projects
- User defined macros to streamline assembly code
- Conditional assembly for multi-purpose source files
- Directives that allow complete control over the assembly process

12.20 PICDEM 18R PIC18C601/801 Demonstration Board

The PICDEM 18R demonstration board serves to assist development of the PIC18C601/801 family of Microchip microcontrollers. It provides hardware implementation of both 8-bit Multiplexed/De-multiplexed and 16-bit Memory modes. The board includes 2 Mb external FLASH memory and 128 Kb SRAM memory, as well as serial EEPROM, allowing access to the wide range of memory types supported by the PIC18C601/801.

12.21 PICDEM LIN PIC16C43X Demonstration Board

The powerful LIN hardware and software kit includes a series of boards and three PIC microcontrollers. The small footprint PIC16C432 and PIC16C433 are used as slaves in the LIN communication and feature on-board LIN transceivers. A PIC16F874 FLASH microcontroller serves as the master. All three microcontrollers are programmed with firmware to provide LIN bus communication.

12.22 PICkit™ 1 FLASH Starter Kit

A complete "development system in a box", the PICkit FLASH Starter Kit includes a convenient multi-section board for programming, evaluation, and development of 8/14-pin FLASH PIC® microcontrollers. Powered via USB, the board operates under a simple Windows GUI. The PICkit 1 Starter Kit includes the user's guide (on CD ROM), PICkit 1 tutorial software and code for various applications. Also included are MPLAB® IDE (Integrated Development Environment) software, software and hardware "Tips 'n Tricks for 8-pin FLASH PIC® Microcontrollers" Handbook and a USB Interface Cable. Supports all current 8/14-pin FLASH PIC microcontrollers, as well as many future planned devices.

12.23 PICDEM USB PIC16C7X5 Demonstration Board

The PICDEM USB Demonstration Board shows off the capabilities of the PIC16C745 and PIC16C765 USB microcontrollers. This board provides the basis for future USB products.

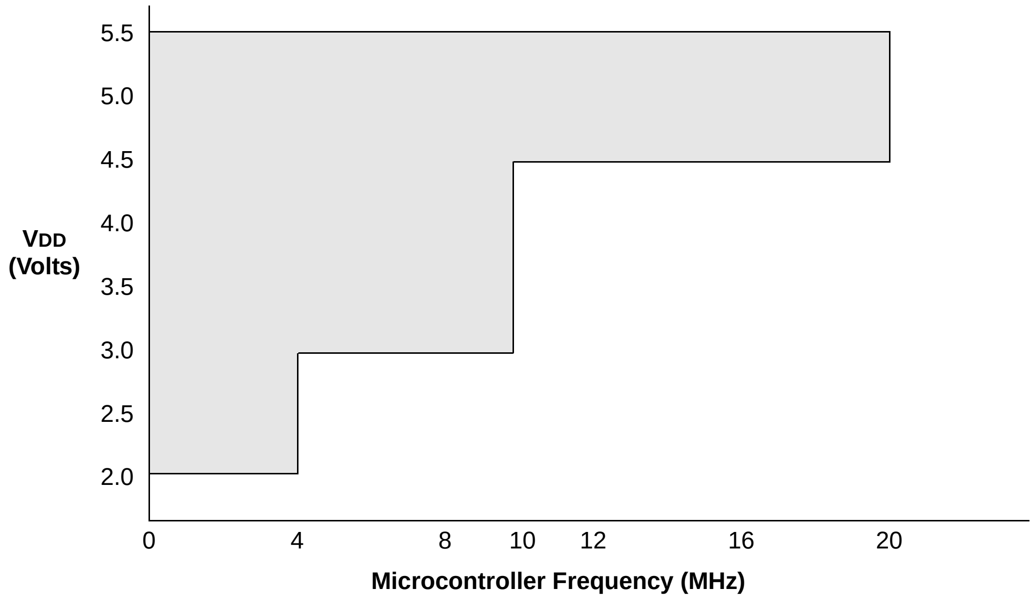
12.24 Evaluation and Programming Tools

In addition to the PICDEM series of circuits, Microchip has a line of evaluation kits and demonstration software for these products.

- KEELOQ evaluation and programming tools for Microchip's HCS Secure Data Products
- CAN developers kit for automotive network applications
- Analog design boards and filter design software
- PowerSmart battery charging evaluation/ calibration kits
- IrDA® development kit
- microID development and rfLab™ development software
- SEEVAL® designer kit for memory evaluation and endurance calculations
- PICDEM MSC demo boards for Switching mode power supply, high power IR driver, delta sigma ADC, and flow rate sensor

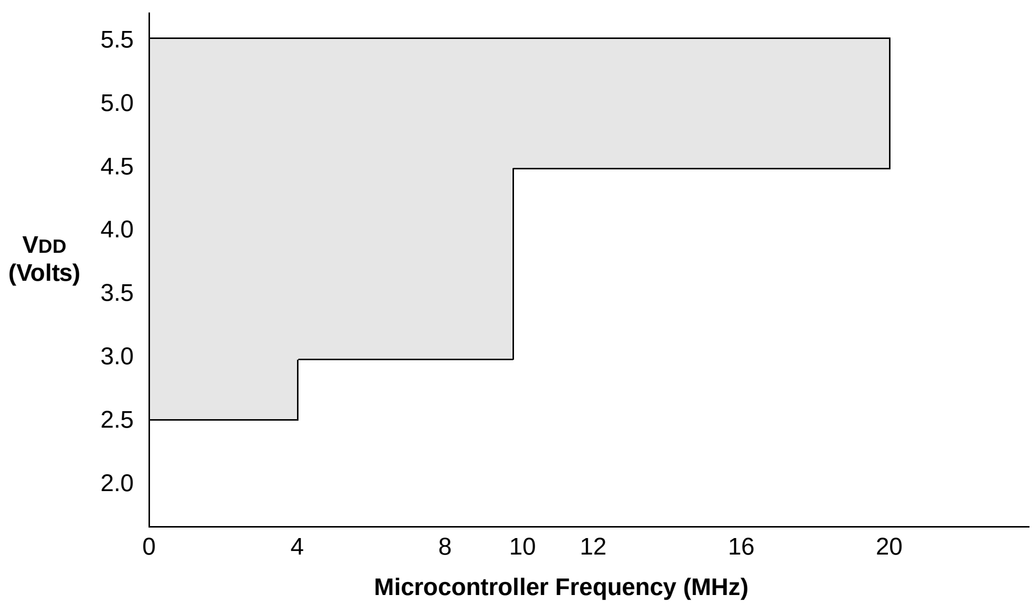
Check the Microchip web page and the latest Product Line Card for the complete list of demonstration and evaluation kits.

FIGURE 13-1: rfPIC12F675 WITH A/D DISABLED VOLTAGE-FREQUENCY GRAPH, -40°C ≤ TA ≤ +125°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

FIGURE 13-2: rfPIC12F675 WITH A/D ENABLED VOLTAGE-FREQUENCY GRAPH, -40°C ≤ TA ≤ +125°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

13.1 DC Characteristics: rfPIC12F675-I (Industrial), rfPIC12F675-E (Extended)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	VDD	**Supply Voltage**					FOSC < = 4 MHz:
D001			2.0	—	5.5	V	rfPIC12F675 with A/D off
D001A			2.2	—	5.5	V	rfPIC12F675 with A/D on, 0°C to +125°C
D001B			2.5	—	5.5	V	rfPIC12F675 with A/D on, -40°C to +125°C
D001C			3.0	—	5.5	V	4 MHz < FOSC < = 10 MHz
D001D			4.5	—	5.5	V	FOSC > 10 MHz
D002	VDR	**RAM Data Retention Voltage**(1)	1.5*	—	—	V	Device in SLEEP mode
D003	VPOR	**VDD Start Voltage** to ensure internal Power-on Reset signal	—	VSS	—	V	See section on Power-on Reset for details
D004	SVDD	**VDD Rise Rate** to ensure internal Power-on Reset signal	0.05*	—	—	V/ms	See section on Power-on Reset for details
D005	VBOD		—	2.1	—	V	
	VDDRF	**RF Transmitter Supply Voltage**					
D006			2.0	—	5.5	V	Output Power = 4 dBm
D006A			3.0	—	5.5	V	Output Power = 7.5 dBm
D006B			4.0	—	5.5	V	Output Power = 8.5 dBm
D006C			5.0	—	5.5	V	Output Power = 9 dBm
D007	VLVD	**RF Low Voltage Disable**	1.8	1.85	1.9	V	TA =+23°C, RFEN = VDDRF

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

13.4 DC Characteristics: rfPIC12F675-E (Extended)

		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C for extended					
Param No.	Device Characteristics	Min	Typ†	Max	Units	Conditions: VDD	Conditions: Note
D010E	**Supply Current (IDD)**(3)	—	9	16	μA	2.0	FOSC = 32 kHz LP Oscillator Mode
		—	18	28	μA	3.0	
		—	35	54	μA	5.0	
D011E		—	110	150	μA	2.0	FOSC = 1 MHz XT Oscillator Mode
		—	190	280	μA	3.0	
		—	330	450	μA	5.0	
D012E		—	220	280	μA	2.0	FOSC = 4 MHz XT Oscillator Mode
		—	370	650	μA	3.0	
		—	0.6	1.4	mA	5.0	
D013E		—	70	110	μA	2.0	FOSC = 1 MHz EC Oscillator Mode
		—	140	250	μA	3.0	
		—	260	390	μA	5.0	
D014E		—	180	250	μA	2.0	FOSC = 4 MHz EC Oscillator Mode
		—	320	470	μA	3.0	
		—	580	850	μA	5.0	
D015E		—	340	450	μA	2.0	FOSC = 4 MHz INTOSC Mode
		—	500	780	μA	3.0	
		—	0.8	1.1	mA	5.0	
D016E		—	180	250	μA	2.0	FOSC = 4 MHz EXTRC Mode
		—	320	450	μA	3.0	
		—	580	800	μA	5.0	
D017E		—	2.1	2.95	mA	4.5	FOSC = 20 MHz HS Oscillator Mode
		—	2.4	3.0	mA	5.0	

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The test conditions for all IDD measurements in Active Operation mode are: OSC1 = external square wave, from rail to rail; all I/O pins tri-stated, pulled to VDD; $\overline{\text{MCLR}}$ = VDD; WDT disabled.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

3: Total device current is the sum of IDD from VDD and IDDRF from VDDRF.

13.6 DC Characteristics: rfPIC12F675K

		Standard Operating Conditions (unless otherwise stated) Operating temperature TA = +23°C Operating Frequency f_c = 315 MHz					
Param No.	Device Characteristics	Min	Typ	Max	Units	Conditions	
						VDD	Note
D018A	RF Transmitter Current (IDDRF)(2)	2.0	2.7	5.0	mA	3.0	Power Step 0, RFEN=DATAASK=1
D018B		2.9	3.5	7.0	mA	3.0	Power Step 1, RFEN=DATAASK=1
D018C		3.2	4.7	7.9	mA	3.0	Power Step 2, RFEN=DATAASK=1
D018D		4.5	6.5	11	mA	3.0	Power Step 3, RFEN=DATAASK=1
D018E		7.0	10.7	16	mA	3.0	Power Step 4, RFEN=DATAASK=1

Note 1: The supply current is mainly a function of the operating voltage and frequency. Other factors such as output loading and temperature also have an impact on the current consumption.

2: Total device current is the sum of IDD from VDD and IDDRF from VDDRF.

13.7 DC Characteristics: rfPIC12F675F

		Standard Operating Conditions (unless otherwise stated) Operating temperature TA = +23°C Operating Frequency f_c = 434 MHz					
Param No.	Device Characteristics	Min	Typ	Max	Units	Conditions	
						VDD	Note
D018A	RF Transmitter Current (IDDRF)(2)	2.0	2.7	5.0	mA	3.0	Power Step 0, RFEN=DATAASK=1
D018B		2.9	3.5	7.0	mA	3.0	Power Step 1, RFEN=DATAASK=1
D018C		3.2	4.7	7.9	mA	3.0	Power Step 2, RFEN=DATAASK=1
D018D		4.5	6.5	11	mA	3.0	Power Step 3, RFEN=DATAASK=1
D018E		7.0	10.7	16	mA	3.0	Power Step 4, RFEN=DATAASK=1

Note 1: The supply current is mainly a function of the operating voltage and frequency. Other factors such as output loading and temperature also have an impact on the current consumption.

2: Total device current is the sum of IDD from VDD and IDDRF from VDDRF.

13.8 DC Characteristics: rfPIC12F675H

		Standard Operating Conditions (unless otherwise stated) Operating temperature TA = +23°C Operating Frequency f_c = 868 MHz					
Param No.	Device Characteristics	Min	Typ	Max	Units	Conditions	
						VDD	Note
D018A	RF Transmitter Current (IDDRF)(2)	2.6	4.0	6.5	mA	3.0	Power Step 0, RFEN=DATAASK=1
D018B		3.5	5.3	8.5	mA	3.0	Power Step 1, RFEN=DATAASK=1
D018C		4.5	6.7	11	mA	3.0	Power Step 2, RFEN=DATAASK=1
D018D		6.0	9.0	14	mA	3.0	Power Step 3, RFEN=DATAASK=1
D018E		9.0	14.0	20	mA	3.0	Power Step 4, RFEN=DATAASK=1

Note 1: The supply current is mainly a function of the operating voltage and frequency. Other factors such as output loading and temperature also have an impact on the current consumption.

2: Total device current is the sum of IDD from VDD and IDDRF from VDDRF.

13.11 TIMING PARAMETER SYMBOLOGY

The timing parameter symbols have been created with one of the following formats:

1. TppS2ppS
2. TppS

T			
F	Frequency	T	Time

Lowercase letters (pp) and their meanings:

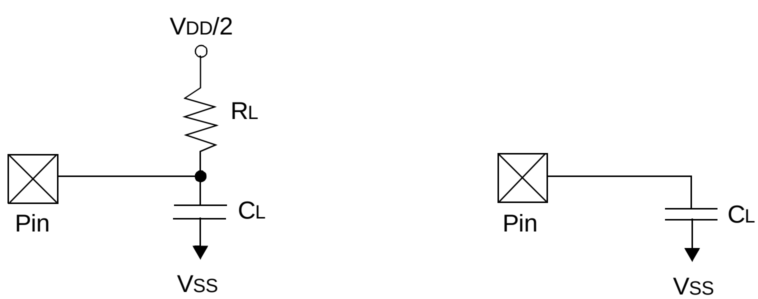
pp			
cc	CCP1	osc	OSC1
ck	CLKOUT	rd	$\overline{\text{RD}}$
cs	$\overline{\text{CS}}$	rw	$\overline{\text{RD}}$ or $\overline{\text{WR}}$
di	SDI	sc	SCK
do	SDO	ss	$\overline{\text{SS}}$
dt	Data in	t0	T0CKI
io	I/O port	t1	T1CKI
mc	$\overline{\text{MCLR}}$	wr	$\overline{\text{WR}}$

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance

FIGURE 13-4: LOAD CONDITIONS

Load Condition 1   Load Condition 2

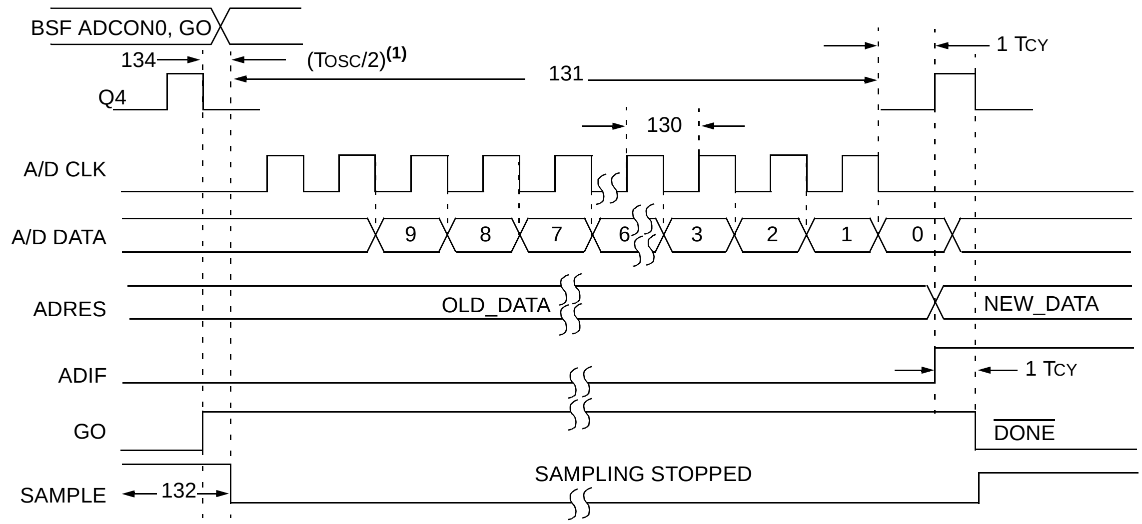


R_L = 464Ω

C_L = 50 pF for all pins

15 pF for OSC2 output

FIGURE 13-10: rfPIC12F675 A/D CONVERSION TIMING (NORMAL MODE)



Note 1: If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the `SLEEP` instruction to be executed.

TABLE 13-9: rfPIC12F675 A/D CONVERSION REQUIREMENTS

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
130	TAD	A/D Clock Period	1.6	—	—	μs	TOSC based, VREF ≥ 3.0V
			3.0*	—	—	μs	TOSC based, VREF full range
130	TAD	A/D Internal RC Oscillator Period					ADCS<1:0> = 11 (RC mode)
			3.0*	6.0	9.0*	μs	At VDD = 2.5V
			2.0*	4.0	6.0*	μs	At VDD = 5.0V
131	TCNV	Conversion Time (not including Acquisition Time)(1)	—	11	—	TAD	Set GO bit to new data in A/D result register
132	TACQ	Acquisition Time	**(Note 2)**	11.5	—	μs	
			5*	—	—	μs	The minimum time is the amplifier settling time. This may be used if the “new” input voltage has not changed by more than 1 LSb (i.e., 4.1 mV @ 4.096V) from the last sampled voltage (as stored on CHOLD).
134	TGO	Q4 to A/D Clock Start	—	TOSC/2	—	—	If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the `SLEEP` instruction to be executed.

* These parameters are characterized but not tested.

† Data in ‘Typ’ column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: ADRES register may be read on the following TCY cycle.

2: See Section 7.1 for minimum conditions.

FIGURE 14-5: MAXIMUM IPD vs. VDD OVER TEMP (+85°C)

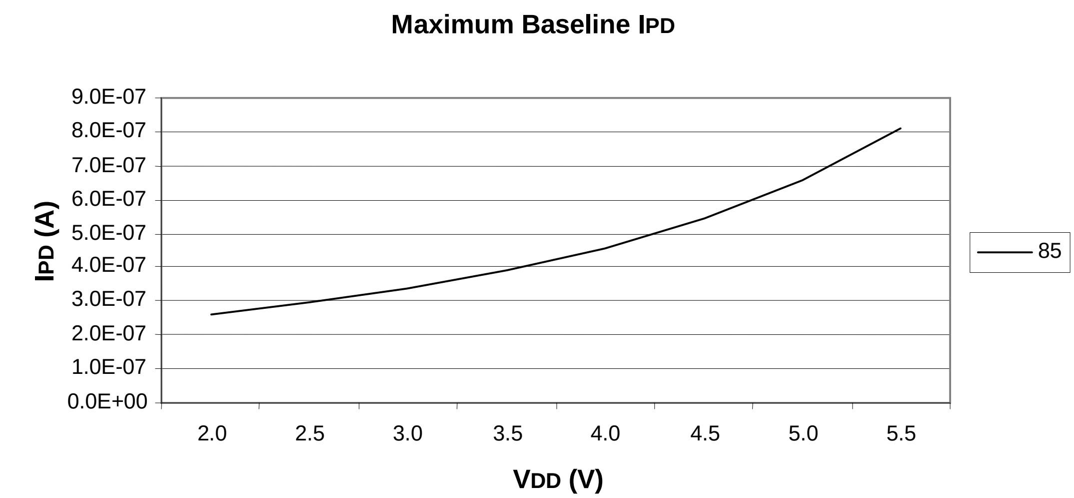
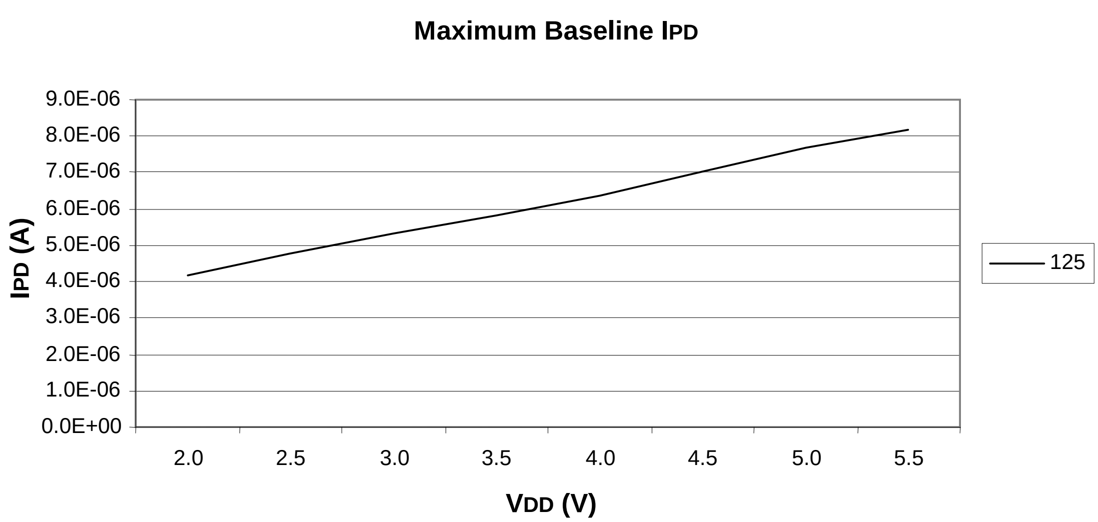


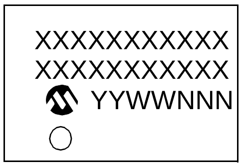
FIGURE 14-6: MAXIMUM IPD vs. VDD OVER TEMP (+125°C)



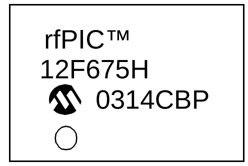
15.0 PACKAGING INFORMATION

15.1 Package Marking Information

20-Lead SSOP



Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.