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What Are <u>Embedded - Microcontrollers -</u> <u>Application Specific</u>?

Application enacific microcontrollars are analyzared to

Details

Details	
Product Status	Active
Applications	RKE, Security Systems
Core Processor	PIC
Program Memory Type	FLASH (1.75kB)
Controller Series	rfPIC™
RAM Size	64 x 8
Interface	-
Number of I/O	6
Voltage - Supply	2V ~ 5.5V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/rfpic12f675h-i-ss

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2.2.2 SPECIAL FUNCTION REGISTERS

The Special Function registers are registers used by the CPU and peripheral functions for controlling the desired operation of the device (see Table 2-1). These registers are static RAM.

The special registers can be classified into two sets: core and peripheral. The Special Function registers associated with the "core" are described in this section. Those related to the operation of the peripheral features are described in the section of that peripheral feature.

FIGURE 2-2: DATA MEMORY MAP OF THE rfPIC12F675

		rfPIC12F675	
	File Address	A	File ddres
Indirect addr. ⁽¹⁾	00h	Indirect addr. ⁽¹⁾	80ŀ
TMR0	01h	OPTION_REG	81ŀ
PCL	02h	PCL	82ŀ
STATUS	03h	STATUS	83ł
FSR	04h	FSR	84ł
GPIO	05h	TRISIO	85ł
	06h		86ł
	07h		87ł
	08h		88ŀ
	09h		89ŀ
PCLATH	0Ah	PCLATH	8AI
INTCON	0Bh	INTCON	8BI
PIR1	0Ch	PIE1	8C
	0Dh		8D
TMR1L	0Eh	PCON	8EI
TMR1H	0Fh		8Fł
T1CON	10h	OSCCAL	90ŀ
	11h		911
	12h		921
	13h		93h
	14h		941
	15h	WPU	95ł
	16h	IOC	961
	17h	100	97h
	18h		981
CMCON	19h	VRCON	99h
OMOON	1Ah	EEDATA	9Ał
	1Bh	EEADR	9Bł
	1Ch	EECON1	9CI
	1Dh	EECON1	901 9D1
ADRESH	1Eh	ADRESL	9Eł
	-		
ADCON0	1Fh 20h	ANSEL	9Fh A0h
General Purpose Registers 64 Bytes		accesses 20h-5Fh	
	5Fh 60h		DF E0
Bank 0	7Fh	Bank 1	FFI

2.2.2.6 PCON Register

The Power Control (PCON) register contains flag bits to differentiate between a:

- Power-on Reset (POR)
- Brown-out Detect (BOD)
- Watchdog Timer Reset (WDT)
- External MCLR Reset

The PCON Register bits are shown in Register 2-6.

REGISTER 2-6: PCON — POWER CONTROL REGISTER (ADDRESS: 8Eh)

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-x
_	—	—	—	— — POR		BOD	
bit 7							bit 0

bit 7-2 Unimplemented: Read as '0'

bit 1 **POR:** Power-on Reset STATUS bit

1 = No Power-on Reset occurred

0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)

bit 0 BOD: Brown-out Detect STATUS bit

- 1 = No Brown-out Detect occurred
- 0 = A Brown-out Detect occurred (must be set in software after a Brown-out Detect occurs)

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented	bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

2.2.2.7 OSCCAL Register

bit 7-2

bit 1-0

The Oscillator Calibration register (OSCCAL) is used to calibrate the internal 4 MHz oscillator. It contains 6 bits to adjust the frequency up or down to achieve 4 MHz.

The OSCCAL register bits are shown in Register 2-7.

REGISTER 2-7: OSCCAL — OSCILLATOR CALIBRATION REGISTER (ADDRESS: 90h)

R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0				
CAL5	CAL4	CAL3	CAL2	CAL1	CAL0	_	—				
bit 7 bit											
CAL5:CAL0: 6-bit Signed Oscillator Calibration bits 111111 = Maximum frequency 100000 = Center frequency 000000 = Minimum frequency											
Unimplemented: Read as '0' Legend:											
R = Readable bit $W = Writable bit$ $U = Unimplemented bit, read as '0'$											
- n = Value a	at POR	'1' = Bi	t is set	'0' = Bit is cleared x = Bit is unknown							

3.2.2 INTERRUPT-ON-CHANGE

Each of the GPIO pins is individually configurable as an interrupt-on-change pin. Control bits IOC enable or disable the interrupt function for each pin. Refer to Register 3-4. The interrupt-on-change is disabled on a Power-on Reset.

For enabled interrupt-on-change pins, the values are compared with the old value latched on the last read of GPIO. The 'mismatch' outputs of the last read are OR'd together to set, the GP Port Change Interrupt flag bit (GPIF) in the INTCON register. This interrupt can wake the device from SLEEP. The user, in the Interrupt Service Routine, can clear the interrupt in the following manner:

- a) Any read or write of GPIO. This will end the mismatch condition.
- b) Clear the flag bit GPIF.

A mismatch condition will continue to set flag bit GPIF. Reading GPIO will end the mismatch condition and allow flag bit GPIF to be cleared.

Note: If a change on the I/O pin should occur when the read operation is being executed (start of the Q2 cycle), then the GPIF interrupt flag may not get set.

REGISTER 3-4: IOC — INTERRUPT-ON-CHANGE GPIO REGISTER (ADDRESS: 96h)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
—	— IOC		— IOC5 IOC4 IOC3		IOC2	IOC1	IOC0	
bit 7							bit 0	

bit 7-6 Unimplemented: Read as '0'

bit 5-0 IOC<5:0>: Interrupt-on-Change GPIO Control bit

1 = Interrupt-on-change enabled

0 = Interrupt-on-change disabled

Note 1: Global interrupt enable (GIE) must be enabled for individual interrupts to be recognized.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented b	oit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

4.0 TIMER0 MODULE

The Timer0 module timer/counter has the following features:

- 8-bit timer/counter
- Readable and writable
- 8-bit software programmable prescaler
- · Internal or external clock select
- Interrupt on overflow from FFh to 00h
- Edge select for external clock

Figure 4-1 is a block diagram of the Timer0 module and the prescaler shared with the WDT.

Note:		information						
	module is available in the PICmicro™ Mid-							
	Range Refe	erence Manu	al (D	S3302	23).			

4.1 Timer0 Operation

Timer mode is selected by clearing the TOCS bit (OPTION_REG<5>). In Timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If TMR0 is written, the increment is inhibited for the following two instruction cycles. The user can work around this by writing an adjusted value to the TMR0 register.

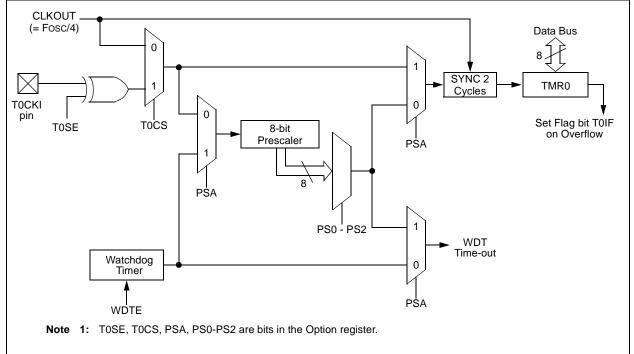
Counter mode is selected by setting the T0CS bit (OPTION_REG<5>). In this mode, the Timer0 module will increment either on every rising or falling edge of pin GP2/T0CKI. The incrementing edge is determined by the source edge (T0SE) control bit (OPTION_REG<4>). Clearing the T0SE bit selects the rising edge.

Note: Counter mode has specific external clock requirements. Additional information on these requirements is available in the *PICmicro™ Mid-Range Reference Manual* (DS33023).

4.2 Timer0 Interrupt

A Timer0 interrupt is generated when the TMR0 register timer/counter overflows from FFh to 00h. This overflow sets the T0IF bit. The interrupt can be masked by clearing the T0IE bit (INTCON<5>). The T0IF bit (INTCON<2>) must be cleared in software by the Timer0 module Interrupt Service Routine before reenabling this interrupt. The Timer0 interrupt cannot wake the processor from SLEEP since the timer is shut-off during SLEEP.





5.0 TIMER1 MODULE WITH GATE CONTROL

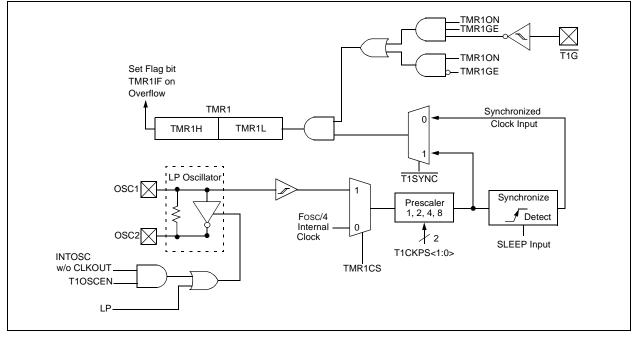
The rfPIC12F675 devices have a 16-bit timer. Figure 5-1 shows the basic block diagram of the Timer1 module. Timer1 has the following features:

- 16-bit timer/counter (TMR1H:TMR1L)
- Readable and writable
- Internal or external clock selection
- Synchronous or asynchronous operation
- Interrupt on overflow from FFFFh to 0000h
- Wake-up upon overflow (Asynchronous mode)
- Optional external enable input $(\overline{T1G})$
- · Optional LP oscillator

FIGURE 5-1: TIMER1 BLOCK DIAGRAM

The Timer1 Control register (T1CON), shown in Register 5-1, is used to enable/disable Timer1 and select the various features of the Timer1 module.

Note:	Additional information on timer modules is
	available in the PICmicro [™] Mid-Range
	Reference Manual (DS33023).

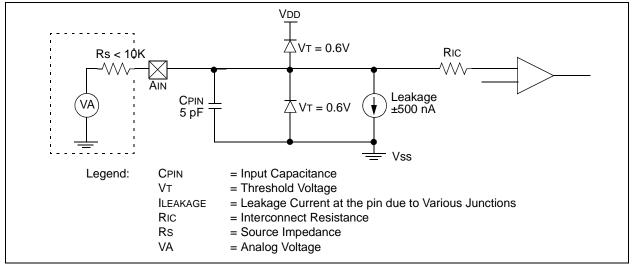


6.3 Analog Input Connection Considerations

A simplified circuit for an analog input is shown in Figure 6-3. Since the analog pins are connected to a digital output, they have reverse biased diodes to VDD and Vss. The analog input, therefore, must be between Vss and VDD. If the input voltage deviates from this

range by more than 0.6V in either direction, one of the diodes is forward biased and a latchup may occur. A maximum source impedance of $10 \text{ k}\Omega$ is recommended for the analog sources. Any external component connected to an analog input pin, such as a capacitor or a Zener diode, should have very little leakage current.

FIGURE 6-3: ANALOG INPUT MODE



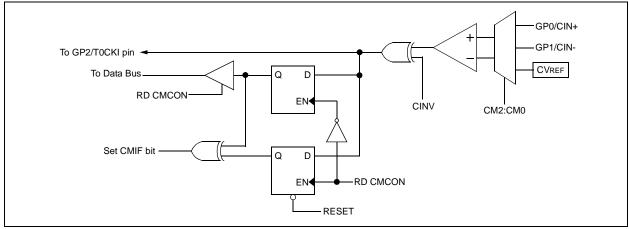
6.4 Comparator Output

The comparator output, COUT, is read through the CMCON register. This bit is read-only. The comparator output may also be directly output to the GP2 pin in three of the eight possible modes, as shown in Figure 6-2. When in one of these modes, the output on GP2 is asynchronous to the internal clock. Figure 6-4 shows the comparator output block diagram.

The TRISIO<2> bit functions as an output enable/ disable for the GP2 pin while the comparator is in an Output mode.

- Note 1: When reading the GPIO register, all pins configured as analog inputs will read as a '0'. Pins configured as digital inputs will convert an analog input according to the TTL input specification.
 - 2: Analog levels on any pin that is defined as a digital input, may cause the input buffer to consume more current than is specified.

FIGURE 6-4: MODIFIED COMPARATOR OUTPUT BLOCK DIAGRAM



ANOLL					,					
U-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1			
	ADCS2	ADCS1	ADCS0	ANS3	ANS2	ANS1	ANS0			
bit 7			· · · · ·				bit 0			
Unimplen	n ented: Rea	d as '0'.								
ADCS<2:	0>: A/D Conי	version Clo	ck Select bits	;						
001 = Fos 010 = Fos x11 = Fro 100 = Fos 101 = Fos	SC/8 SC/32 C (clock deriv SC/4 SC/16	ed from a d	edicated inte	ernal oscillator	⁻ = 500 kHz	max)				
 ANS3:ANS0: Analog Select bits (Between analog or digital function on pins AN<3:0>, respectively.) 1 = Analog input; pin is assigned as analog input⁽¹⁾ 0 = Digital I/O; pin is assigned to port or special function 										
Note 1	Note 1: Setting a pin to an analog input automatically disables the digital input circuitry, weak pull-ups, and interrupt-on-change. The corresponding TRISIO bit must be set to Input mode in order to allow external control of the voltage on the pin.									
	— bit 7 Unimplem ADCS<2:: 000 = Fos 001 = Fos 010 = Fos 100 = Fos 101 = Fos 110 = Fos	U-0R/W-0-ADCS2bit 7Unimplemented: RealADCS<2:0>: A/D Conv $000 = Fosc/2$ $001 = Fosc/8$ $010 = Fosc/8$ $010 = Fosc/32$ x11 = FRc (clock deriv) $100 = Fosc/4$ $101 = Fosc/16$ $110 = Fosc/64$ ANS3:ANS0: Analog S(Between analog or dig1 = Analog input; pin is0 = Digital I/O; pin is asNote 1: Setting a pweak pull-to	U-0R/W-0R/W-0-ADCS2ADCS1bit 7Unimplemented: Read as '0'.ADCS<2:0>: A/D Conversion Clost000 = Fosc/2001 = Fosc/2001 = Fosc/8010 = Fosc/32x11 = FRC (clock derived from a d100 = Fosc/4101 = Fosc/16110 = Fosc/64ANS3:ANS0: Analog Select bits(Between analog or digital function1 = Analog input; pin is assigned to pNote 1: Setting a pin to an arweak pull-ups, and interview	U-0R/W-0R/W-0R/W-0—ADCS2ADCS1ADCS0bit 7Unimplemented: Read as '0'.ADCS<2:0>: A/D Conversion Clock Select bits000 = Fosc/2001 = Fosc/8010 = Fosc/8010 = Fosc/32x11 = FRC (clock derived from a dedicated inter100 = Fosc/4101 = Fosc/16110 = Fosc/64ANS3:ANS0: Analog Select bits(Between analog or digital function on pins AN-1 = Analog input; pin is assigned as analog input a weak pull-ups, and interrupt-on-character	U-0 R/W-0 R/W-0 R/W-0 R/W-1	U-0 R/W-0 R/W-0 R/W-0 R/W-1 R/W-1 — ADCS2 ADCS1 ADCS0 ANS3 ANS2 bit 7 Unimplemented: Read as '0'. ADCS-2:0>: A/D Conversion Clock Select bits 000 = Fosc/2 001 = Fosc/8 010 = Fosc/8 010 = Fosc/8 010 = Fosc/32 x11 = FRC (clock derived from a dedicated internal oscillator = 500 kHz 100 = Fosc/4 101 = Fosc/16 110 = Fosc/64 ANS3:ANS0: Analog Select bits (Between analog or digital function on pins AN<3:0>, respectively.) 1 = Analog input; pin is assigned as analog input ⁽¹⁾ 0 = Digital I/O; pin is assigned to port or special function Note 1: Setting a pin to an analog input automatically disables the weak pull-ups, and interrupt-on-change. The corresponding	U-0 R/W-0 R/W-0 R/W-1 R/W-1 R/W-1 — ADCS2 ADCS1 ADCS0 ANS3 ANS2 ANS1 bit 7 Unimplemented: Read as '0'. ADCS A/D Conversion Clock Select bits 000 = Fosc/2 01 = Fosc/8 010 = Fosc/8 010 = Fosc/8 010 = Fosc/8 010 = Fosc/16 101 = Fosc/16 101 = Fosc/16 101 = Fosc/64 ANS3:ANS0: Analog Select bits (Between analog or digital function on pins AN<3:0>, respectively.) 1 = Analog input; pin is assigned as analog input ⁽¹⁾ 0 = Digital I/O; pin is assigned to port or special function Note 1: Setting a pin to an analog input automatically disables the digital input weak pull-ups, and interrupt-on-change. The corresponding TRISIO bit of the set of the			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented	l bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

REGISTER 7-2: ANSEL — ANALOG SELECT REGISTER (ADDRESS: 9Fh)

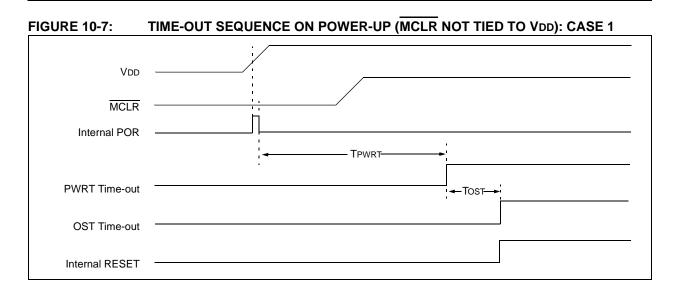


FIGURE 10-8: TIME-OUT SEQUENCE ON POWER-UP (MCLR NOT TIED TO VDD): CASE 2

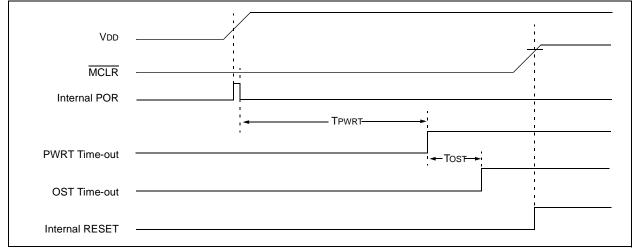


FIGURE 10-9: TIME-OUT SEQUENCE ON POWER-UP (MCLR TIED TO VDD)

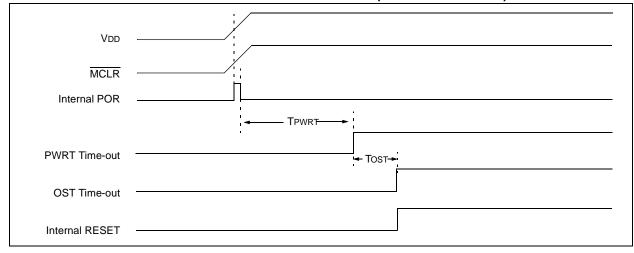


TABLE 11-2: rfPIC12F675 INSTRUCTION SET

Mner	nonic,	Description Cycles			14-Bit	Opcode	9	Status	Notos
Operands		Description		MSb			LSb	Affected	Notes
		BYTE-ORIENTED FILE	E REGISTER OPE	RATIC	ONS				
ADDWF	f, d	Add W and f	1	00	0111	dfff	ffff	C,DC,Z	1,2
ANDWF	f, d	AND W with f	1	00	0101	dfff	ffff	Z	1,2
CLRF	f	Clear f	1	00	0001	lfff	ffff	Z	2
CLRW	-	Clear W	1	00	0001	0xxx	xxxx	Z	
COMF	f, d	Complement f	1	00	1001	dfff	ffff	Z	1,2
DECF	f, d	Decrement f	1	00	0011	dfff	ffff	Z	1,2
DECFSZ	f, d	Decrement f, Skip if 0	1(2)	00	1011	dfff	ffff		1,2,3
INCF	f, d	Increment f	1	00	1010	dfff	ffff	Z	1,2
INCFSZ	f, d	Increment f, Skip if 0	1(2)	00	1111	dfff	ffff		1,2,3
IORWF	f, d	Inclusive OR W with f	1	00	0100	dfff	ffff	Z	1,2
MOVF	f, d	Move f	1	00	1000	dfff	ffff	z	1,2
MOVWF	f	Move W to f	1	0.0	0000	lfff	ffff		,
NOP	-	No Operation	1	0.0	0000	0xx0	0000		
RLF	f, d	Rotate Left f through Carry	1	00	1101		ffff	С	1,2
RRF	f, d	Rotate Right f through Carry	1	00	1100		ffff	C	1,2
SUBWF	f, d	Subtract W from f	1	00	0010		ffff	C,DC,Z	1,2
SWAPF	f, d	Swap nibbles in f	1	00	1110	dfff	ffff	0,20,2	1,2
XORWF	f, d	Exclusive OR W with f	1	00	0110	dfff	ffff	Z	1,2
	., a	BIT-ORIENTED FILE				4111		_	- ,=
BCF	f, b	Bit Clear f	1	1		bfff	ffff		1,2
BSF	f, b	Bit Set f		01					
	,			01		bfff			1,2
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	01		bfff			3 3
BTFSS	f, b	Bit Test f, Skip if Set		01	11bb	bfff	ffff		3
	<u> </u>			T				0.00.7	
ADDLW	k	Add literal and W	1	11		kkkk		C,DC,Z	
ANDLW	k	AND literal with W	1	11		kkkk		Z	
CALL	k	Call subroutine	2	10		kkkk			
CLRWDT	-	Clear Watchdog Timer	1	00	0000	0110	0100	TO,PD	
GOTO	k	Go to address	2	10		kkkk		_	
IORLW	k	Inclusive OR literal with W	1	11	1000		kkkk	Z	
MOVLW	k	Move literal to W	1	11		kkkk			
RETFIE	-	Return from interrupt	2	00	0000	0000	1001		
RETLW	k	Return with literal in W	2	11		kkkk			
RETURN	-	Return from Subroutine	2	00	0000	0000	1000		
SLEEP	-	Go into Standby mode	1	00	0000	0110	0011	TO,PD	
SUBLW	k	Subtract W from literal	1	11	110x	kkkk	kkkk	C,DC,Z	
XORLW	k	Exclusive OR literal with W	1	11	1010	kkkk	kkkk	Z	
Note 1:		I/O register is modified as a function of itse							
	on the nin	s themselves. For example, if the data late	h is '1' for a pip of	onfigur	nd on inr	out and	ia driva	a low by on	ovtorno

Note 1: When an I/O register is modified as a function of itself (e.g., MOVF GPIO, 1), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

2: If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 module.

3: If Program Counter (PC) is modified, or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

Note: Additional information on the mid-range instruction set is available in the *PIC Mid-Range MCU Family Reference Manual* (DS33023).

SWAPF	Swap Nibbles in f
Syntax:	[label] SWAPF f,d
Operands:	$\begin{array}{l} 0\leq f\leq 127\\ d\in [0,1] \end{array}$
Operation:	$(f<3:0>) \rightarrow (destination<7:4>), (f<7:4>) \rightarrow (destination<3:0>)$
Status Affected:	None
Description:	The upper and lower nibbles of register 'f' are exchanged. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed in register 'f'.

XORWF	Exclusive OR W with f					
Syntax:	[<i>label</i>] XORWF f,d					
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]					
Operation:	(W) .XOR. (f) \rightarrow (destination)					
Status Affected:	Z					
Description:	Exclusive OR the contents of the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.					

XORLW	Exclusive OR Literal with W					
Syntax:	[<i>label</i>] XORLW k					
Operands:	$0 \leq k \leq 255$					
Operation:	(W) .XOR. $k \rightarrow (W)$					
Status Affected:	Z					
Description:	The contents of the W register are XOR'ed with the eight-bit literal 'k'. The result is placed in the W register.					

12.20 PICDEM 18R PIC18C601/801 Demonstration Board

The PICDEM 18R demonstration board serves to assist development of the PIC18C601/801 family of Microchip microcontrollers. It provides hardware implementation of both 8-bit Multiplexed/De-multiplexed and 16-bit Memory modes. The board includes 2 Mb external FLASH memory and 128 Kb SRAM memory, as well as serial EEPROM, allowing access to the wide range of memory types supported by the PIC18C601/801.

12.21 PICDEM LIN PIC16C43X Demonstration Board

The powerful LIN hardware and software kit includes a series of boards and three PIC microcontrollers. The small footprint PIC16C432 and PIC16C433 are used as slaves in the LIN communication and feature onboard LIN transceivers. A PIC16F874 FLASH microcontroller serves as the master. All three microcontrollers are programmed with firmware to provide LIN bus communication.

12.22 PICkit[™] 1 FLASH Starter Kit

A complete "development system in a box", the PICkit FLASH Starter Kit includes a convenient multi-section board for programming, evaluation, and development of 8/14-pin FLASH PIC[®] microcontrollers. Powered via USB, the board operates under a simple Windows GUI. The PICkit 1 Starter Kit includes the user's guide (on CD ROM), PICkit 1 tutorial software and code for various applications. Also included are MPLAB[®] IDE (Integrated Development Environment) software, software and hardware "Tips 'n Tricks for 8-pin FLASH PIC[®] Microcontrollers" Handbook and a USB Interface Cable. Supports all current 8/14-pin FLASH PIC microcontrollers, as well as many future planned devices.

12.23 PICDEM USB PIC16C7X5 Demonstration Board

The PICDEM USB Demonstration Board shows off the capabilities of the PIC16C745 and PIC16C765 USB microcontrollers. This board provides the basis for future USB products.

12.24 Evaluation and Programming Tools

In addition to the PICDEM series of circuits, Microchip has a line of evaluation kits and demonstration software for these products.

- KEELOQ evaluation and programming tools for Microchip's HCS Secure Data Products
- CAN developers kit for automotive network applications
- Analog design boards and filter design software
- PowerSmart battery charging evaluation/ calibration kits
- IrDA[®] development kit
- microID development and rfLab[™] development software
- SEEVAL[®] designer kit for memory evaluation and endurance calculations
- PICDEM MSC demo boards for Switching mode power supply, high power IR driver, delta sigma ADC, and flow rate sensor

Check the Microchip web page and the latest Product Line Card for the complete list of demonstration and evaluation kits.

			ard Ope ting tem			•	ss otherwise stated) +85°C for industrial
Param	Device Characteristics	Min	Тур†	Max	Units		Conditions
No.			-761			Vdd	Note
D010	Supply Current (IDD) ⁽³⁾	—	9	16	μΑ	2.0	Fosc = 32 kHz
			18	28	μΑ	3.0	LP Oscillator Mode
			34	54	μΑ	5.0	
D011		—	110	150	μΑ	2.0	Fosc = 1 MHz
		—	190	280	μΑ	3.0	XT Oscillator Mode
		_	330	450	μΑ	5.0	
D012		—	220	280	μΑ	2.0	Fosc = 4 MHz
		—	370	650	μΑ	3.0	XT Oscillator Mode
		—	0.6	1.4	mA	5.0	
D013		—	70	110	μΑ	2.0	Fosc = 1 MHz
		—	140	250	μΑ	3.0	EC Oscillator Mode
		—	260	390	μΑ	5.0	
D014		—	180	250	μΑ	2.0	Fosc = 4 MHz
		—	320	470	μΑ	3.0	EC Oscillator Mode
		—	580	850	μΑ	5.0	
D015		—	340	450	μΑ	2.0	Fosc = 4 MHz
			500	700	μΑ	3.0	INTOSC Mode
		_	0.8	1.1	mA	5.0	
D016		—	180	250	μΑ	2.0	Fosc = 4 MHz
		_	320	450	μΑ	3.0 EXTR	EXTRC Mode
		_	580	800	μA	5.0	
D017		_	2.1	2.95	mA	4.5	Fosc = 20 MHz
			2.4	3.0	mA	5.0	HS Oscillator Mode

13.2 DC Characteristics: rfPIC12F675-I (Industrial)

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The test conditions for all IDD measurements in Active Operation mode are: OSC1 = external square wave, from rail to rail; all I/O pins tri-stated, pulled to VDD; MCLR = VDD; WDT disabled.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

3: Total device current is the sum of IDD from VDD and IDDRF from VDDRF.

13.9 DC Characteristics: rfPIC12F675-I (Industrial), rfPIC12F675-E (Extended)

	ARACI	ERISTICS	Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for extended					
Param No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions	
		Input Low Voltage						
	VIL	I/O ports						
D030		with TTL buffer	Vss	—	0.8	V	$4.5V \le VDD \le 5.5V$	
D030A			Vss	—	0.15 Vdd	V	Otherwise	
D031		with Schmitt Trigger buffer	Vss	—	0.2 Vdd	V	Entire range	
D032		MCLR, OSC1 (RC mode)	Vss	—	0.2 Vdd	V		
D033		OSC1 (XT and LP modes)	Vss	—	0.3	V	(Note 1)	
D033A		OSC1 (HS mode)	Vss	—	0.3 Vdd	V	(Note 1)	
D034		DATAASK, DATAFSK, RFEN	Vss	—	0.3 Vddrf	V		
		Input High Voltage						
	Vih	I/O ports		—				
D040		with TTL buffer	2.0	—	Vdd	V	$4.5V \le VDD \le 5.5V$	
D040A			(0.25 VDD+0.8)	—	Vdd	V	otherwise	
D041		with Schmitt Trigger buffer	0.8 Vdd	—	Vdd		entire range	
D042		MCLR	0.8 Vdd	—	Vdd	V		
D043		OSC1 (XT and LP modes)	1.6	—	Vdd	V	(Note 1)	
D043A		OSC1 (HS mode)	0.7 Vdd	—	Vdd	V	(Note 1)	
D043B		OSC1 (RC mode)	0.9 Vdd	—	Vdd	V		
D044		DATAASK, DATAFSK, RFEN	0.7 Vdd	—	VDDRF	V		
D070	IPUR	GPIO Weak Pull-up Current	50*	250	400*	μΑ	VDD = 5.0V, VPIN = VSS	
D071		DATAASK Weak Pull-up	0.1*	1.5	12*	μΑ	VDDRF = RFEN = 3.0V	
D072		RFENIN Weak Pull-down	0.2*	2.0	20*	μΑ	VDDRF = RFEN = 3.0V	
		Input Leakage Current ⁽³⁾						
D060	lı∟	GPIO ports, DATAASK, DATAFSK, RFEN	—	± 0.1	± 1	μA	$Vss \le VPIN \le VDD,$ Pin at hi-impedance	
D060A		Analog inputs	_	± 0.1	± 1	μA	$VSS \leq VPIN \leq VDD$	
D060B		VREF	_	± 0.1	± 1	μA	$VSS \leq VPIN \leq VDD$	
D061		MCLR ⁽²⁾	_	± 0.1	± 5	μA	$VSS \leq VPIN \leq VDD$	
D063		OSC1	—	± 0.1	± 5	μΑ	Vss \leq VPIN \leq VDD, XT, HS and LP osc configuration	
		Output Low Voltage						
D080	Vol	I/O ports	—	—	0.6	V	IOL = 8.5 mA, VDD = 4.5V (Ind.)	
D083		OSC2/CLKOUT (RC mode)	_	_	0.6	V	IOL = 1.6 mA, VDD = 4.5V (Ind.) IOL = 1.2 mA, VDD = 4.5V (Ext.)	
		Output High Voltage						
D090	Vон	I/O ports	Vdd - 0.7	—	—	V	ІОН = -3.0 mA, VDD = 4.5V (Ind.)	
D092		OSC2/CLKOUT (RC mode)	Vdd - 0.7	_	_	V	ІОН = -1.3 mA, VDD = 4.5V (Ind.) ІОН = -1.0 mA, VDD = 4.5V (Ext.)	

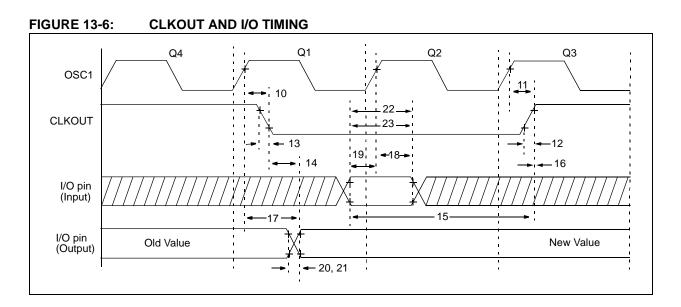
* These parameters are characterized but not tested.

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended to use an external clock in RC mode.

2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.



Param No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
10	TosH2ckL	OSC1↑ to CLK- OUT↓	—	75	200	ns	(Note 1)
11	TosH2ckH	OSC1↑ to CLK- OUT↑	—	75	200	ns	(Note 1)
12	TckR	CLKOUT rise time	—	35	100	ns	(Note 1)
13	TckF	CLKOUT fall time	—	35	100	ns	(Note 1)
14	TckL2ioV	CLKOUT↓ to Port out valid	—	—	20	ns	(Note 1)
15	TioV2ckH	Port in valid before CLKOUT↑	Tosc + 200 ns	—	—	ns	(Note 1)
16	TckH2iol	Port in hold after CLKOUT [↑]	0	—	_	ns	(Note 1)
17	TosH2ioV	OSC1 [↑] (Q1 cycle) to Port out valid	—	50	150 *	ns	
			—	—	300	ns	
18	TosH2iol	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	100	—	—	ns	
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	0	—	—	ns	
20	TioR	Port output rise time	—	10	40	ns	
21	TioF	Port output fall time	—	10	40	ns	
22	Tinp	INT pin high or low time	25	—	_	ns	
23	Trbp	GPIO change INT high or low time	Тсү	—	_	ns	

* These parameters are characterized but not tested.

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated.

Note 1: Measurements are taken in RC mode where CLKOUT output is 4xTosc.

TABLE 13-11: rfPIC12F675K RF TRANSMITTER SPECIFICATIONS (315 MHz)

RF Trans	mitter Specifications	TA = +23° VDDRF = 3	C (unless 3.0V (unles	g Conditions otherwise sta ss otherwise s ss otherwise	ted) stated)	
Sym	Characteristics	Min	Тур	Max	Units	Comments
Fc	VCO Frequency	290	—	350	MHz	32 x Frfxtal
FXTAL	Crystal Frequency	9.06	—	10.94	MHz	Fundamental mode
Fref	Reference Frequency	2.265	—	2.735	MHz	FRFXTAL / 4
CL	Load Capacitance	10	—	15	pF	
Со	Static Capacitance	—	—	7	pF	
Rs	Series Resistance		—	70	Ω	
ASPUR	Spurious response		—	-10	dB	For FSK operation
ΔF VDD	Frequency Stability vs VDDRF		—	±3	ppm	
ΔFta	Frequency Stability vs Temp	—	_	±10	ppm	Crystal temp constant
ΔF	FSK Deviation	±5	—	±80	kHz	Depends on crystal parameters
Rfsk	FSK Data Rate	—	—	40	Kbit/s	NRZ
Rask	ASK Data Rate	—	—	40	Kbit/s	NRZ
Τον	RFEN High to Transmit	—	1.2	1.5	ms	
Poff	RF Output Power in Step 0	—	—	-70	dBm	RFEN=1
P1	RF Output Power in Step 1	—	-12	—	dBm	RFEN=1
P2	RF Output Power in Step 2	—	-4	—	dBm	RFEN=1
P3	RF Output Power in Step 3	—	2	—	dBm	RFEN=1
P4	RF Output Power in Step 4	—	4	—	dBm	RFEN=1, VDDRF=2.0V
			7.5	—	dBm	RFEN=1, VDDRF=3.0V
			8.5	9.5	dBm	RFEN=1, VDDRF=4.0V
		_	9.0	10.5	dBm	RFEN=1, VDDRF=5.0V
L(FM)	Phase Noise	—	-86	—	dBc/Hz	200 kHz offset
PSPUR	Spurious Emissions	-	_	-54	dBm	47 MHz < f < 74 MHz 87.5 MHz < f < 118 MHz 174 MHz < f < 230 MHz 470 MHz < f < 862 MHz RBW = 100 kHz
		—	—	-36	dBm	f < 1 GHz RBW = 100 kHz
		—	—	-30	dBm	f > 1 GHz RBW = 1 MHz

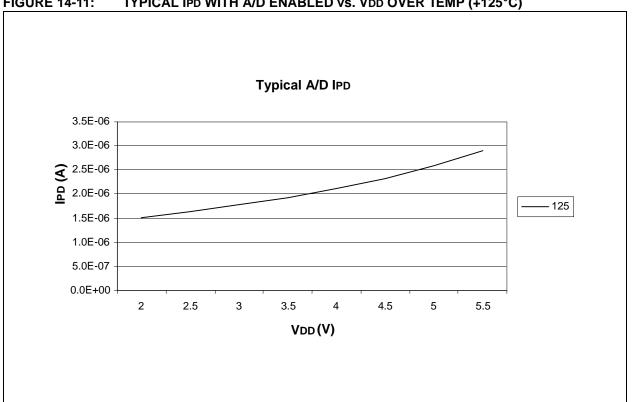
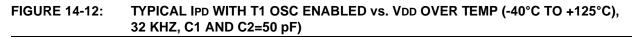
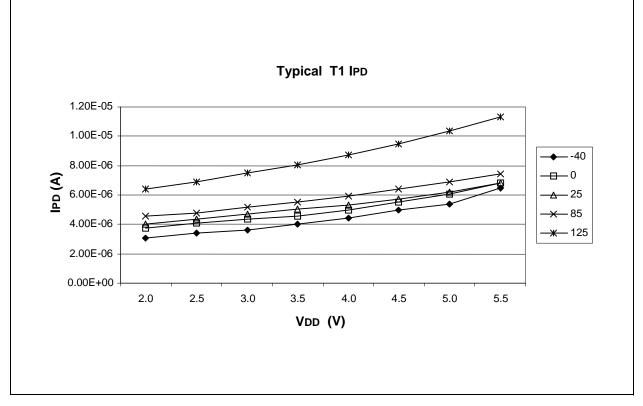


FIGURE 14-11: TYPICAL IPD WITH A/D ENABLED vs. VDD OVER TEMP (+125°C)





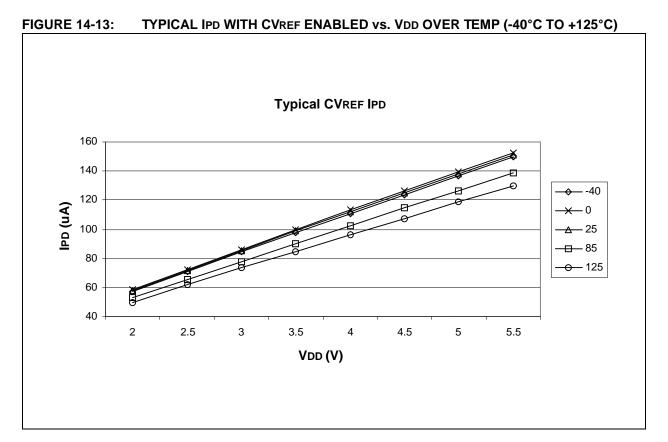
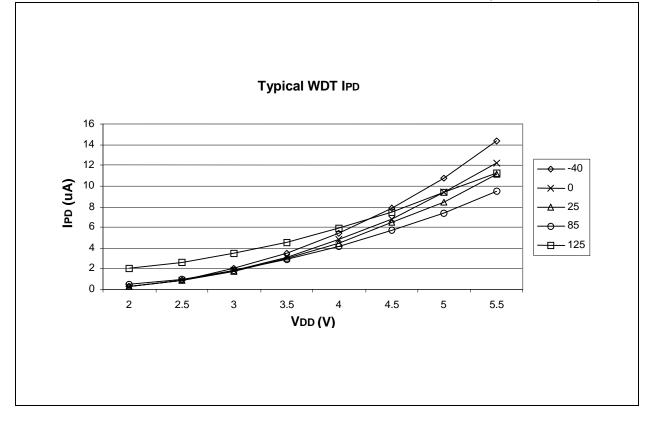
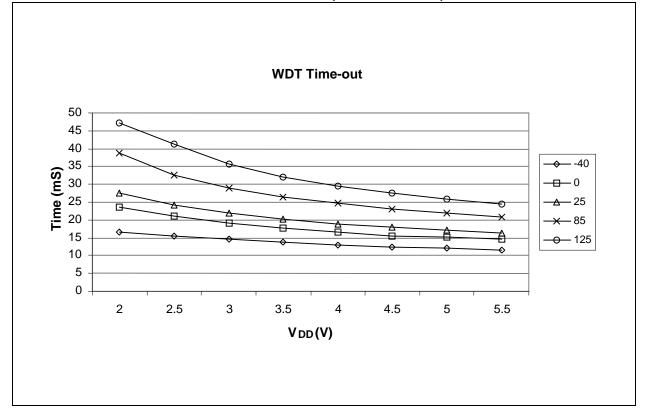


FIGURE 14-14: TYPICAL IPD WITH WDT ENABLED vs. VDD OVER TEMP (-40°C TO +125°C)







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