Infineon Technologies - SAF-TC1164-128F80HL AB Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	TriCore™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	ASC, CANbus, MLI, MSC, SSC
Peripherals	DMA, POR, WDT
Number of I/O	81
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	76K x 8
Voltage - Supply (Vcc/Vdd)	1.42V ~ 1.58V
Data Converters	A/D 36x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	PG-LQFP-176-2
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/saf-tc1164-128f80hl-ab

2 General Device Information

Chapter 2 provides the general information for the TC1163/TC1164.

2.1 Block Diagram

Figure 2-1 shows the TC1163/TC1164 block diagram.

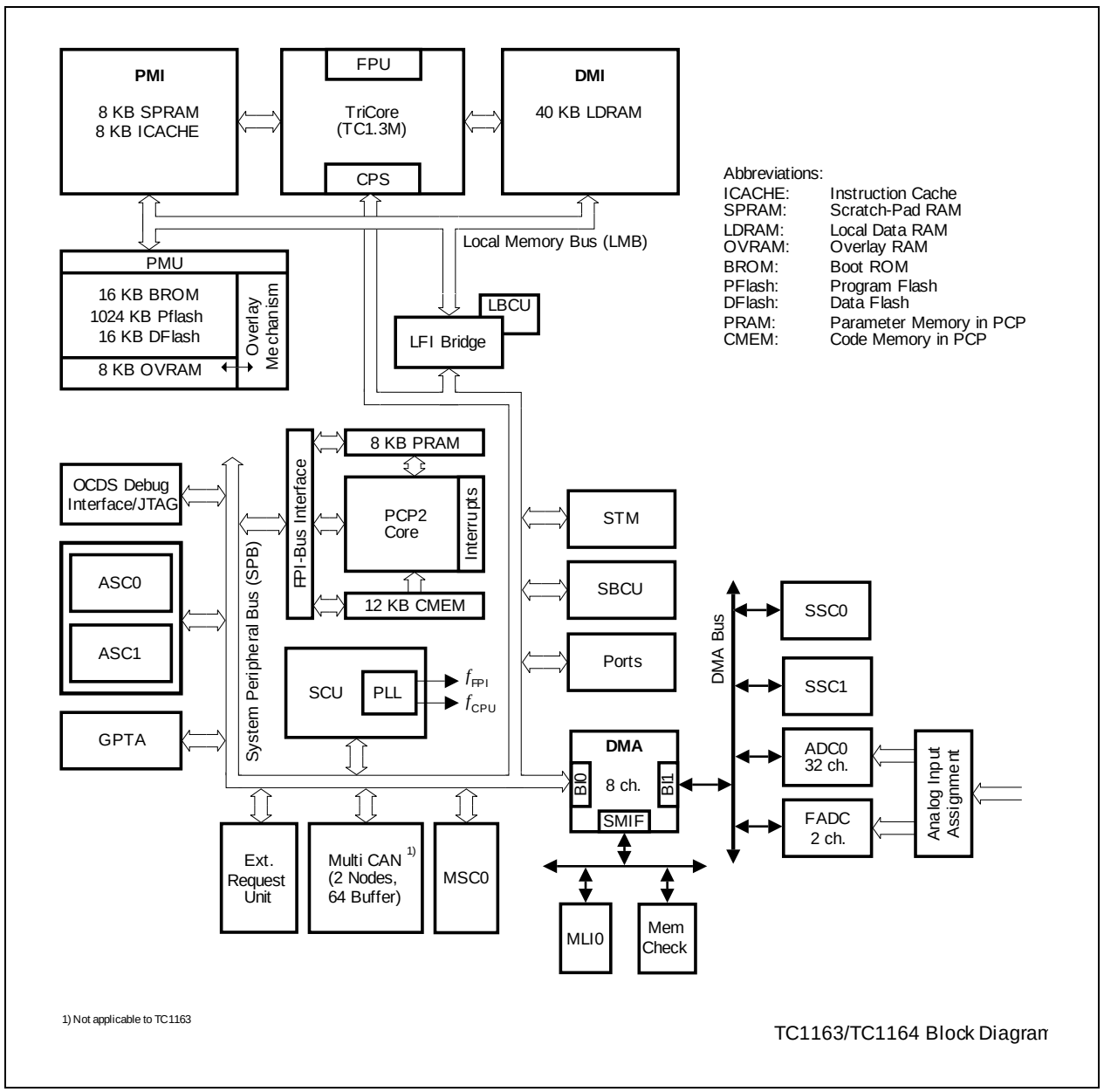

Figure 2-1 TC1163/TC1164 Block Diagram

Table 2-2 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Driver Class	Power Supply	Functions
MSC0 Outputs					
			C	V_{DDP}	**LVDS MSC Clock and Data Outputs**[4]
FCLP0A	157	O			MSC0 Differential Driver Clock Output Positive A
FCLN0	156	O			MSC0 Differential Driver Clock Output Negative
SOP0A	159	O			MSC0 Differential Driver Serial Data Output Positive A
SON0	158	O			MSC0 Differential Driver Serial Data Output Negative

Table 2-2 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Driver Class	Power Supply	Functions
Analog Inputs					
AN[35:0]		I	D	–	**Analog Input Port** The Analog Input Port provides altogether 36 analog input lines to ADC0 and FADC. AN[31:0]: ADC0 analog inputs [31:0] AN[35:32]: FADC analog differential inputs
AN0	67				Analog input 0
AN1	66				Analog input 1
AN2	65				Analog input 2
AN3	64				Analog input 3
AN4	63				Analog input 4
AN5	62				Analog input 5
AN6	61				Analog input 6
AN7	36				Analog input 7
AN8	60				Analog input 8
AN9	59				Analog input 9
AN10	58				Analog input 10
AN11	57				Analog input 11
AN12	56				Analog input 12
AN13	55				Analog input 13
AN14	50				Analog input 14
AN15	49				Analog input 15
AN16	48				Analog input 16
AN17	47				Analog input 17
AN18	46				Analog input 18
AN19	45				Analog input 19
AN20	44				Analog input 20
AN21	43				Analog input 21
AN22	42				Analog input 22
AN23	41				Analog input 23
AN24	40				Analog input 24
AN25	39				Analog input 25
AN26	38				Analog input 26
AN27	37				Analog input 27
AN28	35				Analog input 28
AN29	34				Analog input 29
AN30	33				Analog input 30

Table 2-2 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Driver Class	Power Supply	Functions
N.C.	21, 89	–	–	–	**Not Connected** These pins are reserved for future extension and must not be connected externally.
Power Supplies					
V_{DDM}	54	–	–	–	**ADC Analog Part Power Supply (3.3 V)**
V_{SSM}	53	–	–	–	**ADC Analog Part Ground for V_{DDM}**
V_{DDMF}	24	–	–	–	**FADC Analog Part Power Supply (3.3 V)**
V_{SSMF}	25	–	–	–	**FADC Analog Part Ground for V_{DDMF}**
V_{DDAF}	23	–	–	–	**FADC Analog Part Logic Power Supply (1.5 V)**
V_{SSAF}	22	–	–	–	**FADC Analog Part Logic Ground for V_{DDAF}**
V_{AREF0}	52	–	–	–	**ADC Reference Voltage**
V_{AGND0}	51	–	–	–	**ADC Reference Ground**
V_{FAREF}	26	–	–	–	**FADC Reference Voltage**
V_{FAGND}	27	–	–	–	**FADC Reference Ground**
V_{DDOSC}	105	–	–	–	**Main Oscillator and PLL Power Supply (1.5 V)**
V_{DDOSC3}	106	–	–	–	**Main Oscillator Power Supply (3.3 V)**
V_{SSOSC}	104	–	–	–	**Main Oscillator and PLL Ground**
V_{DDFL3}	141	–	–	–	**Power Supply for Flash (3.3 V)**
V_{DD}	10, 68, 84, 99, 123, 153, 170	–	–	–	**Core Power Supply (1.5 V)**

Table 3-6 PCP2 Instruction Set Overview

Instruction Group	Description
DMA primitives	Efficient DMA channel implementation
Load/Store	Transfer data between PRAM or FPI memory and the general purpose registers, as well as move or exchange values between registers
Arithmetic	Add, subtract, compare and complement
Divide/Multiply	Divide and multiply
Logical	And, Or, Exclusive Or, Negate
Shift	Shift right or left, rotate right or left, prioritize
Bit Manipulation	Set, clear, insert and test bits
Flow Control	Jump conditionally, jump long, exit
Miscellaneous	No operation, Debug

3.9 High-Speed Synchronous Serial Interfaces (SSC0 and SSC1)

Figure 3-5 shows a global view of the functional blocks and interfaces of the two high-speed Synchronous Serial Interfaces, SSC0 and SSC1.

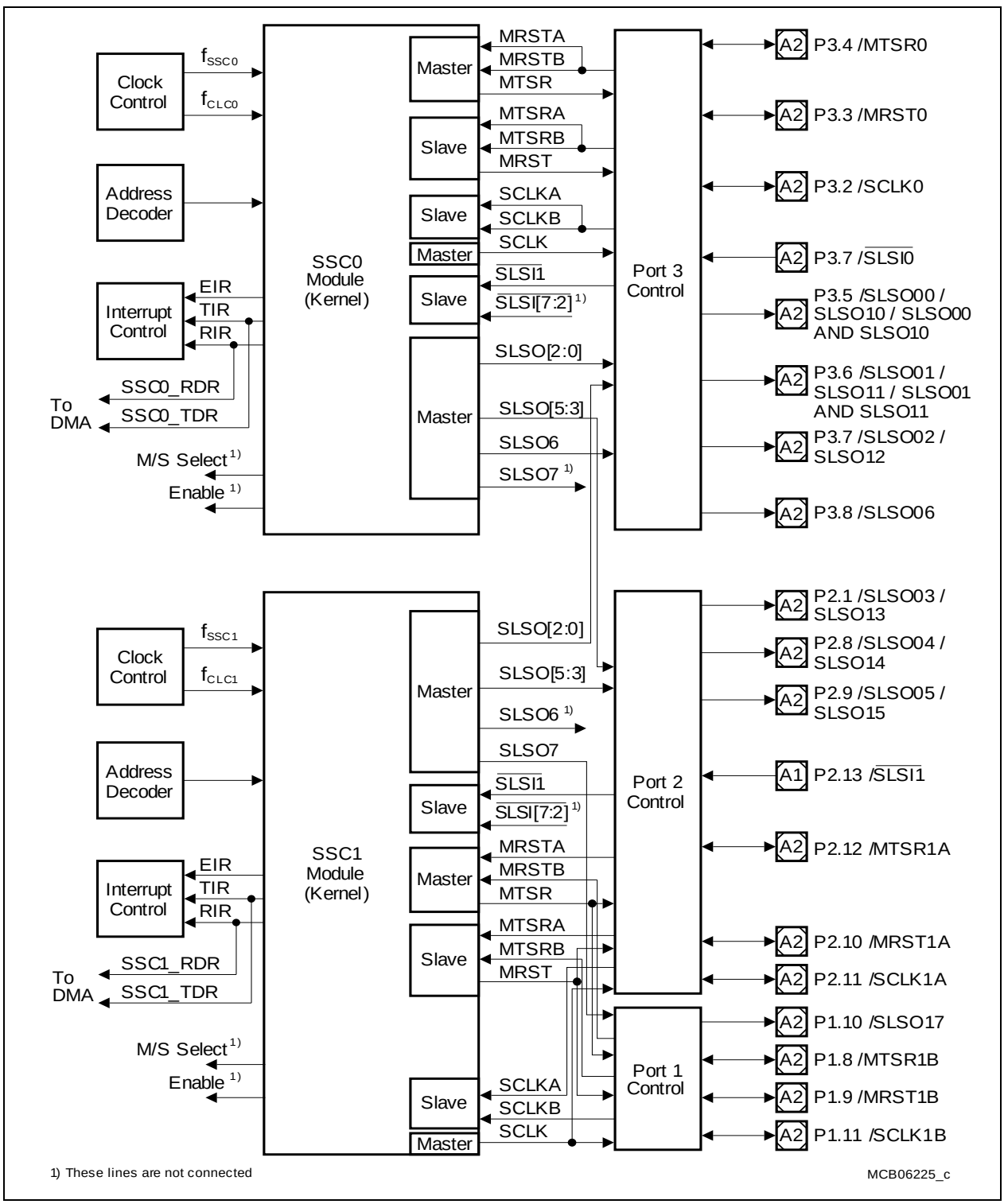

Figure 3-5 Block Diagram of the SSC Interfaces

3.13 General Purpose Timer Array

The GPTA provides a set of timer, compare, and capture functionalities that can be flexibly combined to form signal measurement and signal generation units. They are optimized for tasks typical of electrical motor control applications, but can also be used to generate simple and complex signal waveforms needed in other industrial applications.

The TC1163/TC1164 contains one General Purpose Timer Array (GPTA0). **Figure 3-10** shows a global view of the GPTA module.

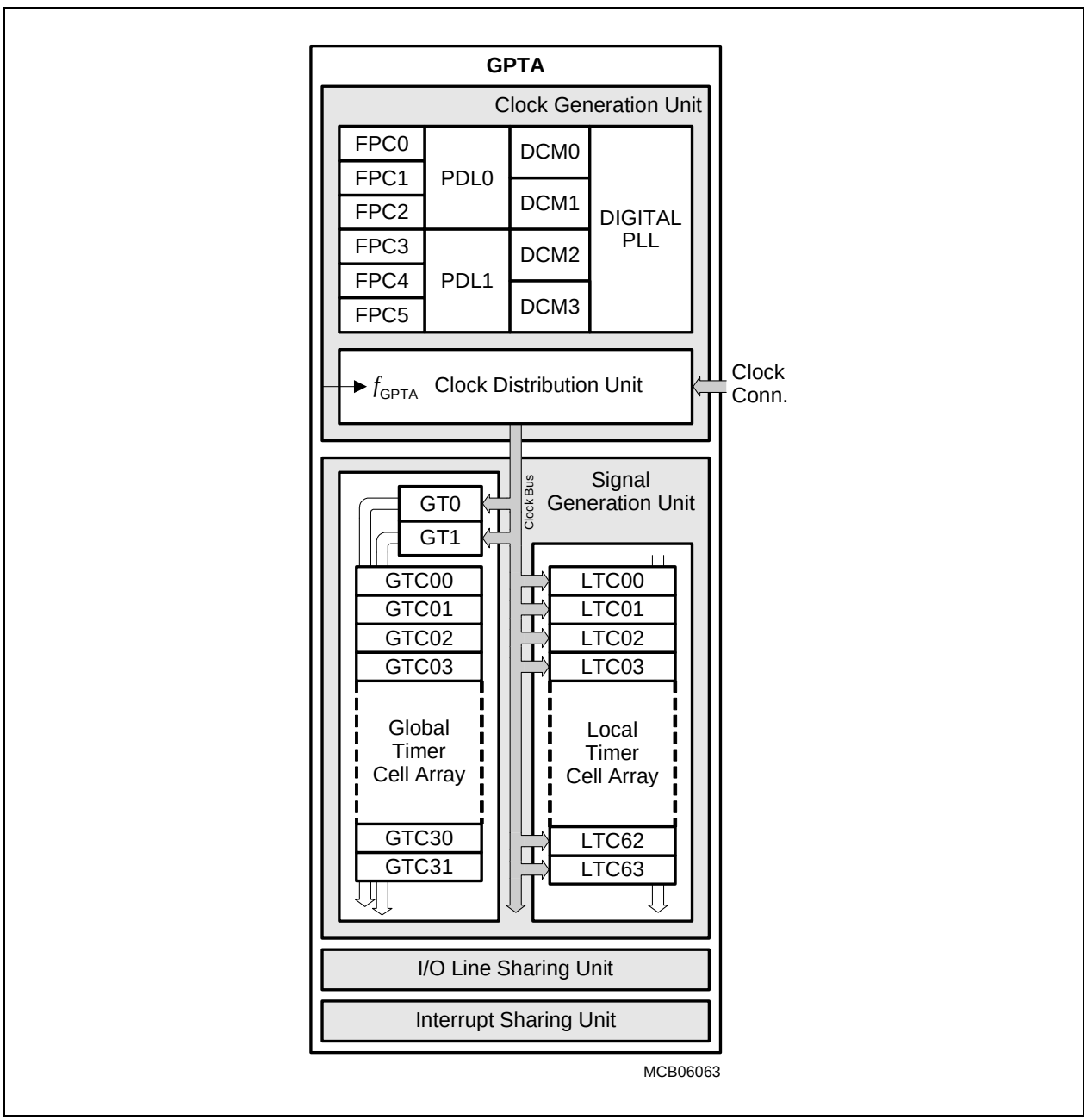

Figure 3-10 Block Diagram of the GPTA Module

- Duty Cycle Measurement (DCM)
  - Four independent units
  - 0 - 100% margin and time-out handling
  - f_{GPTA} maximum resolution
  - f_{GPTA}/2 maximum input signal frequency
- Digital Phase Locked Loop (PLL)
  - One unit
  - Arbitrary multiplication factor between 1 and 65535
  - f_{GPTA} maximum resolution
  - f_{GPTA}/2 maximum input signal frequency
- Clock Distribution Unit (CDU)
  - One unit
  - Provides nine clock output signals:
    f_{GPTA}, divided f_{GPTA} clocks, FPC1/FPC4 outputs, DCM clock, LTC prescaler clock

Signal Generation Unit

- Global Timers (GT)
  - Two independent units
  - Two operating modes (Free-Running Timer and Reload Timer)
  - 24-bit data width
  - f_{GPTA} maximum resolution
  - f_{GPTA}/2 maximum input signal frequency
- Global Timer Cell (GTC)
  - 32 units related to the Global Timers
  - Two operating modes (Capture, Compare and Capture after Compare)
  - 24-bit data width
  - f_{GPTA} maximum resolution
  - f_{GPTA}/2 maximum input signal frequency
- Local Timer Cell (LTC)
  - 64 independent units
  - Three basic operating modes (Timer, Capture and Compare) for 63 units
  - Special compare modes for one unit
  - 16-bit data width
  - f_{GPTA} maximum resolution
  - f_{GPTA}/2 maximum input signal frequency

Interrupt Control Unit

- 111 interrupt sources, generating up to 38 service requests

OCDS Level 1 Debug Support

The OCDS Level 1 debug support is mainly assigned for real-time software debugging purposes which have a demand for low-cost standard debugger hardware.

The OCDS Level 1 is based on a JTAG interface that is used by the external debug hardware to communicate with the system. The on-chip Cerberus module controls the interactions between the JTAG interface and the on-chip modules. The external debug hardware may become master of the internal buses, and read or write the on-chip register/memory resources. The Cerberus also makes it possible to define breakpoint and trigger conditions as well as to control user program execution (run/stop, break, single-step).

OCDS Level 2 Debug Support

The OCDS Level 2 debug support makes it possible to implement program tracing capabilities for enhanced debuggers by extending the OCDS Level 1 debug functionality with an additional 16-bit wide trace output port with trace clock. With the trace extension, the following four trace capabilities are provided (only one of the four trace capabilities can be selected at a time):

- Trace of the CPU program flow
- Trace of the PCP2 program flow
- Trace of the DMA Controller transaction requests
- Trace of the DMA Controller Move Engine status information

4.1.2 Pad Driver and Pad Classes Summary

This section gives an overview on the different pad driver classes and its basic characteristics. More details (mainly DC parameters) are defined in **Section 4.2.1**.

Table 4-1 Pad Driver and Pad Classes Overview

Class	Power Supply	Type	Sub Class	Speed Grade	Load	Leakage[1)]	Termination
A	3.3V	LVTTL I/O, LVTTL outputs	**A1** (e.g. GPIO)	6 MHz	100 pF	500 nA	No
			A2 (e.g. serial I/Os)	40 MHz	50 pF	6 µA	Series termination recommended
			A3 (e.g. BRKIN, BRKOUT)	80 MHz/	50 pF	6 µA	Series termination recommended (for f > 25 MHz)
			A4 (e.g. Trace Clock)	80 MHz	25 pF	6 µA	Series termination recommended
C	3.3V	LVDS	–	50 MHz		–	Parallel termination[2)], 100Ω ± 10%
D	–	Analog inputs, reference voltage inputs					

1) Values are for T_{Jmax} = 125 °C.

2) In applications where the LVDS pins are not used (disabled), these pins must be either left unconnected, or properly terminated with the differential parallel termination of 100Ω ± 10%.

Table 4-4 Pin Groups for Overload/Short-Circuit Current Sum Parameter

Group	Pins
1	TRCLK, P5.[7:0], P0.[7:6], P0.[15:14]
2	P0.[13:12], P0.[5:4], P2.[13:8], SOP0A, SON0, FCLP0A, FCLN0
3	P0.[11:8], P0.[3:0], P3.[13:11]
4	P3[10:0], P3.[15:14]
5	$\overline{\text{HDRST}}$, $\overline{\text{PORST}}$, $\overline{\text{NMI}}$, $\overline{\text{TESTMODE}}$, $\overline{\text{BRKIN}}$, $\overline{\text{BRKOUT}}$, BYPASS, TCK, $\overline{\text{TRST}}$, TDO, TMS, TDI, P1.[7:4]
6	P1.[3:0], P1.[11:8], P4.[3:0]
7	P2.[7:0], P1.[14:12]
8	P5.[15:8]

4.2 DC Parameters

The electrical characteristics of the DC Parameters are detailed in this section.

4.2.1 Input/Output Pins

Table 4-5 provides the characteristics of the input/output pins of the TC1163/TC1164.

Table 4-5 Input/Output DC-Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
General Parameters						
Pull-up current[1)]	$\|I_{PUH}\|$	CC	10	100	µA	$V_{IN} < V_{IHAmin}$; class A1/A2/Input pads.
			20	200	µA	$V_{IN} < V_{IHAmin}$; class A3/A4 pads.
Pull-down current[1)]	$\|I_{PDL}\|$	CC	10	150	µA	$V_{IN} > V_{ILAmax}$; class A1/A2/Input pads.
			20	200	µA	$V_{IN} > V_{ILAmax}$; class A3/A4 pads.
Pin capacitance[1)] (Digital I/O)	C_{IO}	CC	–	10	pF	f = 1 MHz T_A = 25 °C
Input only Pads (V_{DDP} = 3.13 to 3.47 V = 3.3V ±5%)						
Input low voltage class A1/A2 pins	V_{ILA}	SR	-0.3	0.34 × V_{DDP}	V	–
Input high voltage class A1/A2 pins	V_{IHA}	SR	0.64 × V_{DDP}	V_{DDP}+ 0.3 or max. 3.6	V	Whatever is lower
Ratio V_{IL}/V_{IH}		CC	0.53	–	–	–
Input low voltage class A3 pins	V_{ILA3}	SR	–	0.8	V	–
Input high voltage class A3 pins	V_{IHA3}	SR	2.0	–	V	–
Input hysteresis	HYSA	CC	0.1 × V_{DDP}	–	V	[2)5)]
Input leakage current	I_{OZI}	CC	–	±3000 ±6000	nA	$(V_{DDP}/2)-1) < V_{IN} < ((V_{DDP}/2)+1)$ otherwise[3)]

4.2.2 Analog to Digital Converter (ADC0)

Table 4-6 provides the characteristics of the ADC module in the TC1163/TC1164.

Table 4-6 ADC Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Test Conditions / Remarks
			Min.	Typ.	Max.		
Analog supply voltage	V_{DDM}	SR	3.13	3.3	3.47[1)]	V	–
	V_{DD}	SR	1.42	1.5	1.58[2)]	V	Power supply for ADC digital part, internal supply
Analog ground voltage	V_{SSM}	SR	-0.1	–	0.1	V	–
Analog reference voltage [17)]	V_{AREFx}	SR	V_{AGNDx}+ 1V	V_{DDM}	V_{DDM}+ 0.05 [1)3)4)]	V	–
Analog reference ground [17)]	V_{AGNDx}	SR	V_{SSMx} - 0.05V	0	V_{AREF} - 1 V	V	–
Analog reference voltage range[5)17)]	V_{AREFx}- V_{AGNDx}	SR	V_{DDM}/2		V_{DDM} + 0.05		
Analog input voltage range	V_{AIN}	SR	V_{AGNDx}	–	V_{AREFx}	V	–
V_{DDM} supply current	I_{DDM}	SR		2.5	4	mA rms	[6)]
Power-up calibration time	t_{PUC}	CC	–	–	3840	f_{ADC} CLK	–
Internal ADC clocks	f_{BC}	CC	2	–	40	MHz	$f_{BC} = f_{ANA} \times 4$
	f_{ANA}	CC	0.5	–	10	MHz	$f_{ANA} = f_{BC} / 4$
Sample time	t_S	CC	4 × (CHCONn.STC + 2) × t_{BC}			µs	–
			8 × t_{BC}	–	–	µs	

4.3.2 Output Rise/Fall Times

Table 4-11 provides the characteristics of the output rise/fall times in the TC1163/TC1164.

Table 4-11 Output Rise/Fall Times (Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Conditions
		Min.	Max.		
Class A1 Pads					
Rise/fall times[1)] Class A1 pads	t_{RA1}, t_{FA1}		50 140 18000 150 550 65000	ns	Regular (medium) driver, 50 pF Regular (medium) driver, 150 pF Regular (medium) driver, 20 nF Weak driver, 20 pF Weak driver, 150 pF Weak driver, 20 000 pF
Class A2 Pads					
Rise/fall times [1)] Class A2 pads	t_{FA2}, t_{FA2}		3.3 6 5.5 16 50 140 18000 150 550 65000	ns	Strong driver, sharp edge, 50 pF Strong driver, sharp edge, 100pF Strong driver, med. edge, 50 pF Strong driver, soft edge, 50 pF Medium driver, 50 pF Medium driver, 150 pF Medium driver, 20 000 pF Weak driver, 20 pF Weak driver, 150 pF Weak driver, 20 000 pF
Class A3 Pads					
Rise/fall times [1)] Class A3 pads	t_{FA3}, t_{FA3}		2.5	ns	50 pF
Class A4 Pads					
Rise/fall times [1)] Class A4 pads	t_{FA4}, t_{FA4}		2.0	ns	25 pF
Class C Pads					
Rise/fall times Class C pads	t_{rC}, t_{fC}		2	ns	

1) Not all parameters are subject to production test, but verified by design/characterization and test correlation.

4) Applicable for input pins $\overline{\text{TESTMODE}}$, $\overline{\text{TRST}}$, $\overline{\text{BRKIN}}$, and TXD1A with noise suppression filter of $\overline{\text{PORST}}$ switched-on (BYPASS = 0).
5) The setup/hold values are applicable for Port 0 and Port 4 input pins with noise suppression filter of $\overline{\text{HDRST}}$ switched-on (BYPASS = 0), independently whether $\overline{\text{HDRST}}$ is used as input or output.
6) Not subject to production test, verified by design / characterization.
7) This parameter includes the delay of the analog spike filter in the $\overline{\text{PORST}}$ pad.
8) Not subject to production test, verified by design / characterization.
9) In case of power loss during internal flash write, prevents Flash write to random address.
10) Booting from Flash, the duration of the boot-time is defined between the rising edge of the $\overline{\text{PORST}}$ and the moment when the first user instruction has entered the CPU and its processing starts.
11) Booting from Flash, the duration of the boot time is defined between the following events:
1. Hardware reset: the falling edge of a short $\overline{\text{HDRST}}$ pulse and the moment when the first user instruction has entered the CPU and its processing starts, if the $\overline{\text{HDRST}}$ pulse is shorter than 1024 × T_{SYS}.
If the $\overline{\text{HDRST}}$ pulse is longer than 1024 × T_{SYS}, only the time beyond the 1024 × T_{SYS} should be added to the boot time ($\overline{\text{HDRST}}$ falling edge to first user instruction).
2. Software reset: the moment of starting the software reset and the moment when the first user instruction has entered the CPU and its processing starts

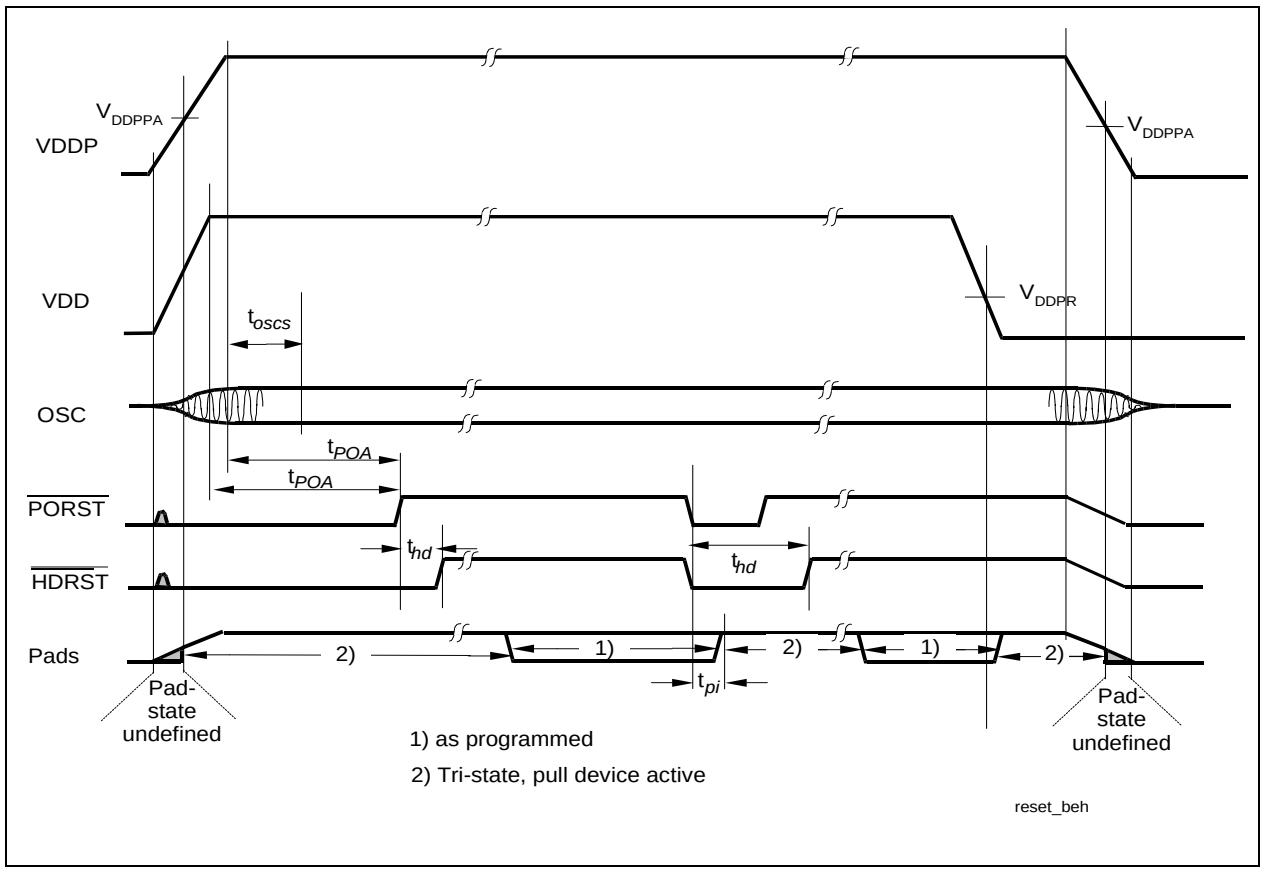

Figure 4-11 Power, Pad and Reset Timing

Note: The frequency of system clock f_{SYS} can be selected to be either f_{CPU} or $f_{CPU}/2$.

With rising number P of clock cycles the maximum jitter increases linearly up to a value of P that is defined by the K-factor of the PLL. Beyond this value of P the maximum accumulated jitter remains at a constant value. Further, a lower CPU clock frequency f_{CPU} results in a higher absolute maximum jitter value.

Figure 4-12 illustrates the jitter curve for several K/ f_{CPU} combinations.

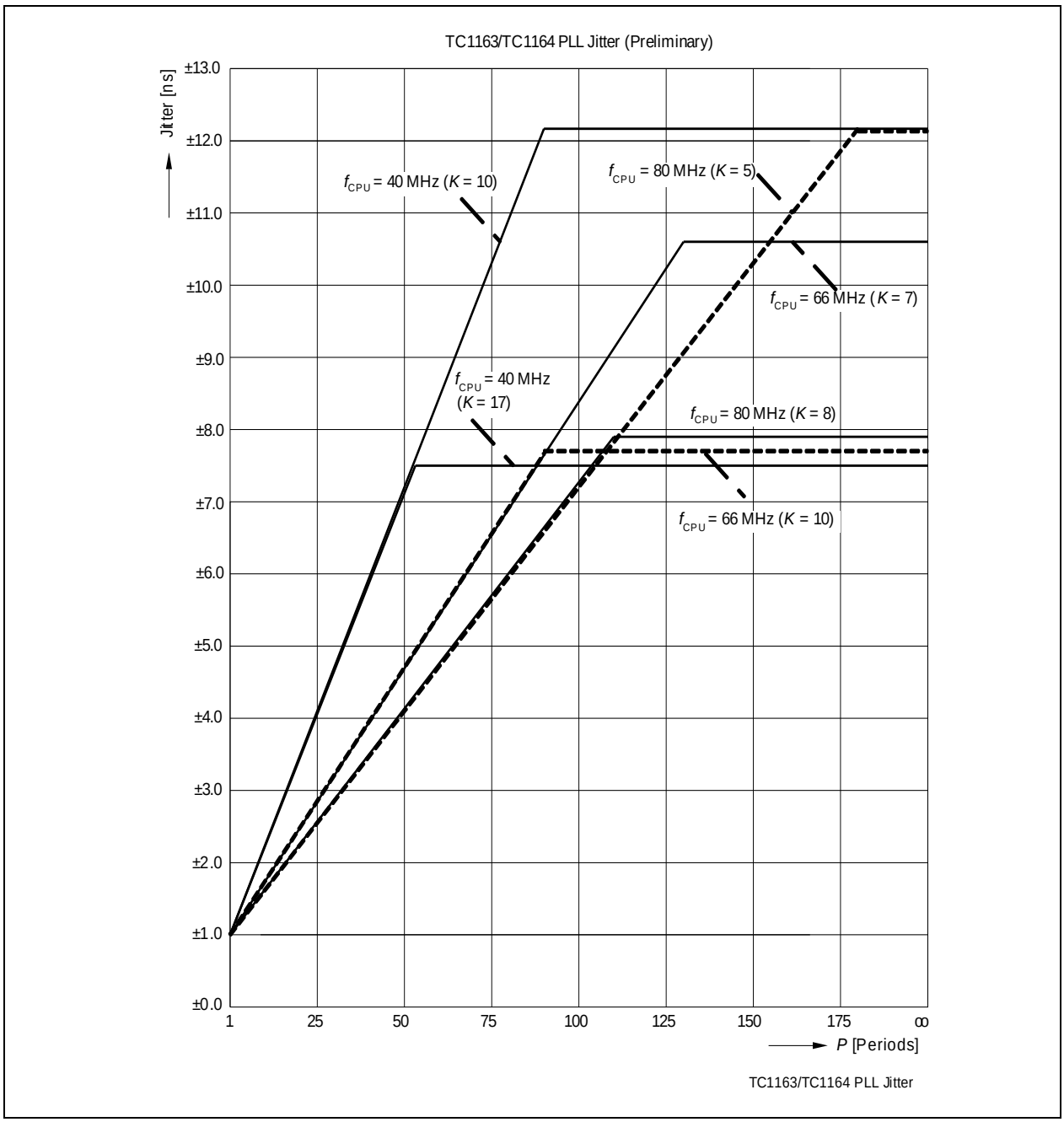

Figure 4-12 Approximated Maximum Accumulated PLL Jitter for Typical CPU Clock Frequencies f_{CPU} (overview)

Table 4-16 JTAG Timing Parameter[1)]

Parameter	Symbol		Limit Values		Unit	Test Conditions / Remarks
			Min.	Max.		
TMS setup to TCK	t_1	SR	6.0	–	ns	–
TMS hold to TCK	t_2	SR	6.0	–	ns	–
TDI setup to TCK	t_1	SR	6.0	–	ns	–
TDI hold to TCK	t_2	SR	6.0	–	ns	–
TDO valid output from TCK[2)]	t_3	CC	–	14.5	ns	C_L = 50 pF[3)4)]
			3.0	–		C_L = 20 pF
TDO high impedance to valid output from TCK[2)]	t_4	CC	–	15.5	ns	C_L = 50 pF[3)4)]
TDO valid output to high impedance from TCK[2)]	t_5	CC	–	14.5	ns	C_L = 50 pF[4)]

1) Not subject to production test, verified by design / characterization.

2) The falling edge on TCK is used to capture the TDO timing.

3) By reducing the load from 50 pF to 20 pF, a reduction of approximately 1.0 ns in timing is expected.

4) By reducing the power supply range from +/-5 % to +5/-2 %, a reduction of approximately 0.5 ns in timing is expected.

5 Package and Reliability

Chapter 5 provides the information of the TC1163/TC1164 package and reliability section.

5.1 Package Parameters (PG-LQFP-176-2)

Table 5-1 provides the thermal characteristics of the package.

Table 5-1 Thermal Characteristics of the Package

Parameter	Symbol		Limit Values		Unit	Notes
			Min.	Max.		
Thermal resistance junction case top[1)]	R_{TJCT}	CC	–	5.4	K/W	–
Thermal resistance junction leads[1)]	R_{TJL}	CC	–	21.5	K/W	–

1) The thermal resistances between the case top and the ambient (R_{TCAT}), the leads and the ambient (R_{TLA}) are to be combined with the thermal resistances between the junction and the case top (R_{TJCT}), the junction and the leads (R_{TJL}) given above, in order to calculate the total thermal resistance between the junction and the ambient (R_{TJA}). The thermal resistances between the case top and the ambient (R_{TCAT}), the leads and the ambient (R_{TLA}) depend on the external system (PCB, case) characteristics, and are under user responsibility. The junction temperature can be calculated using the following equation: $T_J=T_A+R_{TJA} \times P_D$, where the R_{TJA} is the total thermal resistance between the junction and the ambient. This total junction ambient resistance R_{TJA} can be obtained from the upper four partial thermal resistances.

5.4 Quality Declaration

Table 5-3 shows the characteristics of the quality parameters in the TC1163/TC1164.

Table 5-3 Quality Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
ESD susceptibility according to Human Body Model (HBM)	V_{HBM}	–	2000	V	Conforming to EIA/JESD22-A114-B
ESD susceptibility of the LVDS pins	V_{HBM1}	–	500	V	–
ESD susceptibility according to Charged Device Model (CDM) pins	V_{CDM}	–	500	V	Conforming to JESD22-C101-C
Moisture Sensitivity Level (MSL)	–	–	3	–	Conforming to J-STD-020C for 240°C

*Note: Information about soldering can be found on the “package” information page under: **http://www.infineon.com/products**.*

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