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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	H8SX
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, IrDA, SCI, SmartCard, USB
Peripherals	DMA, PWM, WDT
Number of I/O	75
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	40K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	External
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	120-TQFP
Supplier Device Package	120-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df61653n50ftv

(7) Area 6

Area 6 includes internal I/O registers. In external extended mode, area 6 other than on-chip I/O register area is external address space.

When area 6 external address space is accessed, the $\overline{CS6}$ signal can be output.

Either of the basic bus interface, byte control SRAM interface, or address/data multiplexed I/O interface can be selected for area 6 by the MPXE6 bit in MPXCR and the BCSEL6 bit in SRAMCR. Table 6.13 shows the external interface of area 6.

Table 6.13 Area 6 External Interface

	Register Setting	
Interface	**MPXE6 of MPXCR**	**BCSEL6 of SRAMCR**
Basic bus interface	0	0
Byte control SRAM interface	0	1
Address/data multiplexed I/O interface	1	0
Setting prohibited	1	1

(8) Area 7

Area 7 includes internal I/O registers. In external extended mode, area 7 other than internal I/O register area is external address space.

When area 7 external address space is accessed, the $\overline{CS7}$ signal can be output.

Either of the basic bus interface, byte control SRAM interface, or address/data multiplexed I/O interface can be selected for area 7 by the MPXE7 bit in MPXCR and the BCSEL7 bit in SRAMCR. Table 6.14 shows the external interface of area 7.

Table 6.14 Area 7 External Interface

	Register Setting	
Interface	**MPXE7 of MPXCR**	**BCSEL7 of SRAMCR**
Basic bus interface	0	0
Byte control SRAM interface	0	1
Address/data multiplexed I/O interface	1	0
Setting prohibited	1	1

(4) $\overline{\text{BREQO}}$ Output Timing

When the BREQOE bit is set to 1 and the $\overline{\text{BREQO}}$ signal is output, both the $\overline{\text{BREQO}}$ and $\overline{\text{BACK}}$ signals may go low simultaneously.

This will occur if the next external access request occurs while internal bus arbitration is in progress after the chip samples a low level of the $\overline{\text{BREQ}}$ signal.

Figure 7.15 shows an example of the extended repeat area operation.

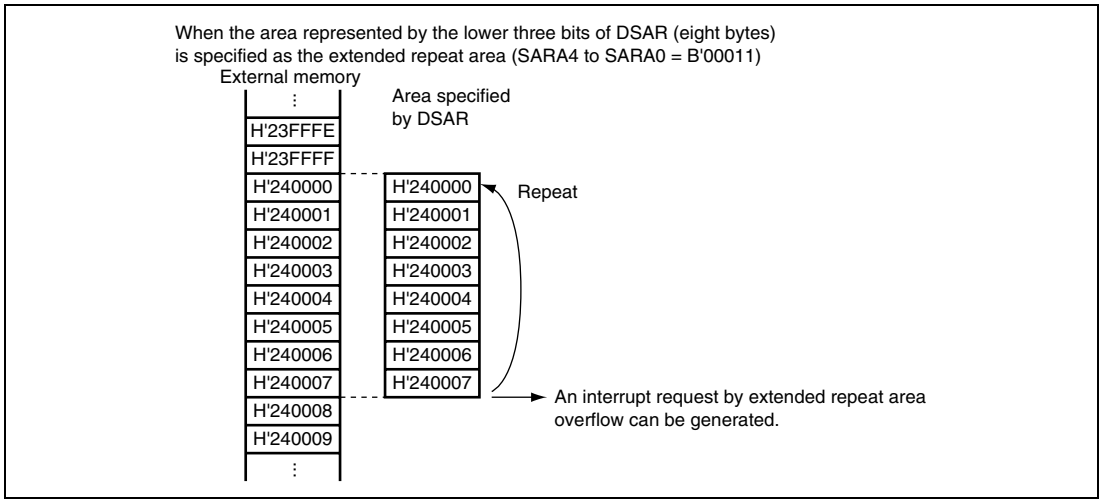

Figure 7.15 Example of Extended Repeat Area Operation

When an interrupt by an extended repeat area overflow is used in block transfer mode, the following should be taken into consideration.

When a transfer is stopped by an interrupt by an extended repeat area overflow, the address register must be set so that the block size is a power of 2 or the block size boundary is aligned with the extended repeat area boundary. When an overflow on the extended repeat area occurs during a transfer of one block, the interrupt by the overflow is suspended and the transfer overruns.

8.2.1 DTC Mode Register A (MRA)

MRA selects DTC operating mode. MRA cannot be accessed directly by the CPU.

Bit	7	6	5	4	3	2	1	0
Bit Name	MD1	MD0	Sz1	Sz0	SM1	SM0	—	—
Initial Value	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
R/W	—	—	—	—	—	—	—	—

Bit	Bit Name	Initial Value	R/W	Description
7	MD1	Undefined	—	DTC Mode 1 and 0
6	MD0	Undefined	—	Specify DTC transfer mode. 00: Normal mode 01: Repeat mode 10: Block transfer mode 11: Setting prohibited
5	Sz1	Undefined	—	DTC Data Transfer Size 1 and 0
4	Sz0	Undefined	—	Specify the size of data to be transferred. 00: Byte-size transfer 01: Word-size transfer 10: Longword-size transfer 11: Setting prohibited
3	SM1	Undefined	—	Source Address Mode 1 and 0
2	SM0	Undefined	—	Specify an SAR operation after a data transfer. 0x: SAR is fixed (SAR writeback is skipped) 10: SAR is incremented after a transfer (by 1 when Sz1 and Sz0 = B'00; by 2 when Sz1 and Sz0 = B'01; by 4 when Sz1 and Sz0 = B'10) 11: SAR is decremented after a transfer (by 1 when Sz1 and Sz0 = B'00; by 2 when Sz1 and Sz0 = B'01; by 4 when Sz1 and Sz0 = B'10)
1, 0	—	Undefined	—	Reserved The write value should always be 0.

[Legend]
X: Don't care

Bit	Bit Name	Initial Value	R/W	Description
15	DTCE15	0	R/W	DTC Activation Enable 15 to 0
14	DTCE14	0	R/W	Setting this bit to 1 specifies a relevant interrupt source to a DTC activation source.
13	DTCE13	0	R/W	[Clearing conditions]
12	DTCE12	0	R/W	• When writing 0 to the bit to be cleared after reading 1
11	DTCE11	0	R/W	• When the DISEL bit is 1 and the data transfer has ended
10	DTCE10	0	R/W	• When the specified number of transfers have ended
9	DTCE9	0	R/W	These bits are not cleared when the DISEL bit is 0 and the specified number of transfers have not ended
8	DTCE8	0	R/W	
7	DTCE7	0	R/W	
6	DTCE6	0	R/W	
5	DTCE5	0	R/W	
4	DTCE4	0	R/W	
3	DTCE3	0	R/W	
2	DTCE2	0	R/W	
1	DTCE1	0	R/W	
0	DTCE0	0	R/W	

8.2.8 DTC Control Register (DTCCR)

DTCCR specifies transfer information read skip.

Bit	7	6	5	4	3	2	1	0
Bit Name	—	—	—	RRS	RCHNE	—	—	ERR
Initial Value	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/(W)*

Note: * Only 0 can be written to clear the flag.

Bit	Bit Name	Initial Value	R/W	Description
7 to 5	—	All 0	R/W	Reserved These bits are always read as 0. The write value should always be 0.

9.3.5 Port Function Control Register 6 (PFCR6)

PFCR6 selects the TPU clock input pin.

Bit	7	6	5	4	3	2	1	0
Bit Name	—	LHWROE	—	—	TCLKS	—	—	—
Initial Value	1	1	1	0	0	0	0	0
R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	—	1	R/W	Reserved This bit is always read as 1. The write value should always be 1.
6	LHWROE	1	R/W	$\overline{\text{LHWR}}$ Output Enable Enables/disables $\overline{\text{LHWR}}$ output (valid in external extended mode). 0: Specifies pin PA4 as I/O port 1: Specifies pin PA4 as $\overline{\text{LHWR}}$ output pin
5	—	1	R/W	Reserved This bit is always read as 1. The write value should always be 1.
4	—	0	R	Reserved This is a read-only bit and cannot be modified.
3	TCLKS	0	R/W	TPU External Clock Input Pin Select Selects the TPU external clock input pins. 0: External clock input pins cannot be used. 1: Specifies pins P14 to P17 as external clock inputs
2 to 0	—	All 0	R/W	Reserved These bits are always read as 0. The write value should always be 0.

Table 10.13 TIORH_0

				Description	
Bit 7 IOB3	**Bit 6 IOB2**	**Bit 5 IOB1**	**Bit 4 IOB0**	**TGRB_0 Function**	**TIOCB0 Pin Function**
0	0	0	0	Output compare register	Output disabled
0	0	0	1	—	Setting prohibited
0	0	1	0		
0	0	1	1		
0	1	0	0		
0	1	0	1		
0	1	1	0		
0	1	1	1		
1	0	0	0		
1	0	0	1		
1	0	1	x		
1	1	x	x	Input capture register	Capture input source is channel 1/count clock Input capture at TCNT_1 count-up/count-down*

[Legend]

X: Don't care

Note: When bits TPSC2 to TPSC0 in TCR_1 are set to B'000 and Pϕ/1 is used as the TCNT_1 count clock, this setting is invalid and input capture is not generated.

Table 10.19 TIOR_4

				Description	
Bit 7 IOB3	**Bit 6 IOB2**	**Bit 5 IOB1**	**Bit 4 IOB0**	**TGRB_4 Function**	**TIOCB4 Pin Function**
0	0	0	0	Output compare register	Output disabled
0	0	0	1		Initial output is 0 output 0 output at compare match
0	0	1	0		Initial output is 0 output 1 output at compare match
0	0	1	1		Initial output is 0 output Toggle output at compare match
0	1	0	0		Output disabled
0	1	0	1		Initial output is 1 output 0 output at compare match
0	1	1	0		Initial output is 1 output 1 output at compare match
0	1	1	1		Initial output is 1 output Toggle output at compare match
1	0	0	0	Input capture register	Capture input source is TIOCB4 pin Input capture at rising edge
1	0	0	1		Capture input source is TIOCB4 pin Input capture at falling edge
1	0	1	x		Capture input source is TIOCB4 pin Input capture at both edges
1	1	x	x		Capture input source is TGRC_3 compare match/input capture Input capture at generation of TGRC_3 compare match/input capture

[Legend]

X: Don't care

12.5.4 Timing of Counter Clear by Compare Match

TCNT is cleared when compare match A or B occurs, depending on the settings of the bits CCLR1 and CCLR0 in TCR. Figure 12.11 shows the timing of this operation.

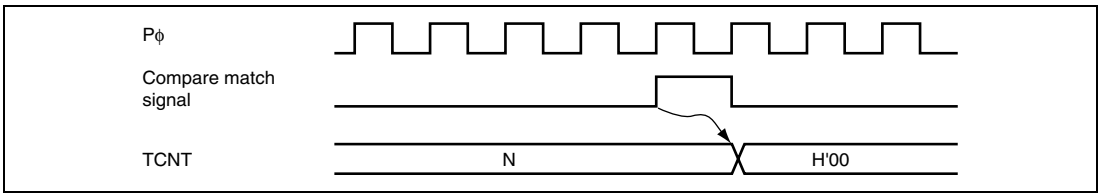

Figure 12.11 Timing of Counter Clear by Compare Match

12.5.5 Timing of TCNT External Reset*

TCNT is cleared at the rising edge or high level of an external reset input, depending on the settings of bits CCLR1 and CCLR0 in TCR. The clear pulse width must be at least 2 states. Figure 12.12 and Figure 12.13 shows the timing of this operation.

Note: * Clearing by an external reset is available only in units 0 and 1.

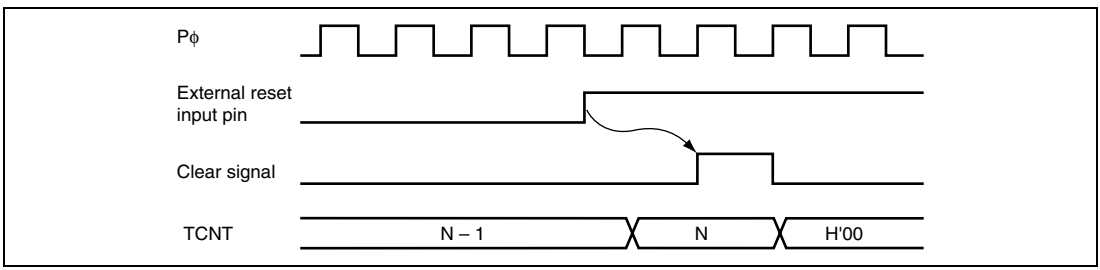

Figure 12.12 Timing of Clearance by External Reset (Rising Edge)

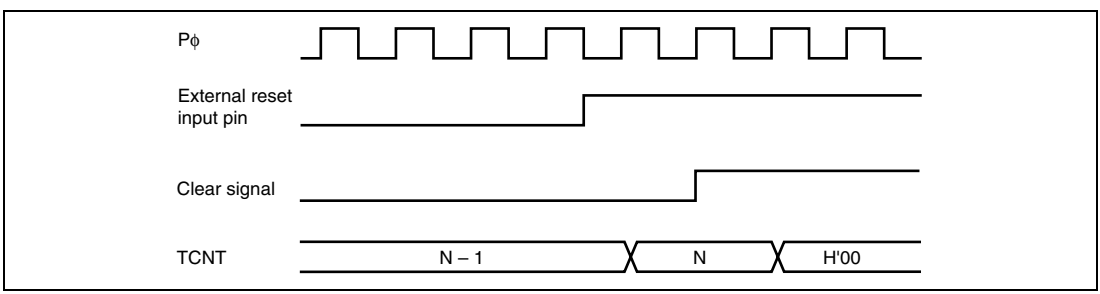

Figure 12.13 Timing of Clearance by External Reset (High Level)

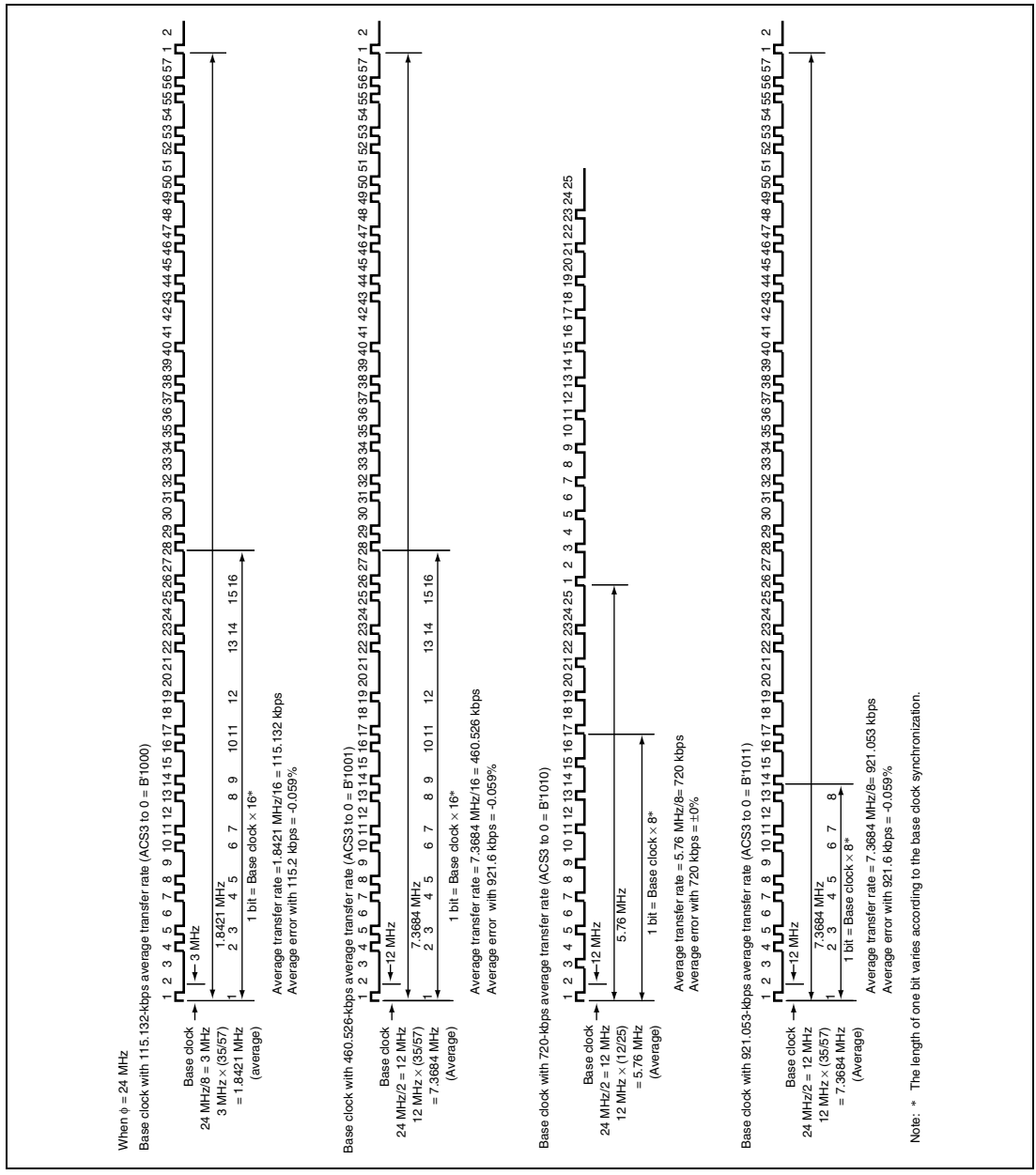

Figure 14.3 Examples of Base Clock when Average Transfer Rate Is Selected (3)

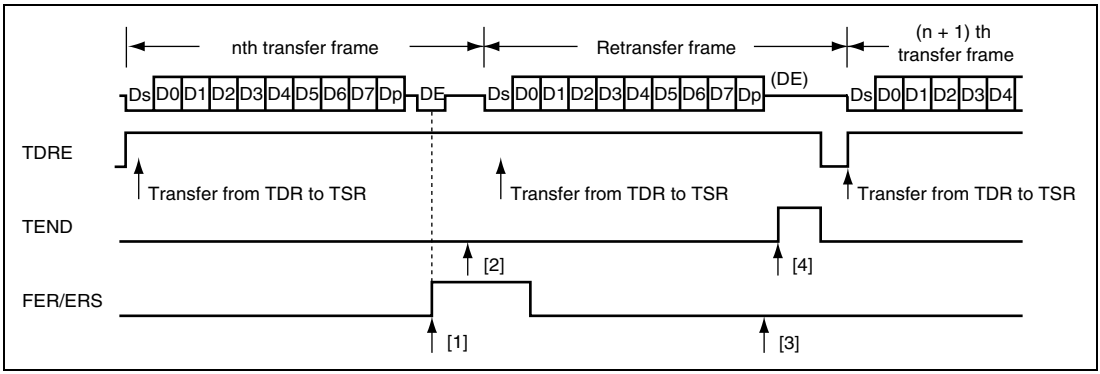

Figure 14.29 Data Re-Transfer Operation in SCI Transmission Mode

Note that the TEND flag is set in different timings depending on the GM bit setting in SMR. Figure 14.30 shows the TEND flag set timing.

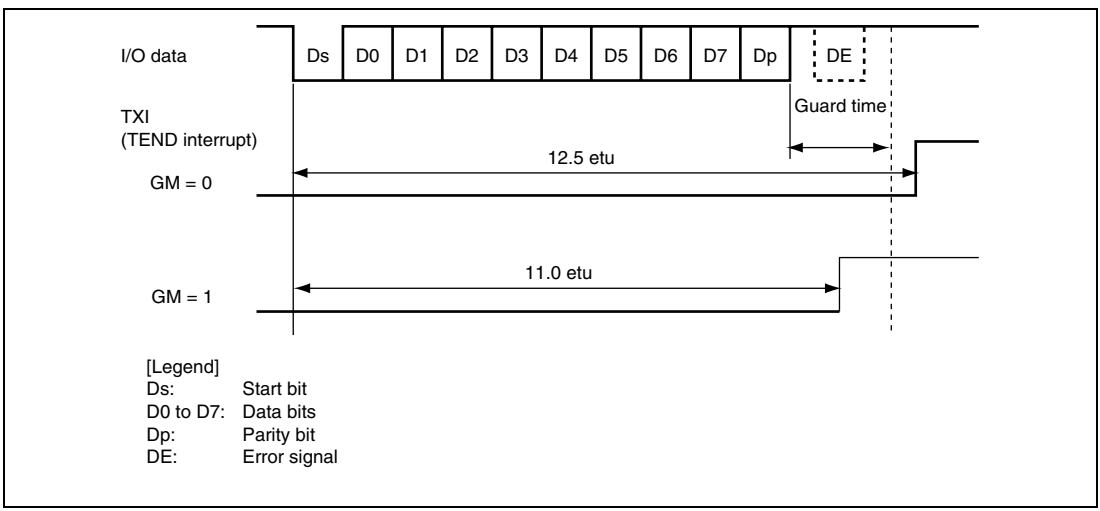

Figure 14.30 TEND Flag Set Timing during Transmission

Section 16 I²C Bus Interface2 (IIC2)

This LSI has a two-channel I²C bus interface.

The I²C bus interface conforms to and provides a subset of the Philips I²C bus (inter-IC bus) interface functions. The register configuration that controls the I²C bus differs partly from the Philips configuration, however.

Figure 16.1 shows the block diagram of the I²C bus interface2.

Figure 16.2 shows an example of I/O pin connections to external circuits.

16.1 Features

- Continuous transmission/reception

  Since the shift register, transmit data register, and receive data register are independent from each other, the continuous transmission/reception can be performed.
- Start and stop conditions generated automatically in master mode
- Selection of acknowledge output levels when receiving
- Automatic loading of acknowledge bit when transmitting
- Bit synchronization/wait function

  In master mode, the state of SCL is monitored per bit, and the timing is synchronized automatically. If transmission or reception is not yet possible, drive the SCL signal low until preparations are completed
- Six interrupt sources

  Transmit-data-empty (including slave-address match), transmit-end, receive-data-full (including slave-address match), arbitration lost, NACK detection, and stop condition detection
- Direct bus drive

  Two pins, the SCL and SDA pins function as NMOS open-drain outputs.

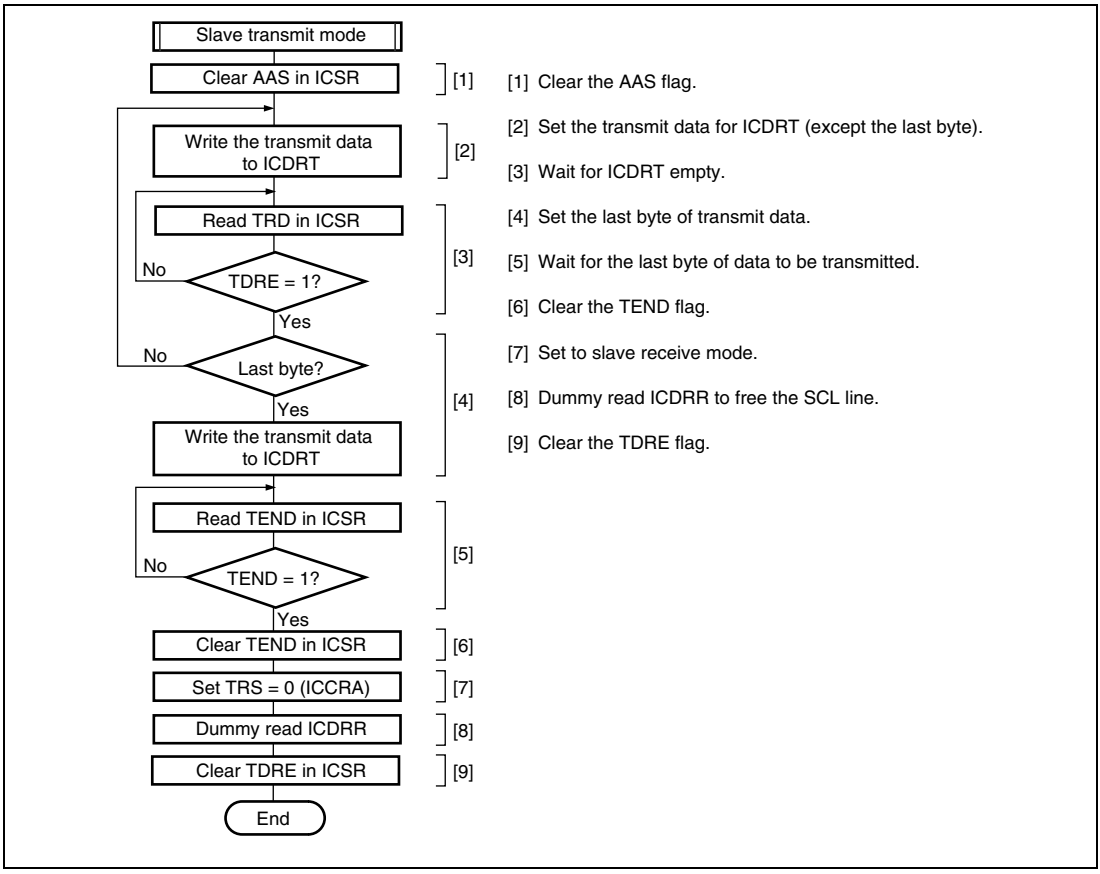

Figure 16.16 Sample Flowchart for Slave Transmit Mode

20.5 Input/Output Pins

The flash memory is controlled through the input/output pins shown in table 20.2.

Table 20.2 Pin Configuration

Abbreviation	I/O	Function
$\overline{\text{RES}}$	Input	Reset
EMLE	Input	On-chip emulator enable pin (EMLE = 0 for flash memory programming/erasing)
MD2 to MD0	Input	Set operating mode of this LSI
PM2	Input	SCI boot mode/USB boot mode setting (for boot mode setting by MD2 to MD0)
TxD4	Output	Serial transmit data output (used in SCI boot mode)
RxD4	Input	Serial receive data input (used in SCI boot mode)
USD+, USD−	I/O	USB data I/O (used in USB boot mode)
VBUS	Input	USB cable connection/disconnection detect (used in USB boot mode)
PM3	Input	USB bus power mode/self power mode setting (used in USB boot mode)
PM4	Output	D+ pull-up control (used in USB boot mode)

(4) Flash Key Code Register (FKEY)

FKEY is a register for software protection that enables to download the on-chip program and perform programming/erasing of the flash memory.

Bit	7	6	5	4	3	2	1	0
Bit Name	K7	K6	K5	K4	K3	K2	K1	K0
Initial Value	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	K7	0	R/W	Key Code
6	K6	0	R/W	When H'A5 is written to FKEY, writing to the SCO bit in FCCS is enabled. When a value other than H'A5 is written, the SCO bit cannot be set to 1. Therefore, the on-chip program cannot be downloaded to the on-chip RAM.
5	K5	0	R/W	
4	K4	0	R/W	
3	K3	0	R/W	
2	K2	0	R/W	Only when H'5A is written can programming/erasing of the flash memory be executed. When a value other than H'5A is written, even if the programming/erasing program is executed, programming/erasing cannot be performed.
1	K1	0	R/W	
0	K0	0	R/W	
				H'A5: Writing to the SCO bit is enabled. (The SCO bit cannot be set to 1 when FKEY is a value other than H'A5.)
				H'5A: Programming/erasing of the flash memory is enabled. (When FKEY is a value other than H'A5, the software protection state is entered.)
				H'00: Initial value

Register Abbreviation	Reset	Sleep	Module Stop	All-Module-Clock-Stop	Software Standby	Hardware Standby	Module
TCR_2	Initialized	—	—	—	—	Initialized	TPU_2
TMDR_2	Initialized	—	—	—	—	Initialized	
TIOR_2	Initialized	—	—	—	—	Initialized	
TIER_2	Initialized	—	—	—	—	Initialized	
TSR_2	Initialized	—	—	—	—	Initialized	
TCNT_2	Initialized	—	—	—	—	Initialized	
TGRA_2	Initialized	—	—	—	—	Initialized	
TGRB_2	Initialized	—	—	—	—	Initialized	
TCR_3	Initialized	—	—	—	—	Initialized	TPU_3
TMDR_3	Initialized	—	—	—	—	Initialized	
TIORH_3	Initialized	—	—	—	—	Initialized	
TIORL_3	Initialized	—	—	—	—	Initialized	
TIER_3	Initialized	—	—	—	—	Initialized	
TSR_3	Initialized	—	—	—	—	Initialized	
TCNT_3	Initialized	—	—	—	—	Initialized	
TGRA_3	Initialized	—	—	—	—	Initialized	
TGRB_3	Initialized	—	—	—	—	Initialized	
TGRC_3	Initialized	—	—	—	—	Initialized	
TGRD_3	Initialized	—	—	—	—	Initialized	

Port Name	MCU Operating Mode	Reset	Hardware Standby Mode	Software Standby Mode		Bus Released State
				OPE = 1	OPE = 0	
PA6/ $\overline{AS}$/ $\overline{AH}$/ $\overline{BS}$-B	Single-chip mode (EXPE = 0)	Hi-Z	Hi-Z	[$\overline{AS}$, $\overline{BS}$ output]	[$\overline{AS}$, $\overline{AH}$, $\overline{BS}$ output]	[$\overline{AS}$, $\overline{AH}$, $\overline{BS}$ output]
	External extended mode (EXPE = 1)	H		H	Hi-Z	Hi-Z
				[$\overline{AH}$ output]	[Other than above]	[Other than above]
				L	Keep	Keep
				[Other than above]		
				Keep		
PA7/Bϕ	Single-chip mode (EXPE = 0)	Hi-Z	Hi-Z	[Clock output]	[Clock output]	[Clock output]
	External extended mode (EXPE = 1)	Clock output	Hi-Z	H	H	Clock output
				[Other than above]	[Other than above]	[Other than above]
				Keep	Keep	Keep
PB0/ $\overline{CS0}$/ $\overline{CS4}$/ $\overline{CS5}$-B	Single-chip mode (EXPE = 0)	Hi-Z	Hi-Z	[$\overline{CS}$ output]	[$\overline{CS}$ output]	[$\overline{CS}$ output]
	External extended mode (EXPE = 1)	H		H	Hi-Z	Hi-Z
				[Other than above]	[Other than above]	[Other than above]
				Keep	Keep	Keep
PB1/ $\overline{CS1}$/ $\overline{CS2}$-B/ $\overline{CS5}$-A/ $\overline{CS6}$-B/ $\overline{CS7}$-B	All	Hi-Z	Hi-Z	[$\overline{CS}$ output]	[$\overline{CS}$ output]	[$\overline{CS}$ output]
				H	Hi-Z	Hi-Z
				[Other than above]	[Other than above]	[Other than above]
				Keep	Keep	Keep
PB2/ $\overline{CS2}$-A/ $\overline{CS6}$-A	All	Hi-Z	Hi-Z	[$\overline{CS}$ output]	[$\overline{CS}$ output]	[$\overline{CS}$ output]
				H	Hi-Z	Hi-Z
				[Other than above]	[Other than above]	[Other than above]
				Keep	Keep	Keep
PB3/ $\overline{CS3}$/ $\overline{CS7}$-A	All	Hi-Z	Hi-Z	[$\overline{CS}$ output]	[$\overline{CS}$ output]	[$\overline{CS}$ output]
				H	Hi-Z	Hi-Z
				[Other than above]	[Other than above]	[Other than above]
				Keep	Keep	Keep

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