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#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	11
Program Memory Size	1.5KB (1K x 12)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	72 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	14-SOIC (0.154", 3.90mm Width)
Supplier Device Package	14-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c505t-04-sl

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

AC CHARACTERISTICS			Electrical Characteristics:Industrial (I): $Vcc = +1.7V$ to 5.5V $TA = -40^{\circ}C$ to $+85^{\circ}C$ Automotive (E): $Vcc = +2.5V$ to 5.5V $TA = -40^{\circ}C$ to $+125^{\circ}C$				
Param. No.	Sym.	Characteristic	Min.	Max.	Units	Conditions	
1	FCLK	Clock Frequency	_	100	kHz	$1.7V \le Vcc \le 2.5V$	
				100	kHz	$2.5V \le VCC \le 4.5V$ , E-temp	
				400	kHz	$2.5V \le Vcc \le 5.5V$	
			_	400	kHz	1.8V ≤ Vcc ≤ 2.5V ( <b>24FC1026</b> )	
				1000	kHz	2.5V ≤ Vcc ≤ 5.5V ( <b>24FC1026</b> )	
2	THIGH	Clock High Time	4000	_	ns	$1.7V \le Vcc \le 2.5V$	
			4000	_	ns	$2.5V \le VCC \le 4.5V$ , E-temp	
			600	—	ns	$2.5V \le Vcc \le 5.5V$	
			600	—	ns	1.8V ≤ Vcc ≤ 2.5V ( <b>24FC1026</b> )	
			500	_	ns	2.5V ≤ Vcc ≤ 5.5V ( <b>24FC1026</b> )	
3	TLOW	Clock Low Time	4700	_	ns	$1.7V \le Vcc \le 2.5V$	
			4700	_	ns	$2.5V \le VCC \le 4.5V$ , E-temp	
			1300	_	ns	$2.5V \le Vcc \le 5.5V$	
			1300	—	ns	1.8V ≤ Vcc ≤ 2.5V ( <b>24FC1026</b> )	
		500	_	ns	2.5V ≤ Vcc ≤ 5.5V ( <b>24FC1026</b> )		
4	4 Tr	SDA and SCL Rise Time (Note 1)	_	1000	ns	$1.7V \le Vcc \le 2.5V$	
				1000	ns	$2.5V \le VCC \le 4.5V$ , E-temp	
			_	300	ns	$2.5V \le Vcc \le 5.5V$	
			_	300	ns	1.8V ≤ Vcc ≤ 2.5V ( <b>24FC1026</b> )	
			_	300	ns	2.5V ≤ Vcc ≤ 5.5V ( <b>24FC1026</b> )	
5	TF	SDA and SCL Fall Time	_	300	ns	All except 24FC1026	
		(Note 1)	—	100	ns	1.8V ≤ Vcc ≤ 5.5V ( <b>24FC1026</b> )	
6	THD:STA	DISTA Start Condition Hold Time	4000	—	ns	$1.7V \le Vcc \le 2.5V$	
			4000	—	ns	$2.5V \le VCC \le 4.5V$ , E-temp	
			600	_	ns	$2.5V \le VCC \le 5.5V$	
			600	_	ns	$1.8V \le VCC \le 2.5V$ (24FC1026)	
			250	_	ns	$2.5V \le VCC \le 5.5V$ ( <b>24FC1026</b> )	
7	TSU:STA	Start Condition Setup	4700		ns	$1.7V \le VCC \le 2.5V$	
		Time	4700	—	ns	$2.5V \le VCC \le 4.5V$ , E-temp	
			600		ns	$2.5V \le VCC \le 5.5V$	
			600		ns	1.8V ≤ Vcc ≤ 2.5V ( <b>24FC1026</b> )	
			250	—	ns	2.5V ≤ Vcc ≤ 5.5V ( <b>24FC1026</b> )	
8	THD:DAT	Data Input Hold Time	0	_	ns	(Note 2)	

#### TABLE 1-2: AC CHARACTERISTICS

Note 1: Not 100% tested. CB = total capacitance of one bus line in pF.

**2:** As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

**3:** The combined TSP and VHYS specifications are due to new Schmitt Trigger inputs which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but established by characterization. For endurance estimates in a specific application, please consult the Total Endurance<sup>™</sup> Model which can be obtained from Microchip's website at www.microchip.com.

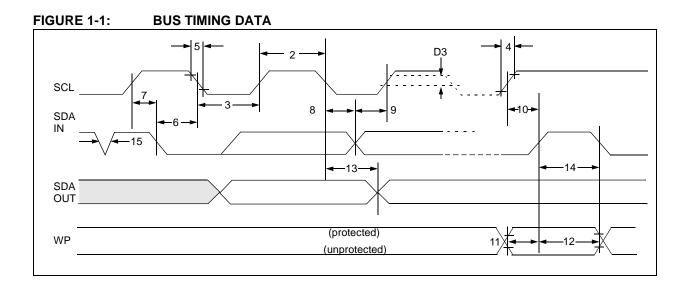
AC CHARACTERISTICS (Continued)			Electrical Characteristics: Industrial (I): VCC = $+1.7V$ to 5.5V TA = $-40^{\circ}$ C to $+85^{\circ}$ C Automotive (E): Vcc = $+2.5V$ to 5.5V TA = $-40^{\circ}$ C to $+125^{\circ}$ C				
Param. No.	Sym.	Characteristic	Min.	Max.	Units	Conditions	
9	TSU:DAT	Data Input Setup Time	250	_	ns	$1.7V \le Vcc \le 2.5V$	
			250		ns	$2.5V \le VCC \le 4.5V$ , E-temp	
			100		ns	$2.5V \le VCC \le 5.5V$	
			100	_	ns	1.8V ≤ Vcc ≤ 2.5V ( <b>24FC1026</b> )	
			100	_	ns	2.5V ≤ Vcc ≤ 5.5V ( <b>24FC1026</b> )	
10	Tsu:sto	Stop Condition Setup	4000		ns	$1.7V \le Vcc \le 2.5V$	
		Time	4000		ns	$2.5V \le VCC \le 4.5V$ , E-temp	
			600		ns	$2.5V \le Vcc \le 5.5V$	
			600		ns	1.8V ≤ Vcc ≤ 2.5V ( <b>24FC1026</b> )	
			250	_	ns	2.5V ≤ Vcc ≤ 5.5V ( <b>24FC1026</b> )	
11	TSU:WP	WP Setup Time	4000		ns	$1.7V \le Vcc \le 2.5V$	
			4000		ns	$2.5V \le VCC \le 4.5V$ , E-temp	
			600	_	ns	$2.5V \le Vcc \le 5.5V$	
			600		ns	1.8V ≤ Vcc ≤ 2.5V ( <b>24FC1026</b> )	
			600		ns	2.5V ≤ Vcc ≤ 5.5V ( <b>24FC1026</b> )	
12	THD:WP	WP Hold Time	4700	_	ns	$1.7V \le Vcc \le 2.5V$	
			4700		ns	$2.5V \le VCC \le 4.5V$ , E-temp	
			1300	_	ns	$2.5V \le Vcc \le 5.5V$	
			1300	_	ns	1.8V ≤ Vcc ≤ 2.5V ( <b>24FC1026</b> )	
			1300		ns	2.5V ≤ Vcc ≤ 5.5V ( <b>24FC1026</b> )	
13	ΤΑΑ	Output Valid from Clock	_	3500	ns	$1.7V \le Vcc \le 2.5V$	
		(Note 2)	_	3500	ns	$2.5V \le Vcc \le 4.5V$ , E-temp	
			_	900	ns	$2.5V \le Vcc \le 5.5V$	
			_	900	ns	1.8V ≤ Vcc ≤ 2.5V ( <b>24FC1026</b> )	
			_	400	ns	2.5V ≤ Vcc ≤ 5.5V ( <b>24FC1026</b> )	
14	TBUF	Bus Free Time: bus time	4700	_	ns	$1.7V \le Vcc \le 2.5V$	
		must be free before a new	4700	_	ns	$2.5V \le VCC \le 4.5V$ , E-temp	
	transmission can sta	transmission can start	1300		ns	$2.5V \leq VCC \leq 5.5V$	
			1300		ns	1.8V ≤ Vcc ≤ 2.5V ( <b>24FC1026</b> )	
			500		ns	2.5V ≤ Vcc ≤ 5.5V ( <b>24FC1026</b> )	
15	TSP	Input Filter Spike Suppression (SDA and SCL pins)	—	50	ns	All except 24FC1026 (Notes 1 and 3)	
16	Twc	Write Cycle Time (byte or page)	—	5	ms		
17		Endurance	1,000,000		cycles	Page mode, 25°C, Vcc = 5.5V (Note 4)	

Note 1: Not 100% tested. CB = total capacitance of one bus line in pF.

**2:** As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

**3:** The combined TSP and VHYS specifications are due to new Schmitt Trigger inputs which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but established by characterization. For endurance estimates in a specific application, please consult the Total Endurance<sup>™</sup> Model which can be obtained from Microchip's website at www.microchip.com.



#### 2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TADLE Z-T.	FINTO	FIN FONCTION TABLE					
Name	PDIP	SOIC	SOIJ	Function			
NC	1	1	1	Not Connected			
A1	2	2	2	User Configurable Chip Select			
A2	3	3	3	User Configurable Chip Select			
Vss	4	4	4	Ground			
SDA	5	5	5	Serial Data			
SCL	6	6	6	Serial Clock			
WP	7	7	7	Write-Protect Input			
Vcc	8	8	8	+1.7 to 5.5V (24AA1026) +2.5 to 5.5V (24LC1026) +1.8 to 5.5V (24FC1026)			

#### TABLE 2-1: PIN FUNCTION TABLE

#### 2.1 A1, A2 Chip Address Inputs

The A1 and A2 inputs are used by the 24XX1026 for multiple device operations. The levels on these inputs are compared with the corresponding bits in the slave address. The chip is selected if the comparison is true.

Up to four devices may be connected to the same bus by using different Chip Select bit combinations. In most applications, the chip address inputs A1 and A2 are hard-wired to logic '0' or logic '1'. For applications in which these pins are controlled by a microcontroller or other programmable device, the chip address pins must be driven to logic '0' or logic '1' before normal device operation can proceed.

#### 2.2 Serial Data (SDA)

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open-drain terminal, therefore, the SDA bus requires a pull-up resistor to Vcc (typical 10 k $\Omega$  for 100 kHz, 2 k $\Omega$ for 400 kHz and 1 MHz).

For normal data transfer, SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the Start and Stop conditions.

### 2.3 Serial Clock (SCL)

This input is used to synchronize the data transfer from and to the device.

#### 2.4 Write-Protect (WP)

This pin must be connected to either Vss or Vcc. If tied to Vss, write operations are enabled. If tied to Vcc, write operations are inhibited, but read operations are not affected.

### 3.0 FUNCTIONAL DESCRIPTION

The 24XX1026 supports a bidirectional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data as a receiver. The bus must be controlled by a master device which generates the Serial Clock (SCL), controls the bus access, and generates the Start and Stop conditions while the 24XX1026 works as a slave. Both master and slave can operate as a transmitter or receiver, but the master device determines which mode is activated.

### 6.0 WRITE OPERATIONS

#### 6.1 Byte Write

Following the Start condition from the master, the control code (four bits), the Chip Select (two bits), the block select (one bit), and the R/W bit (which is a logic low) are clocked onto the bus by the master transmitter. This indicates to the addressed slave receiver that the address high byte will follow after it has generated an Acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the high-order byte of the word address and will be written into the Address Pointer of the 24XX1026. The next byte is the Least Significant Address Byte. After receiving another Acknowledge signal from the 24XX1026, the master device will transmit the data word to be written into the addressed memory location. The 24XX1026 acknowledges again and the master generates a Stop condition. This initiates the internal write cycle and during this time, the 24XX1026 will not generate Acknowledge signals as long as the control byte being polled matches the control byte that was used to initiate the write (Figure 6-1). If an attempt is made to write to the array with the WP pin held high, the device will acknowledge the command, but no write cycle will occur, no data will be written and the device will immediately accept a new command. After a byte Write command, the internal address counter will point to the address location following the one that was just written.

Note:	When doing a write of less than 128 bytes			
	the data in the rest of the page is			
	refreshed along with the data bytes being			
	written. This will force the entire page to			
	endure a write cycle, for this reason			
	endurance is specified per page.			

#### 6.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24XX1026 in the same way as in a byte write. But instead of generating a Stop condition, the master transmits up to 127 additional bytes, which are temporarily stored in the on-chip page buffer and will be written into memory after the master has transmitted a Stop condition. After receipt of each word, the seven lower Address Pointer bits are internally incremented by one. If the master should transmit more than 128 bytes prior to generating the Stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the Stop condition is received, an internal write cycle will begin (Figure 6-2). If an attempt is made to write to the array with the WP pin held high, the device will acknowledge the command, but no write cycle will occur, no data will be written and the device will immediately accept a new command.

#### 6.3 Write Protection

The WP pin allows the user to write-protect the entire array (00000-1FFFF) when the pin is tied to Vcc. If tied to Vss the write protection is disabled. The WP pin is sampled at the Stop bit for every Write command (Figure 1-1). Toggling the WP pin after the Stop bit will have no effect on the execution of the write cycle.

Note: Page write operations are limited to writing bytes within a single physical page, regardless of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or 'page size') and end at addresses that are integer multiples of [page size - 1]. If a Page Write command attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page as might be expected. It is therefore necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

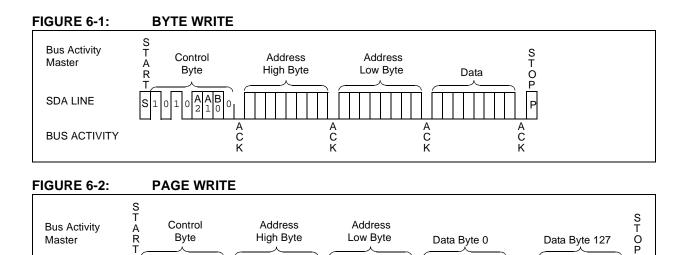
0 2 1 0 0

A C K

S

SDA Line

Bus Activity



A C K ТТТ

A C K  тттт

A C K Ρ

A C K

#### 7.0 ACKNOWLEDGE POLLING

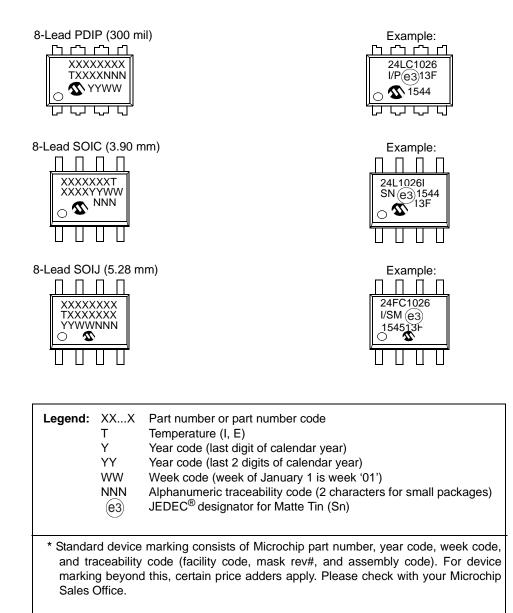
Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete. (This feature can be used to maximize bus throughput.) Once the Stop condition for a Write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a Start condition, followed by the control byte for a Write command (R/W = 0). If the device is still busy with the write cycle, then no ACK will be returned. If no ACK is returned, then the Start bit and control byte must be resent. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next Read or Write command. See Figure 7-1 for flow diagram.

**Note:** Care must be taken when polling the 24XX1026. The control byte that was used to initiate the write needs to match the control byte used for polling.

### FIGURE 7-1: ACKNOWLEDGE **POLLING FLOW** Send Write Command Send Stop Condition to Initiate Write Cycle Send Start Send Control Byte with $R/\overline{W} = 0$ Did Device No Acknowledge (ACK = 0)?Yes Next Operation

### 9.0 PACKAGING INFORMATION

### 9.1 Package Marking Information\*

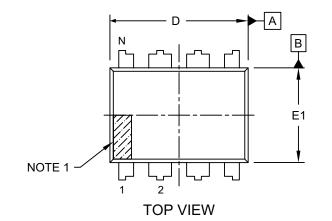


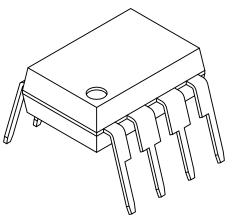
Note:	For very small packages with no room for the JEDEC <sup>®</sup> designator
	$(e_3)$ , the marking will only appear on the outer carton or reel label.

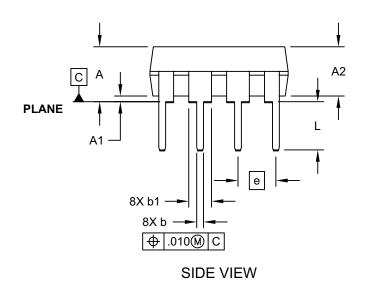
**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

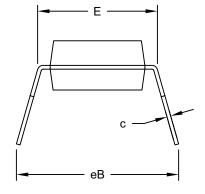
#### 8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging







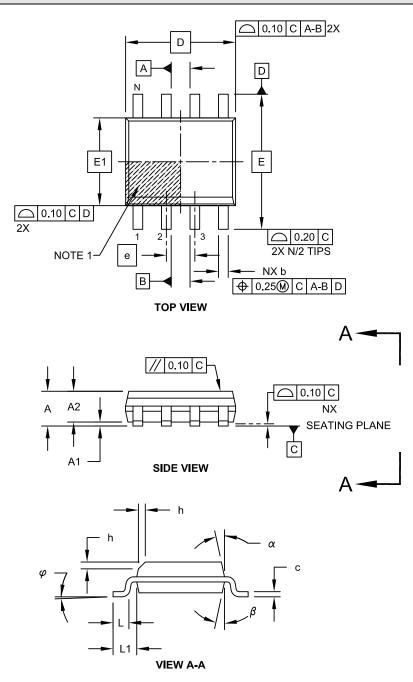


END VIEW

Microchip Technology Drawing No. C04-018D Sheet 1 of 2

#### 8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

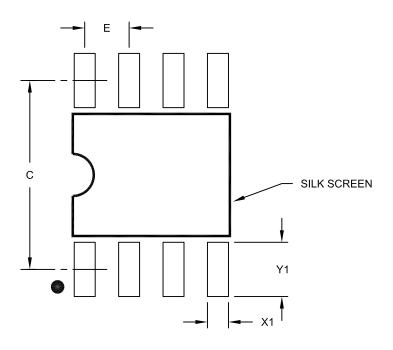
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-057C Sheet 1 of 2

#### 8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	MILLIMETERS			
Dimension	MIN	NOM	MAX	
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	С		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

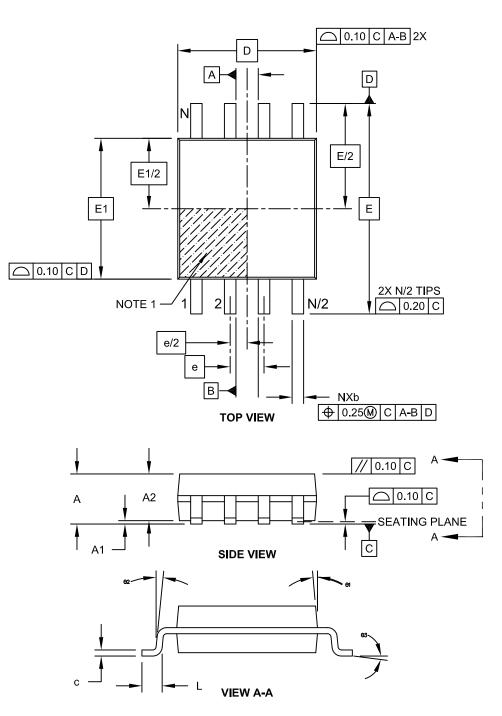
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

#### 8-Lead Plastic Small Outline (SM) - Medium, 5.28 mm Body [SOIJ]

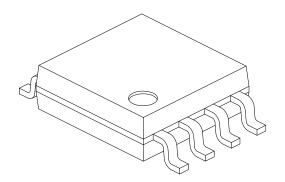
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-056C Sheet 1 of 2

#### 8-Lead Plastic Small Outline (SM) - Medium, 5.28 mm Body [SOIJ]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS				
Dimensio	on Limits	MIN	NOM	MAX	
Number of Pins	N	8			
Pitch	е		1.27 BSC		
Overall Height	A	1.77	-	2.03	
Standoff §	A1	0.05		0.25	
Molded Package Thickness	A2	1.75	-	1.98	
Overall Width		7.94 BSC			
Molded Package Width	E1		5.25 BSC		
Overall Length	D		5.26 BSC		
Foot Length	L	0.51	-	0.76	
Lead Thickness	С	0.15	-	0.25	
Lead Width	b	0.36	-	0.51	
Mold Draft Angle	Θ1	-	-	15°	
Lead Angle	Θ2	0°	-	8°	
Foot Angle	Θ3	0°	-	8°	

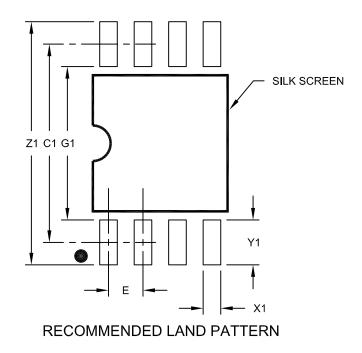
Notes:

- 1. SOIJ, JEITA/EIAJ Standard, Formerly called SOIC
- 2. § Significant Characteristic
- 3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.

Microchip Technology Drawing No. C04-056C Sheet 2 of 2

8-Lead Plastic Small Outline (SM) - Medium, 5.28 mm Body [SOIJ]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS			
Dimen	Dimension Limits		NOM	MAX
Contact Pitch E		1.27 BSC		
Overall Width	Z1			9.00
Contact Pad Spacing	C1		7.30	
Contact Pad Width (X8)	X1			0.65
Contact Pad Length (X8)	Y1			1.70
Distance Between Pads	G1	5.60		
Distance Between Pads	G	0.62		

#### Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2056C

### APPENDIX A: REVISION HISTORY

#### Revision A (01/2011)

Original release of this document.

#### Revision B (5/2011)

Added Automotive Temperature.

#### Revision C (04/2012)

Revised document title (removed CMOS); Revised Table 1-1, Param D9; Revised Section 5.1.

#### Revision D (07/2013)

Added TSSOP package.

#### **Revision E (11/2015)**

Removed TSSOP package.

NOTES:

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- Business of Microchip Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

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#### **PRODUCT IDENTIFICATION SYSTEM**

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	<u>[X]</u> <sup>(1)</sup> X /X	Examples:
Device	Tape and Reel Temperature Pack Option Range	a) 244 44026 L/Dr. Industrial Temperature
Device:	24AA1026 = 1024K Bit 1.7V I <sup>2</sup> C CMOS 24AA1026T = 1024K Bit 1.7V I <sup>2</sup> C CMOS (Tape and Reel)	Serial EEPROM Serial EEPROM C) 24AA1026T-I/SN: Tape and Reel, Industrial Temperature, 1.7V, SOIC package
	24LC1026 = 1024K Bit 2.5V I <sup>2</sup> C CMOS 24LC1026T= 1024K Bit 2.5V I <sup>2</sup> C CMOS (Tape and Reel)	Serial EEPROM d) 24AA1026T-I/SM: Tape and Reel, Industrial Temperature,   1 TV SOL package
	24FC1026 = 1024K Bit 1.8V I <sup>2</sup> C CMOS 24FC1026T = 1024K Bit 1.8V I <sup>2</sup> C CMOS (Tape and Reel)	Serial EEPROM
Tape and	Blank = Standard packaging (tube or tra	f) 24FC1026T-I/SN: Tape and Reel, Industrial Temperature, 1.8V, SOIC package.
Reel Option:	T = Tape and Reel(1)	g) 24LC1026-I/P: Industrial Temperature, 2.5V, PDIP package.
Temperature Range:	$I = -40^{\circ}C \text{ to } +85^{\circ}C$ $E = -40^{\circ}C \text{ to } +125^{\circ}C$	h) 24LC1026T-I/SM: Tape and Reel, Industrial Temperature, 2.5V, SOIJ package.
Package:	P = Plastic DIP (300 mil Body), 8 SM = Plastic SOIJ (5.28 mm Body) SN = Plastic SOIC (3.90 mm Body)	8-lead
		Note1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering pur- poses and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

#### Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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ISBN: 978-1-5224-0012-7

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