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Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	40
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	6K x 8
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 13x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l081cbt6

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2 Description

The access line ultra-low-power STM32L081xx microcontrollers incorporate the high-performance ARM® Cortex®-M0+ 32-bit RISC core operating at a 32 MHz frequency, a memory protection unit (MPU), high-speed embedded memories (up to 192 Kbytes of Flash program memory, 6 Kbytes of data EEPROM and 20 Kbytes of RAM) plus an extensive range of enhanced I/Os and peripherals.

The STM32L081xx devices provide high power efficiency for a wide range of performance. It is achieved with a large choice of internal and external clock sources, an internal voltage adaptation and several low-power modes.

The STM32L081xx devices offer several analog features, one 12-bit ADC with hardware oversampling, two ultra-low-power comparators, AES, several timers, one low-power timer (LPTIM), four general-purpose 16-bit timers and two basic timer, one RTC and one SysTick which can be used as timebases. They also feature two watchdogs, one watchdog with independent clock and window capability and one window watchdog based on bus clock.

Moreover, the STM32L081xx devices embed standard and advanced communication interfaces: up to three I2Cs, two SPIs, four USARTs, a low-power UART (LPUART), .

The STM32L081xx also include a real-time clock and a set of backup registers that remain powered in Standby mode.

The ultra-low-power STM32L081xx devices operate from a 1.8 to 3.6 V power supply (down to 1.65 V at power down) with BOR and from a 1.65 to 3.6 V power supply without BOR option. They are available in the -40 to +125 °C temperature range. A comprehensive set of power-saving modes allows the design of low-power applications.



2.1 Device overview

Table 1. Ultra-low-power STM32L081xx device features and peripheral counts

Peripheral		STM32L081CB	STM32L081KZ	STM32L081CZ
Flash (Kbytes)		128 Kbytes	192 Kbytes	
Data EEPROM (Kbytes)		6 Kbytes		
RAM (Kbytes)		20 Kbytes		
AES		1		
Timers	General-purpose	4		
	Basic	2		
	LPTIMER	1		
RTC/SYSTICK/IWDG/WWDG		1/1/1/1		
Com. interfaces	SPI/I2S	6(4) ⁽¹⁾ /1	4(3) ⁽²⁾ /0	6(4) ⁽¹⁾ /1
	I ² C	3	2	3
	USART	4	3	4
	LPUART	1		
GPIOs		40	25 ⁽³⁾	40
Clocks: HSE/LSE/HSI/MSI/LSI		1/1/1/1/1		
12-bit synchronized ADC Number of channels		1 13	1 10	1 13
Comparators		2		
Max. CPU frequency		32 MHz		
Operating voltage		1.8 V to 3.6 V (down to 1.65 V at power-down) with BOR option 1.65 to 3.6 V without BOR option		
Operating temperatures		Ambient temperature: −40 to +125 °C Junction temperature: −40 to +130 °C		
Packages		LQFP48	LQFP32, UFQFPN32	LQFP48

1. 4 SPI interfaces are USARTs operating in SPI master mode.
2. 3 SPI interfaces are USARTs operating in SPI master mode.
3. UFQFPN32 has 2 GPIOs less than LQFP32.

Table 2. Functionalities depending on the operating power supply range (continued)

Operating power supply range	Functionalities depending on the operating power supply range		
	ADC operation	Dynamic voltage scaling range	I/O operation
$V_{DD} = 2.0$ to 2.4 V	Conversion time up to 1.14 Msps	Range 1, range 2 or range 3	Full speed operation
$V_{DD} = 2.4$ to 3.6 V	Conversion time up to 1.14 Msps	Range 1, range 2 or range 3	Full speed operation

1. CPU frequency changes from initial to final must respect " $f_{cpu\ initial} < 4 * f_{cpu\ final}$ ". It must also respect 5 μ s delay between two changes. For example to switch from 4.2 MHz to 32 MHz, you can switch from 4.2 MHz to 16 MHz, wait 5 μ s, then switch from 16 MHz to 32 MHz.

Table 3. CPU frequency range depending on dynamic voltage scaling

CPU frequency range	Dynamic voltage scaling range
16 MHz to 32 MHz (1ws) 32 kHz to 16 MHz (0ws)	Range 1
8 MHz to 16 MHz (1ws) 32 kHz to 8 MHz (0ws)	Range 2
32 kHz to 4.2 MHz (0ws)	Range 3

Table 4. Functionalities depending on the working mode (from Run/active down to standby) ⁽¹⁾⁽²⁾

IPs	Run/Active	Sleep	Low-power run	Low-power sleep	Stop		Standby	
						Wakeup capability		Wakeup capability
CPU	Y	--	Y	--	--		--	
Flash memory	O	O	O	O	--		--	
RAM	Y	Y	Y	Y	Y		--	
Backup registers	Y	Y	Y	Y	Y		Y	
EEPROM	O	O	O	O	--		--	
Brown-out reset (BOR)	O	O	O	O	O	O	O	O
DMA	O	O	O	O	--		--	
Programmable Voltage Detector (PVD)	O	O	O	O	O	O	-	
Power-on/down reset (POR/PDR)	Y	Y	Y	Y	Y	Y	Y	Y
High Speed Internal (HSI)	O	O	--	--	(3)		--	

3.15.6 Window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.16 Communication interfaces

3.16.1 I²C bus

Up to three I²C interfaces (I2C1 and I2C3) can operate in multimaster or slave modes.

Each I²C interface can support Standard mode (Sm, up to 100 kbit/s), Fast mode (Fm, up to 400 kbit/s) and Fast Mode Plus (Fm+, up to 1 Mbit/s) with 20 mA output drive on some I/Os.

7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (2 addresses, 1 with configurable mask) are also supported as well as programmable analog and digital noise filters.

Table 9. Comparison of I2C analog and digital filters

	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2C peripheral clocks
Benefits	Available in Stop mode	1. Extra filtering capability vs. standard requirements. 2. Stable length
Drawbacks	Variations depending on temperature, voltage, process	Wakeup from Stop on address match is not available when digital filter is enabled.

In addition, I2C1 and I2C3 provide hardware support for SMBus 2.0 and PMBus 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts verifications and ALERT protocol management. I2C1/I2C3 also have a clock domain independent from the CPU clock, allowing the I2C1/I2C3 to wake up the MCU from Stop mode on address match.

Each I2C interface can be served by the DMA controller.

Refer to [Table 10](#) for an overview of I2C interface features.

Table 10. STM32L081xx I²C implementation

I2C features ⁽¹⁾	I2C1	I2C2	I2C3
7-bit addressing mode	X	X	X
10-bit addressing mode	X	X	X
Standard mode (up to 100 kbit/s)	X	X	X
Fast mode (up to 400 kbit/s)	X	X	X

Table 10. STM32L081xx I²C implementation (continued)

I ² C features ⁽¹⁾	I2C1	I2C2	I2C3
Fast Mode Plus with 20 mA output drive I/Os (up to 1 Mbit/s)	X	X ⁽²⁾	X
Independent clock	X	-	X
SMBus	X	-	X
Wakeup from STOP	X	-	X

1. X = supported.

2. See [Table 14: STM32L081xxx pin definition on page 35](#) for the list of I/Os that feature Fast Mode Plus capability

3.16.2 Universal synchronous/asynchronous receiver transmitter (USART)

The four USART interfaces (USART1, USART2, USART4 and USART5) are able to communicate at speeds of up to 4 Mbit/s.

They provide hardware management of the CTS, RTS and RS485 driver enable (DE) signals, multiprocessor communication mode, master synchronous communication and single-wire half-duplex communication mode. USART1 and USART2 also support SmartCard communication (ISO 7816), IrDA SIR ENDEC, LIN Master/Slave capability, auto baud rate feature and has a clock domain independent from the CPU clock, allowing to wake up the MCU from Stop mode using baudrates up to 42 Kbaud.

All USART interfaces can be served by the DMA controller.

[Table 11](#) for the supported modes and features of USART interfaces.

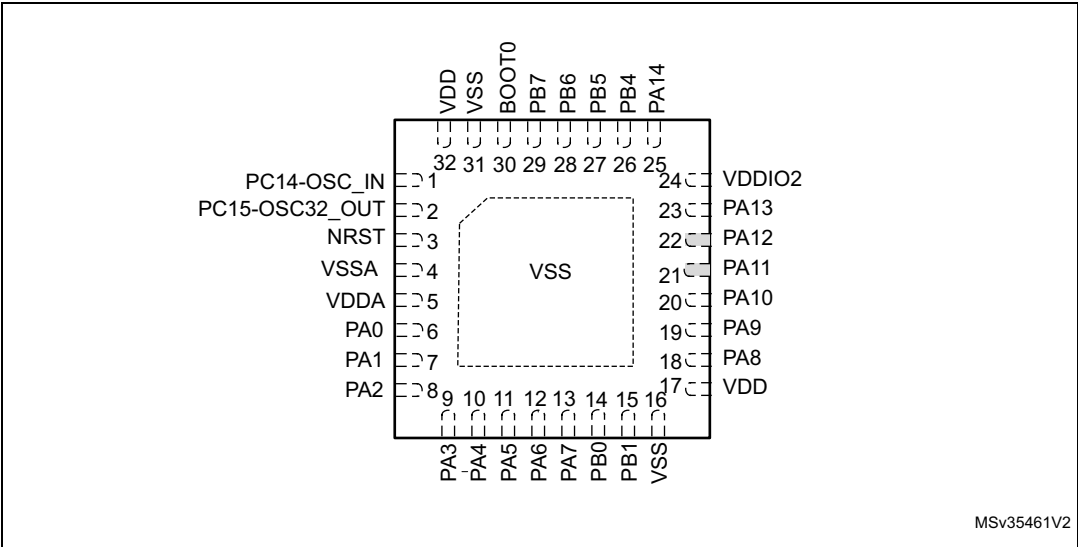
Table 11. USART implementation

USART modes/features ⁽¹⁾	USART1 and USART2	USART4 and USART5
Hardware flow control for modem	X	X
Continuous communication using DMA	X	X
Multiprocessor communication	X	X
Synchronous mode ⁽²⁾	X	X
Smartcard mode	X	-
Single-wire half-duplex communication	X	X
IrDA SIR ENDEC block	X	-
LIN mode	X	-
Dual clock domain and wakeup from Stop mode	X	-
Receiver timeout interrupt	X	-
Modbus communication	X	-
Auto baud rate detection (4 modes)	X	-
Driver Enable	X	X

1. X = supported.

2. This mode allows using the USART as an SPI master.

Figure 5. STM32L081xx UFQFPN32 pinout



MSv35461V2

1. The above figure shows the package top view.
2. I/O supplied by VDDIO2.

Table 13. Legend/abbreviations used in the pinout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input / output pin
I/O structure	FT	5 V tolerant I/O
	FTf	5 V tolerant I/O, FM+ capable
	TC	Standard 3.3V I/O
	B	Dedicated BOOT0 pin
	RST	Bidirectional reset pin with embedded weak pull-up resistor
Notes	Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset.	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers
	Additional functions	Functions directly selected/enabled through peripheral registers

Table 14. STM32L081xxx pin definition (continued)

Pin number			Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP32	UFQFPN32 ⁽¹⁾	LQFP48						
26	-	39	PB3	I/O	FT	-	SPI1_SCK, TIM2_CH2, EVENTOUT, USART1_RTS_DE, USART5_TX	COMP2_INM
27	26	40	PB4	I/O	FTf	-	SPI1_MISO, TIM3_CH1, TIM22_CH1, USART1_CTS, USART5_RX, I2C3_SDA	COMP2_INP
28	27	41	PB5	I/O	FT	-	SPI1_MOSI, LPTIM1_IN1, I2C1_SMBA, TIM3_CH2/TIM22_CH2, USART1_CK, USART5_CK/USART5_ RTS_DE	COMP2_INP
29	28	42	PB6	I/O	FTf	-	USART1_TX, I2C1_SCL, LPTIM1_ETR,	COMP2_INP
30	29	43	PB7	I/O	FTf	-	USART1_RX, I2C1_SDA, LPTIM1_IN2, USART4_CTS	COMP2_INP, VREF_PVD_IN
31	30	44	BOOT0	I		-	-	-
-	-	45	PB8	I/O	FTf	-	I2C1_SCL	-
-	-	46	PB9	I/O	FTf	-	EVENTOUT, I2C1_SDA, SPI2_NSS/I2S2_WS	-
32	31	47	VSS	S		-	-	-
-	32	48	VDD	S		-	-	-

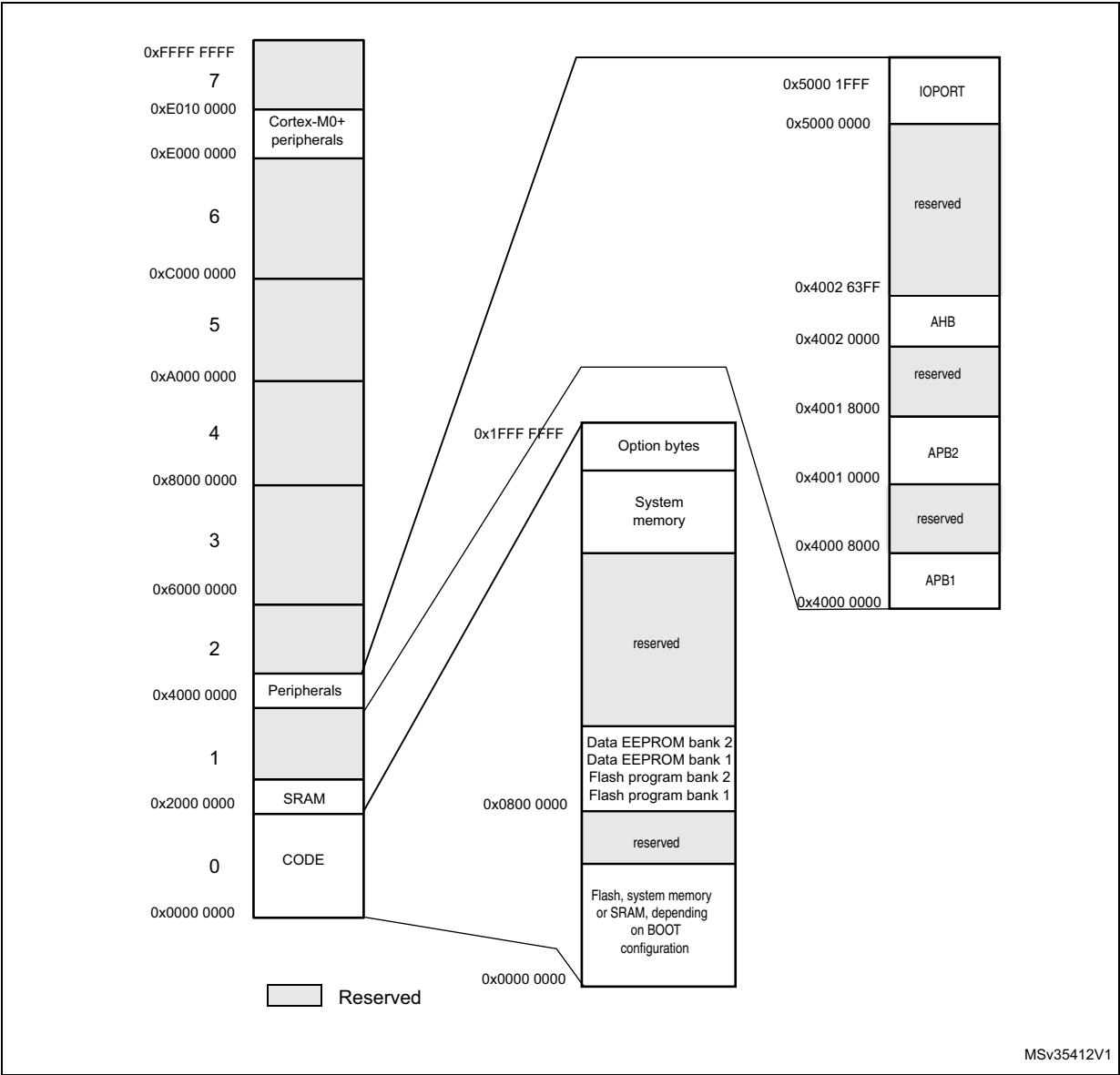
1. UFQFPN32 pinout differs from other STM32 devices except STM32L07xxx and STM32L8xxx.

Table 15. Alternate functions port A

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SPI1/SPI2/I2S2/ USART1/2/ LPUART1/ LPTIM1 TIM2/21/22/ EVENTOUT/ SYS_AF	SPI1/SPI2/I2S2/ I2C1/TIM2/21	SPI1/SPI2/I2S2/ LPUART1/ USART5/LPTIM1/ TIM2/3/ EVENTOUT/ SYS_AF	I2C1/ EVENTOUT	I2C1/USART1/2/L PUART1/ TIM3/22/ EVENTOUT	SPI2/I2S2/I2C2/ USART1/ TIM2/21/22	I2C1/2/ LPUART1/ USART4/ UASRT5/TIM21/ EVENTOUT	I2C3/LPUART1/ COMP1/2/ TIM3
Port A	PA0	-	-	TIM2_CH1	-	USART2_CTS	TIM2_ETR	USART4_TX	COMP1_OUT
	PA1	EVENTOUT	-	TIM2_CH2	-	USART2_RTS_D E	TIM21_ETR	USART4_RX	-
	PA2	TIM21_CH1	-	TIM2_CH3	-	USART2_TX	-	LPUART1_TX	COMP2_OUT
	PA3	TIM21_CH2	-	TIM2_CH4	-	USART2_RX	-	LPUART1_RX	-
	PA4	SPI1_NSS	-	-	-	USART2_CK	TIM22_ETR	-	-
	PA5	SPI1_SCK	-	TIM2_ETR	-		TIM2_CH1	-	-
	PA6	SPI1_MISO	-	TIM3_CH1	-	LPUART1_CTS	TIM22_CH1	EVENTOUT	COMP1_OUT
	PA7	SPI1_MOSI	-	TIM3_CH2	-	-	TIM22_CH2	EVENTOUT	COMP2_OUT
	PA8	MCO	-	-	EVENTOUT	USART1_CK	-	-	I2C3_SCL
	PA9	MCO	-	-	-	USART1_TX	-	I2C1_SCL	I2C3_SMBA
	PA10	-	-	-	-	USART1_RX	-	I2C1_SDA	-
	PA11	SPI1_MISO	-	EVENTOUT	-	USART1_CTS	-	-	COMP1_OUT
	PA12	SPI1_MOSI	-	EVENTOUT	-	USART1_RTS_D E	-	-	COMP2_OUT
	PA13	SWDIO	-	-	-	-	-	LPUART1_RX	-
	PA14	SWCLK	-	-	-	USART2_TX	-	LPUART1_TX	-
	PA15	SPI1_NSS	-	TIM2_ETR	EVENTOUT	USART2_RX	TIM2_CH1	USART4_RTS_D E	-

5 Memory mapping

Figure 6. Memory map



1. Refer to the STM32L081xx reference manual for details on the Flash memory organization for each memory size.

Figure 15. I_{DD} vs V_{DD} , at $T_A = 25/55/85/105/125\text{ }^{\circ}\text{C}$, Stop mode with RTC disabled, all clocks off

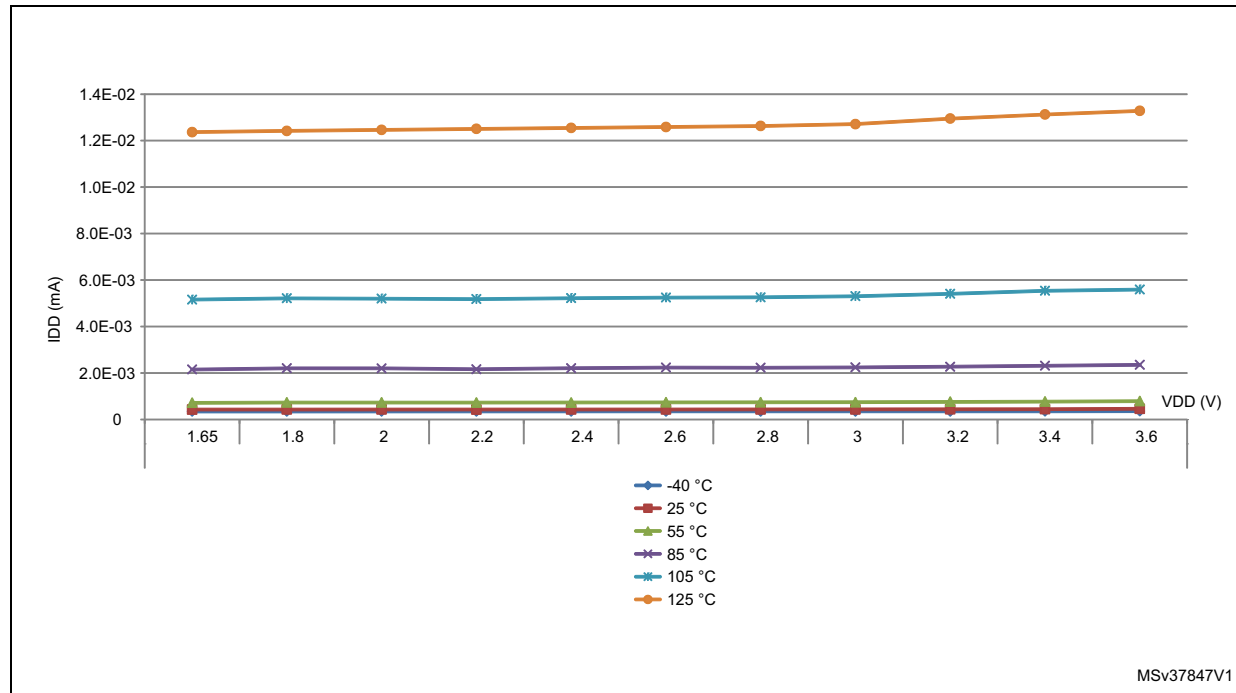


Table 32. Typical and maximum current consumptions in Standby mode

Symbol	Parameter	Conditions		Typ	Max ⁽¹⁾	Unit
I_{DD} (Standby)	Supply current in Standby mode	Independent watchdog and LSI enabled	$T_A = -40\text{ to }25\text{ }^{\circ}\text{C}$	0,855	1,70	μA
			$T_A = 55\text{ }^{\circ}\text{C}$	-	2,90	
			$T_A = 85\text{ }^{\circ}\text{C}$	-	3,30	
			$T_A = 105\text{ }^{\circ}\text{C}$	-	4,10	
			$T_A = 125\text{ }^{\circ}\text{C}$	-	8,50	
		Independent watchdog and LSI off	$T_A = -40\text{ to }25\text{ }^{\circ}\text{C}$	0,29	0,60	
			$T_A = 55\text{ }^{\circ}\text{C}$	0,32	1,20	
			$T_A = 85\text{ }^{\circ}\text{C}$	0,5	2,30	
			$T_A = 105\text{ }^{\circ}\text{C}$	0,94	3,00	
			$T_A = 125\text{ }^{\circ}\text{C}$	2,6	7,00	

1. Guaranteed by characterization results at $125\text{ }^{\circ}\text{C}$, unless otherwise specified

Table 34. Peripheral current consumption in Run or Sleep mode⁽¹⁾ (continued)

Peripheral		Typical consumption, $V_{DD} = 3.0\text{ V}$, $T_A = 25\text{ °C}$				Unit
		Range 1, $V_{CORE}=1.8\text{ V}$ $VOS[1:0] = 01$	Range 2, $V_{CORE}=1.5\text{ V}$ $VOS[1:0] = 10$	Range 3, $V_{CORE}=1.2\text{ V}$ $VOS[1:0] = 11$	Low-power sleep and run	
Cortex-M0+ core I/O port	GPIOA	3.5	3	2.5	2.5	$\mu\text{A/MHz}$ (f_{HCLK})
	GPIOB	3.5	2.5	2	2.5	
	GPIOC	8.5	6.5	5.5	7	
	GIOD	1	0.5	0.5	0.5	
	GPIOE	8	6	5	6	
	GPIOH	1.5	1	1	0.5	
AHB	CRC	1.5	1	1	1	$\mu\text{A/MHz}$ (f_{HCLK})
	FLASH	0 ⁽³⁾	0 ⁽³⁾	0 ⁽³⁾	0 ⁽³⁾	
	AES	0 ⁽³⁾	0 ⁽³⁾	0 ⁽³⁾	0 ⁽³⁾	
	DMA1	10	8	6.5	8.5	
All enabled		204	162	130	202	$\mu\text{A/MHz}$ (f_{HCLK})
PWR		2.5	2	2	1	$\mu\text{A/MHz}$ (f_{HCLK})

1. Data based on differential I_{DD} measurement between all peripherals off and one peripheral with clock enabled, in the following conditions: $f_{HCLK} = 32\text{ MHz}$ (range 1), $f_{HCLK} = 16\text{ MHz}$ (range 2), $f_{HCLK} = 4\text{ MHz}$ (range 3), $f_{HCLK} = 64\text{ kHz}$ (Low-power run/sleep), $f_{APB1} = f_{HCLK}$, $f_{APB2} = f_{HCLK}$, default prescaler value for each peripheral. The CPU is in Sleep mode in both cases. No I/O pins toggling. Not tested in production.
2. HSI oscillator is off for this measure.
3. Current consumption is negligible and close to 0 μA .

Table 43. MSI oscillator characteristics (continued)

Symbol	Parameter	Condition	Typ	Max	Unit
$I_{DD(MSI)}^{(2)}$	MSI oscillator power consumption	MSI range 0	0.75	-	μA
		MSI range 1	1	-	
		MSI range 2	1.5	-	
		MSI range 3	2.5	-	
		MSI range 4	4.5	-	
		MSI range 5	8	-	
		MSI range 6	15	-	
$t_{SU(MSI)}$	MSI oscillator startup time	MSI range 0	30	-	μs
		MSI range 1	20	-	
		MSI range 2	15	-	
		MSI range 3	10	-	
		MSI range 4	6	-	
		MSI range 5	5	-	
		MSI range 6, Voltage range 1 and 2	3.5	-	
		MSI range 6, Voltage range 3	5	-	
$t_{STAB(MSI)}^{(2)}$	MSI oscillator stabilization time	MSI range 0	-	40	μs
		MSI range 1	-	20	
		MSI range 2	-	10	
		MSI range 3	-	4	
		MSI range 4	-	2.5	
		MSI range 5	-	2	
		MSI range 6, Voltage range 1 and 2	-	2	
		MSI range 3, Voltage range 3	-	3	
$f_{OVER(MSI)}$	MSI oscillator frequency overshoot	Any range to range 5	-	4	MHz
		Any range to range 6	-	6	

1. This is a deviation for an individual part, once the initial frequency has been measured.

2. Guaranteed by characterization results.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 49. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. frequency range at 32 MHz	Unit
S _{EMI}	Peak level	V _{DD} = 3.6 V, T _A = 25 °C, compliant with IEC 61967-2	0.1 to 30 MHz	-7	dBμV
			30 to 130 MHz	14	
			130 MHz to 1 GHz	9	
			EMI Level	2	-

6.3.11 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the ANSI/JEDEC standard.

Table 50. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value ⁽¹⁾	Unit
$V_{\text{ESD(HBM)}}$	Electrostatic discharge voltage (human body model)	$T_A = +25\text{ °C}$, conforming to ANSI/JEDEC JS-001	2	2000	V
$V_{\text{ESD(CDM)}}$	Electrostatic discharge voltage (charge device model)	$T_A = +25\text{ °C}$, conforming to ANSI/ESD STM5.3.1.	C4	500	

1. Guaranteed by characterization results.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 51. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	$T_A = +125\text{ °C}$ conforming to JESD78A	II level A

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in [Figure 23](#) and [Table 55](#), respectively.

Unless otherwise specified, the parameters given in [Table 55](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 20](#).

Table 55. I/O AC characteristics⁽¹⁾

OSPEEDRx[1:0] bit value ⁽¹⁾	Symbol	Parameter	Conditions	Min	Max ⁽²⁾	Unit
00	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽³⁾	$C_L = 50 \text{ pF}$, $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	400	kHz
			$C_L = 50 \text{ pF}$, $V_{DD} = 1.65 \text{ V to } 2.7 \text{ V}$	-	100	
	$t_{f(\text{IO})\text{out}}$ $t_{r(\text{IO})\text{out}}$	Output rise and fall time	$C_L = 50 \text{ pF}$, $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	125	ns
			$C_L = 50 \text{ pF}$, $V_{DD} = 1.65 \text{ V to } 2.7 \text{ V}$	-	320	
01	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽³⁾	$C_L = 50 \text{ pF}$, $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	2	MHz
			$C_L = 50 \text{ pF}$, $V_{DD} = 1.65 \text{ V to } 2.7 \text{ V}$	-	0.6	
	$t_{f(\text{IO})\text{out}}$ $t_{r(\text{IO})\text{out}}$	Output rise and fall time	$C_L = 50 \text{ pF}$, $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	30	ns
			$C_L = 50 \text{ pF}$, $V_{DD} = 1.65 \text{ V to } 2.7 \text{ V}$	-	65	
10	$F_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽³⁾	$C_L = 50 \text{ pF}$, $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	10	MHz
			$C_L = 50 \text{ pF}$, $V_{DD} = 1.65 \text{ V to } 2.7 \text{ V}$	-	2	
	$t_{f(\text{IO})\text{out}}$ $t_{r(\text{IO})\text{out}}$	Output rise and fall time	$C_L = 50 \text{ pF}$, $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	13	ns
			$C_L = 50 \text{ pF}$, $V_{DD} = 1.65 \text{ V to } 2.7 \text{ V}$	-	28	
11	$F_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽³⁾	$C_L = 30 \text{ pF}$, $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	35	MHz
			$C_L = 50 \text{ pF}$, $V_{DD} = 1.65 \text{ V to } 2.7 \text{ V}$	-	10	
	$t_{f(\text{IO})\text{out}}$ $t_{r(\text{IO})\text{out}}$	Output rise and fall time	$C_L = 30 \text{ pF}$, $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	6	ns
			$C_L = 50 \text{ pF}$, $V_{DD} = 1.65 \text{ V to } 2.7 \text{ V}$	-	17	
Fm+ configuration ⁽⁴⁾	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽³⁾	$C_L = 50 \text{ pF}$, $V_{DD} = 2.5 \text{ V to } 3.6 \text{ V}$	-	1	MHz
	$t_{f(\text{IO})\text{out}}$	Output fall time		-	10	ns
	$t_{r(\text{IO})\text{out}}$	Output rise time		-	30	
	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽³⁾	$C_L = 50 \text{ pF}$, $V_{DD} = 1.65 \text{ V to } 3.6 \text{ V}$	-	350	KHz
	$t_{f(\text{IO})\text{out}}$	Output fall time		-	15	ns
	$t_{r(\text{IO})\text{out}}$	Output rise time		-	60	
-	$t_{\text{EXTI}pw}$	Pulse width of external signals detected by the EXTI controller	-	8	-	ns

1. The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the line reference manual for a description of GPIO Port configuration register.
2. Guaranteed by design.
3. The maximum frequency is defined in [Figure 23](#).
4. When Fm+ configuration is set, the I/O speed control is bypassed. Refer to the line reference manual for a detailed description of Fm+ I/O configuration.

Table 57. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{CAL}^{(3)(5)}$	Calibration time	$f_{ADC} = 16 \text{ MHz}$	5.2			μs
		-	83			$1/f_{ADC}$
$W_{LATENCY}^{(6)}$	ADC_DR register write latency	ADC clock = HSI16	1.5 ADC cycles + 2 f_{PCLK} cycles	-	1.5 ADC cycles + 3 f_{PCLK} cycles	-
		ADC clock = PCLK/2	-	4.5	-	f_{PCLK} cycle
		ADC clock = PCLK/4	-	8.5	-	f_{PCLK} cycle
$t_{latr}^{(3)}$	Trigger conversion latency	$f_{ADC} = f_{PCLK}/2 = 16 \text{ MHz}$	0.266			μs
		$f_{ADC} = f_{PCLK}/2$	8.5			$1/f_{PCLK}$
		$f_{ADC} = f_{PCLK}/4 = 8 \text{ MHz}$	0.516			μs
		$f_{ADC} = f_{PCLK}/4$	16.5			$1/f_{PCLK}$
		$f_{ADC} = f_{HSI16} = 16 \text{ MHz}$	0.252	-	0.260	μs
Jitter _{ADC}	ADC jitter on trigger conversion	$f_{ADC} = f_{HSI16}$	-	1	-	$1/f_{HSI16}$
$t_S^{(3)}$	Sampling time	$f_{ADC} = 16 \text{ MHz}$	0.093	-	10.03	μs
		-	1.5	-	160.5	$1/f_{ADC}$
$t_{UP_LDO}^{(3)(5)}$	Internal LDO power-up time	-	-	-	10	μs
$t_{STAB}^{(3)(5)}$	ADC stabilization time	-	14			$1/f_{ADC}$
$t_{ConV}^{(3)}$	Total conversion time (including sampling time)	$f_{ADC} = 16 \text{ MHz}$, 12-bit resolution	0.875	-	10.81	μs
		12-bit resolution	14 to 173 (t_S for sampling +12.5 for successive approximation)			$1/f_{ADC}$

- V_{DDA} minimum value can be decreased in specific temperature conditions. Refer to [Table 58: RAIN max for \$f_{ADC} = 16 \text{ MHz}\$](#) .
- A current consumption proportional to the APB clock frequency has to be added (see [Table 34: Peripheral current consumption in Run or Sleep mode](#)).
- Guaranteed by design.
- Standard channels have an extra protection resistance which depends on supply voltage. Refer to [Table 58: RAIN max for \$f_{ADC} = 16 \text{ MHz}\$](#) .
- This parameter only includes the ADC timing. It does not take into account register access latency.
- This parameter specifies the latency to transfer the conversion result into the ADC_DR register. EOC bit is set to indicate the conversion is complete and has the same latency.

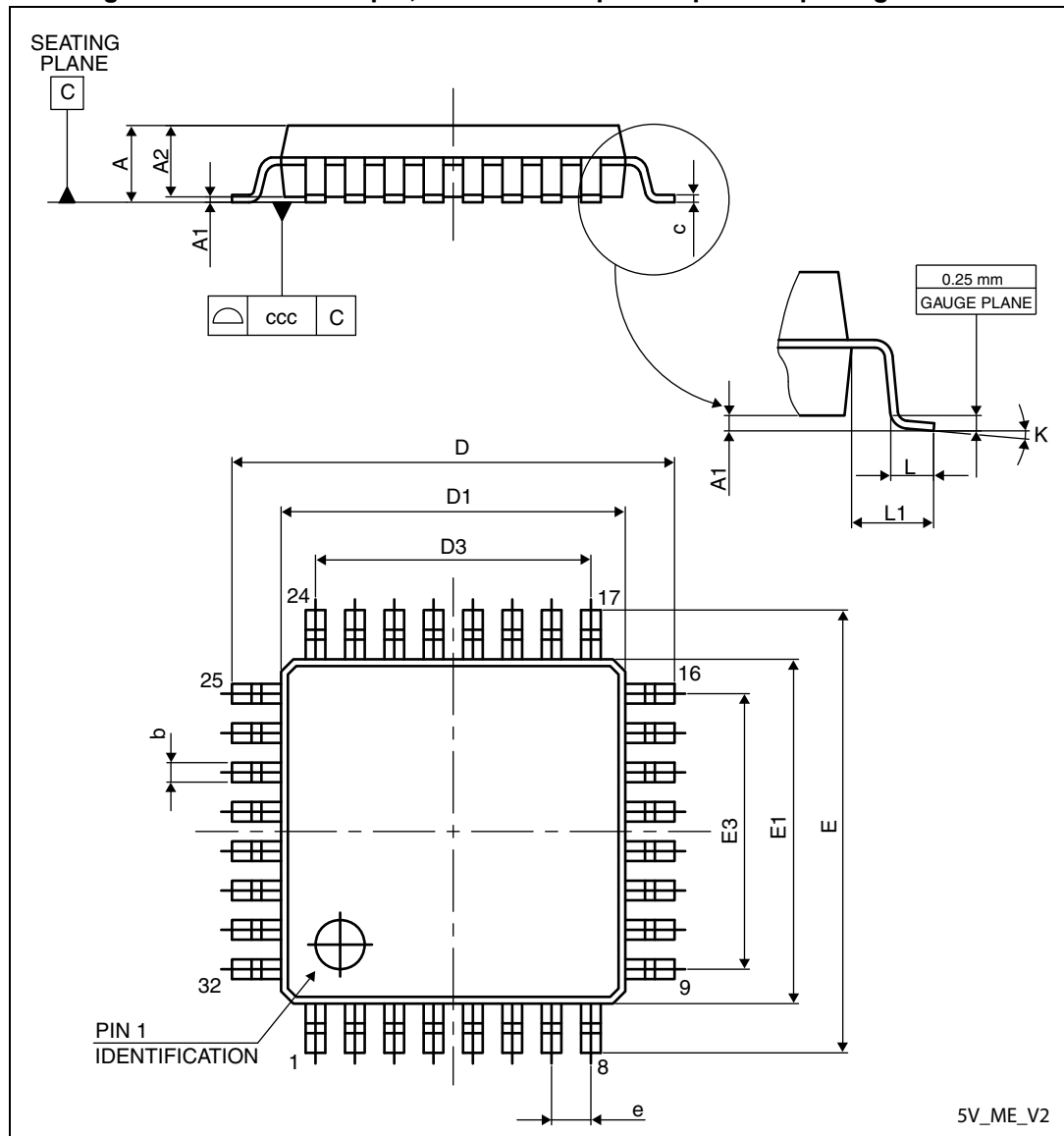
Equation 1: R_{AIN} max formula

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The simplified formula above ([Equation 1](#)) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

7.2 LQFP32 package information

Figure 34. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package outline



1. Drawing is not to scale.

7.4.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.

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