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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	52MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	DMA, PWM, WDT
Number of I/O	51
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.74V ~ 3.6V
Data Converters	A/D 8x12b SAR
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	72-UFBGA, WLCSP
Supplier Device Package	72-WLCSP (3.57x3.16)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aducm4050bcbz-rl

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REVISION HISTORY

6/2018—Revision 0: Initial Version

GENERAL DESCRIPTION

The ADuCM4050 microcontroller unit (MCU) is an ultra low power integrated microcontroller system with integrated power management for processing, control, and connectivity. The MCU system is based on the ARM® Cortex®-M4F processor. The MCU also has a collection of digital peripherals, embedded static random access memory (SRAM) and embedded flash memory, and an analog subsystem that provides clocking, reset, and power management capabilities in addition to an analog-to-digital converter (ADC) subsystem.

This data sheet describes the ARM Cortex-M4F core and memory architecture used on the ADuCM4050 MCU. It does not provide detailed programming information about the ARM processor.

The system features include an up to 52 MHz ARM Cortex-M4F processor, 512 kB of embedded flash memory with error correction code (ECC), an optional 4 kB cache for lower active power, and 128 kB system SRAM with parity. The ADuCM4050 features a power management unit (PMU), multilayer advanced microcontroller bus architecture (AMBA) bus matrix, central direct memory access (DMA) controller, and beeper interface.

The ADuCM4050 features cryptographic hardware supporting advanced encryption standard (AES)-128 and AES-256 with secure hash algorithm (SHA)-256 and the following modes: electronic code book (ECB), cipher block chaining (CBC), counter (CTR), and cipher block chaining-message authentication code (CCM/CCM*) modes.

The ADuCM4050 has protected key storage with key wrap/unwrap, and keyed hashed message authentication code (HMAC) with key unwrap.

The ADuCM4050 supports serial port (SPORT), serial peripheral interface (SPI), I^2C, and universal asynchronous receiver/transmitter (UART) peripheral interfaces.

The ADuCM4050 features a real-time clock (RTC), general-purpose and watchdog timers, and programmable general-purpose input/output (GPIO) pins. There is a hardware cyclic redundancy check (CRC) calculator with programmable generator polynomial. The device also features a power on reset (POR) and power supply monitor (PSM), a 12-bit successive approximation register (SAR) ADC, a red/green/blue (RGB) timer for driving RGB LED, and a true random number generator (TRNG).

To support low dynamic and hibernate power management, the ADuCM4050 MCU provides a collection of power modes and features such as dynamic- and software-controlled clock gating and power gating.

For full details on the ADuCM4050 MCU, refer to the ADuCM4050 Ultra Low Power ARM Cortex-M4F MCU with Integrated Power Management Hardware Reference.

PRODUCT HIGHLIGHTS

1. Ultra low power consumption.
2. Robust operation.
3. Full voltage monitoring in deep sleep modes.
4. ECC support on flash.
5. Parity error detection on SRAM memory.
6. Leading edge security.
7. Fast encryption provides read protection to user algorithms.
8. Write protection prevents device reprogramming by unauthorized code.
9. Failure detection of 32 kHz low frequency external crystal oscillator (LFXTAL) via interrupt.
10. SensorStrobe™ for precise time synchronized sampling of external sensors. Works in hibernate mode, resulting in drastic current reduction in system solutions. Current consumption reduces by 10 times when using, for example, the ADXL363 accelerometer. Software intervention is not required after setup. No pulse drift due to software execution.

SPECIFICATIONS

OPERATING CONDITIONS AND ELECTRICAL CHARACTERISTICS

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
EXTERNAL BATTERY SUPPLY VOLTAGE[1, 2]	V_{BAT}	1.74	3.0	3.6	V	
INPUT VOLTAGE						
High Level	V_{IH}	2.5			V	V_{BAT} = 3.6 V
Low Level	V_{IL}			0.45	V	V_{BAT} = 1.74 V
ADC SUPPLY VOLTAGE	V_{BAT_ADC}	1.74	3.0	3.6	V	
OUTPUT VOLTAGE[3]						
High Level	V_{OH}	1.4			V	V_{BAT} = 1.74 V, I_{OH} = −1.0 mA
Low Level	V_{OL}			0.4	V	V_{BAT} = 1.74 V, I_{OL} = 1.0 mA
INPUT CURRENT PULL-UP[4]						
High Level	I_{IHPU}		0.01	0.2	µA	V_{BAT} = 3.6 V, V_{IN} = 3.6 V
Low Level	I_{ILPU}			100	µA	V_{BAT} = 3.6 V, V_{IN} = 0 V
THREE-STATE LEAKAGE CURRENT						
High Level[5]	I_{OZH}		0.01	0.15	µA	V_{BAT} = 3.6 V, V_{IN} = 3.6 V
Pull-Up[6]	I_{OZHPU}			0.30	µA	V_{BAT} = 3.6 V, V_{IN} = 3.6 V
Pull-Down[7]	I_{OZHPD}			100	µA	V_{BAT} = 3.6 V, V_{IN} = 3.6 V
Low Level[5]	I_{OZL}		0.01	0.15	µA	V_{BAT} = 3.6 V, V_{IN} = 0 V
Pull-Up[6]	I_{OZLPU}			100	µA	V_{BAT} = 3.6 V, V_{IN} = 0 V
Pull-Down[7]	I_{OZLPD}			0.15	µA	V_{BAT} = 3.6 V, V_{IN} = 0 V
INPUT CAPACITANCE	C_{IN}		10		pF	T_J = 25°C
V_{BAT} POWER-ON RESET	V_{VBAT_POR}	1.49	1.59	1.64	V	Power-on reset level on V_{BAT}; trip point is detected when battery is decaying[8]
Junction Temperature	T_J	−40		+85	°C	$T_{AMBIENT}$ = −40°C to +85°C

[1] Value applies to VBAT_ANA1, VBAT_ANA2, VBAT_DIG1, and VBAT_DIG2 pins.
[2] Must remain powered (even if the associated function is not used).
[3] Applies to the output and bidirectional pins: P0_00 to P0_15, P1_00 to P1_15, P2_00 to P2_15, and P3_00 to P3_03.
[4] Applies to the $\overline{\text{SYS\_HWRST}}$ input pin with pull-up.
[5] Applies to the three-state pins: P0_00 to P0_05, P0_08 to P0_15, P1_00 to P1_15, P2_00 to P2_15, P3_00 to P3_03.
[6] Applies to the three-state pins with pull-ups: P0_00 to P0_05, P0_07 to P0_15, P1_00 to P1_15, P2_00 to P2_15, and P3_00 to P3_03.
[7] Applies to the P0_06 three-state pin with pull-down.
[8] This specification is valid when the device is powered up; if the battery decays and falls below 1.71 V, power-on reset is detected. For safer operation of the device, adhere to the V_{BAT} specification.

EMBEDDED FLASH SPECIFICATIONS

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FLASH						
Endurance		10,000			Cycles	
Data Retention			10		Years	

POWER SUPPLY CURRENT SPECIFICATIONS

Active Mode

Table 3.

Parameter	Min	Typ[1]	Max[2]	Unit	Test Conditions/Comments
ACTIVE MODE[3]					Current consumption when V_{BAT} = 3.0 V
Buck Enabled		1.27	2.71	mA	Code executing from flash, cache enabled, system peripheral clock (PCLK) disabled, advanced high performance clock (HCLK) = 26 MHz[4]
		1.83	3.28	mA	Code executing from flash, cache disabled, PCLK disabled, HCLK = 26 MHz[4]
		1.40	2.84	mA	Code executing from flash, cache enabled, PCLK = 26 MHz, HCLK = 26 MHz[4]
		1.97	3.41	mA	Code executing from flash, cache disabled, PCLK = 26 MHz, HCLK = 26 MHz[4]
		2.33	3.78	mA	Code executing from flash, cache enabled, PCLK disabled, HCLK = 52 MHz[5]
		2.94	4.39	mA	Code executing from flash, cache disabled, PCLK disabled, HCLK = 52 MHz[5]
		2.59	4.04	mA	Code executing from flash, cache enabled, PCLK = 52 MHz, HCLK = 52 MHz[5]
		3.21	4.65	mA	Code executing from flash, cache disabled, PCLK = 52 MHz, HCLK = 52 MHz[5]
		1.43	2.87	mA	Code executing from SRAM, PCLK disabled, HCLK = 26 MHz[4]
		1.56	3.00	mA	Code executing from SRAM, PCLK = 26 MHz, HCLK = 26 MHz[4]
		2.64	4.09	mA	Code executing from SRAM, PCLK disabled, HCLK = 52 MHz[5]
		2.90	4.35	mA	Code executing from SRAM, PCLK = 52 MHz, HCLK = 52 MHz[5]
Dynamic Current		41		µA/MHz	Code executing from flash, cache enabled
Buck Disabled		2.34	4.78	mA	Code executing from flash, cache enabled, PCLK disabled, HCLK = 26 MHz[4]
		3.38	5.82	mA	Code executing from flash, cache disabled, PCLK disabled, HCLK = 26 MHz[4]
		2.60	5.04	mA	Code executing from flash, cache enabled, PCLK = 26 MHz, HCLK = 26 MHz[4]
		3.65	6.09	mA	Code executing from flash, cache disabled, PCLK = 26 MHz, HCLK = 26 MHz[4]
		4.46	6.90	mA	Code executing from flash, cache enabled, PCLK disabled, HCLK = 52 MHz[5]
		5.61	8.05	mA	Code executing from flash, cache disabled, PCLK disabled, HCLK = 52 MHz[5]
		4.98	7.42	mA	Code executing from flash, cache enabled, PCLK = 52 MHz, HCLK = 52 MHz[5]
		6.14	8.58	mA	Code executing from flash, cache disabled, PCLK = 52 MHz, HCLK = 52 MHz[5]
		2.66	5.10	mA	Code executing from SRAM, PCLK disabled, HCLK = 26 MHz[4]
		2.92	5.36	mA	Code executing from SRAM, PCLK = 26 MHz, HCLK = 26 MHz[4]
		5.08	7.52	mA	Code executing from SRAM, PCLK disabled, HCLK = 52 MHz[5]
		5.60	8.04	mA	Code executing from SRAM, PCLK = 52 MHz, HCLK = 52 MHz[5]
Dynamic Current		82		µA/MHz	Code executing from flash, cache enabled

[1] T_J = 25°C
[2] T_J = 85°C
[3] The code being executed is a prime number generation in a continuous loop, with high frequency RC oscillator (HFOSC) as the system clock source.
[4] Zero wait states and low buck load.
[5] One wait state and high buck load.

Flexi Mode

Table 4.

Parameter	Min	Typ[1]	Max[2]	Unit	Test Conditions/Comments
FLEXI™ MODE					Current consumption when V_{BAT} = 3.0 V
Buck Enabled		0.40	1.85	mA	PCLK disabled, HCLK = 26 MHz
		0.54	1.98	mA	PCLK = 26 MHz, HCLK = 26 MHz
		0.62	2.06	mA	PCLK disabled, HCLK = 52 MHz
		0.88	2.33	mA	PCLK = 52 MHz, HCLK = 52 MHz
Buck Disabled		0.62	3.06	mA	PCLK disabled, HCLK = 26 MHz
		0.88	3.32	mA	PCLK = 26 MHz, HCLK = 26 MHz
		1.04	3.48	mA	PCLK disabled, HCLK = 52 MHz
		1.57	4.01	mA	PCLK = 52 MHz, HCLK = 52 MHz

[1] T_J = 25°C.
[2] T_J = 85°C.

Deep Sleep Modes—V_{BAT} = 3.0 V

Table 6.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
HIBERNATE MODE[1]					V_{BAT} = 3.0 V
T_J = 25°C		0.65		µA	RTC1 and RTC0 disabled, 16 kB SRAM retained, LFXTAL off
		0.72		µA	RTC1 and RTC0 disabled, 28 kB SRAM retained, LFXTAL off
		0.77		µA	RTC1 and RTC0 disabled, 48 kB SRAM retained, LFXTAL off
		0.83		µA	RTC1 and RTC0 disabled, 60 kB SRAM retained, LFXTAL off
		1.09		µA	RTC1 and RTC0 disabled, 80 kB SRAM retained, LFXTAL off
		1.13		µA	RTC1 and RTC0 disabled, 92 kB SRAM retained, LFXTAL off
		1.17		µA	RTC1 and RTC0 disabled, 112 kB SRAM retained, LFXTAL off
		1.22		µA	RTC1 and RTC0 disabled, 124 kB SRAM retained, LFXTAL off
		0.68		µA	RTC1 enabled, 16 kB SRAM retained, LFOSC as RTC1 source
		1.26		µA	RTC1 enabled, 124 kB SRAM retained, LFOSC as RTC1 source
		0.87		µA	RTC1 enabled, 16 kB SRAM retained, LFXTAL as RTC1 source
		0.95		µA	RTC0 enabled, 16 kB SRAM retained, LFXTAL as RTC0 source
		0.97		µA	RTC1 and RTC0 enabled, 16 kB SRAM retained, LFXTAL as RTC1 and RTC0 source
		1.38		µA	RTC1 enabled, 124 kB SRAM retained, LFXTAL as RTC1 source
		1.46		µA	RTC0 enabled, 124 kB SRAM retained, LFXTAL as RTC0 source
		1.48		µA	RTC1 and RTC0 enabled, 124 kB SRAM retained, LFXTAL as RTC1 and RTC0 source
T_J = 85°C		2.00	4.60	µA	RTC1 and RTC0 disabled, 16 kB SRAM retained, LFXTAL off
		2.38	5.70	µA	RTC1 and RTC0 disabled, 28 kB SRAM retained, LFXTAL off
		2.98	7.80	µA	RTC1 and RTC0 disabled, 48 kB SRAM retained, LFXTAL off
		3.29	9.00	µA	RTC1 and RTC0 disabled, 60 kB SRAM retained, LFXTAL off
		4.04	10.06	µA	RTC1 and RTC0 disabled, 80 kB SRAM retained, LFXTAL off
		4.41	11.80	µA	RTC1 and RTC0 disabled, 92 kB SRAM retained, LFXTAL off
		4.94	13.70	µA	RTC1 and RTC0 disabled, 112 kB SRAM retained, LFXTAL off
		5.20	15.50	µA	RTC1 and RTC0 disabled, 124 kB SRAM retained, LFXTAL off
		2.11	5.00	µA	RTC1 enabled, 16 kB SRAM retained, LFOSC as RTC1 source
		5.32	16.00	µA	RTC1 enabled, 124 kB SRAM retained, LFOSC as RTC1 source
		2.53	5.75	µA	RTC1 enabled, 16 kB SRAM retained, LFXTAL as RTC1 source
		2.61	5.92	µA	RTC0 enabled, 16 kB SRAM retained, LFXTAL as RTC0 source
		2.64	5.98	µA	RTC1 and RTC0 enabled, 16 kB SRAM retained, LFXTAL as RTC1 and RTC0 source
		6.03	16.12	µA	RTC1 enabled, 124 kB SRAM retained, LFXTAL as RTC1 source
		6.10	16.30	µA	RTC0 enabled, 124 kB SRAM retained, LFXTAL as RTC0 source
		6.12	16.37	µA	RTC1 and RTC0 enabled, 124 kB SRAM retained, LFXTAL as RTC1 and RTC0 source
SHUTDOWN MODE[1]					V_{BAT} = 3.0 V
T_J = 25°C		0.05		µA	RTC0 disabled
		0.68		µA	RTC0 enabled, LFXTAL as RTC0 source
T_J = 85°C		0.45	1.60	µA	RTC0 disabled
		1.26	4.18	µA	RTC0 enabled, LFXTAL as RTC0 source
FAST SHUTDOWN MODE[1]					V_{BAT} = 3.0 V
T_J = 25°C		0.20		µA	RTC0 disabled
		0.83		µA	RTC0 enabled, LFXTAL as RTC0 source
T_J = 85°C		0.62	1.80	µA	RTC0 disabled
		1.43	4.74	µA	RTC0 enabled, LFXTAL as RTC0 source

[1] Buck enable/disable does not affect power consumption.

ADC SPECIFICATIONS

Table 8.

Parameter[1, 2]	Min	Typ[3]	Max	Unit	Test Conditions/Comments
INTEGRAL NONLINEARITY ERROR					
64-Lead LFCSP		±1.6		LSB	1.8 V (V_{BAT})/1.25 V (internal/external V_{REF}) [4]
64-Lead LFCSP		−1.7 to +1.3		LSB	3.0 V (V_{BAT})/2.5 V (internal/external V_{REF})[4]
72-Ball WLCSP		±1.4		LSB	1.8 V (V_{BAT})/1.25 V (internal/external V_{REF})[4]
DIFFERENTIAL NONLINEARITY ERROR					
64-Lead LFCSP		−0.7 to +1.15		LSB	1.8 V (V_{BAT})/1.25 V (internal/external V_{REF})[4]
64-Lead LFCSP		−0.7 to +1.1		LSB	3.0 V (V_{BAT})/2.5 V (internal/external V_{REF})[4]
72-Ball WLCSP		−0.75 to +1.0		LSB	1.8 V (V_{BAT})/1.25 V (internal/external V_{REF})[4]
OFFSET ERROR					
64-Lead LFCSP		±0.5		LSB	1.8 V (V_{BAT})/1.25 V (external V_{REF})[4]
64-Lead LFCSP		±0.5		LSB	3.0 V (V_{BAT})/2.5 V (external V_{REF})[4]
72-Ball WLCSP		±0.5		LSB	1.8 V (V_{BAT})/1.25 V (external V_{REF})[4]
GAIN ERROR					
64-Lead LFCSP		±2.5		LSB	1.8 V (V_{BAT})/1.25 V (external V_{REF})[4]
64-Lead LFCSP		±0.5		LSB	3.0 V (V_{BAT})/2.5 V (external V_{REF})[4]
72-Ball WLCSP		±3.0		LSB	1.8 V (V_{BAT})/1.25 V (external V_{REF})[4]
I V_{BAT_ADC}[5]					
64-Lead LFCSP		129		µA	1.8 V (V_{BAT})/1.25 V (internal V_{REF})[6]
64-Lead LFCSP		157		µA	3.0 V (V_{BAT})/2.5 V (internal V_{REF})[6]
72-Ball WLCSP		124		µA	1.8 V (V_{BAT})/1.25 V (internal V_{REF}) [6]
64-Lead LFCSP		47		µA	1.8 V (V_{BAT})/1.25 V (external V_{REF})[7]
64-Lead LFCSP		51		µA	3.0 V (V_{BAT})/2.5 V (external V_{REF})[7]
72-Ball WLCSP		46		µA	1.8 V (V_{BAT})/1.25 V (external V_{REF}) [7]
INTERNAL REFERENCE VOLTAGE		1.25		V	Internal reference, 1.25 V selected
		2.50		V	Internal reference, 2.5 V selected
ADC SAMPLING FREQUENCY (f_S)[8]	0.01		1.8	MSPS	

[1] The ADC is characterized in standalone mode without core activity and minimal or no switching on the adjacent ADC channels and digital inputs/outputs.
[2] The specifications are characterized after performing internal ADC offset calibration.
[3] T_J = 25°C.
[4] f_{IN} = 1068 Hz, f_S = 100 kSPS, internal reference in low power mode, 400,000 samples end point method used.
[5] Current consumption from VBAT_ADC supply when ADC is performing the conversion.
[6] f_{IN} = 1068 Hz, f_S = 100 kSPS, internal reference in low power mode.
[7] f_{IN} = 1068 Hz, f_S = 100 kSPS, sine wave with 1.25 V p-p applied at ADC0_VIN1 channel input.
[8] Effects of analog source impedance must be considered when selecting ADC sampling frequency.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

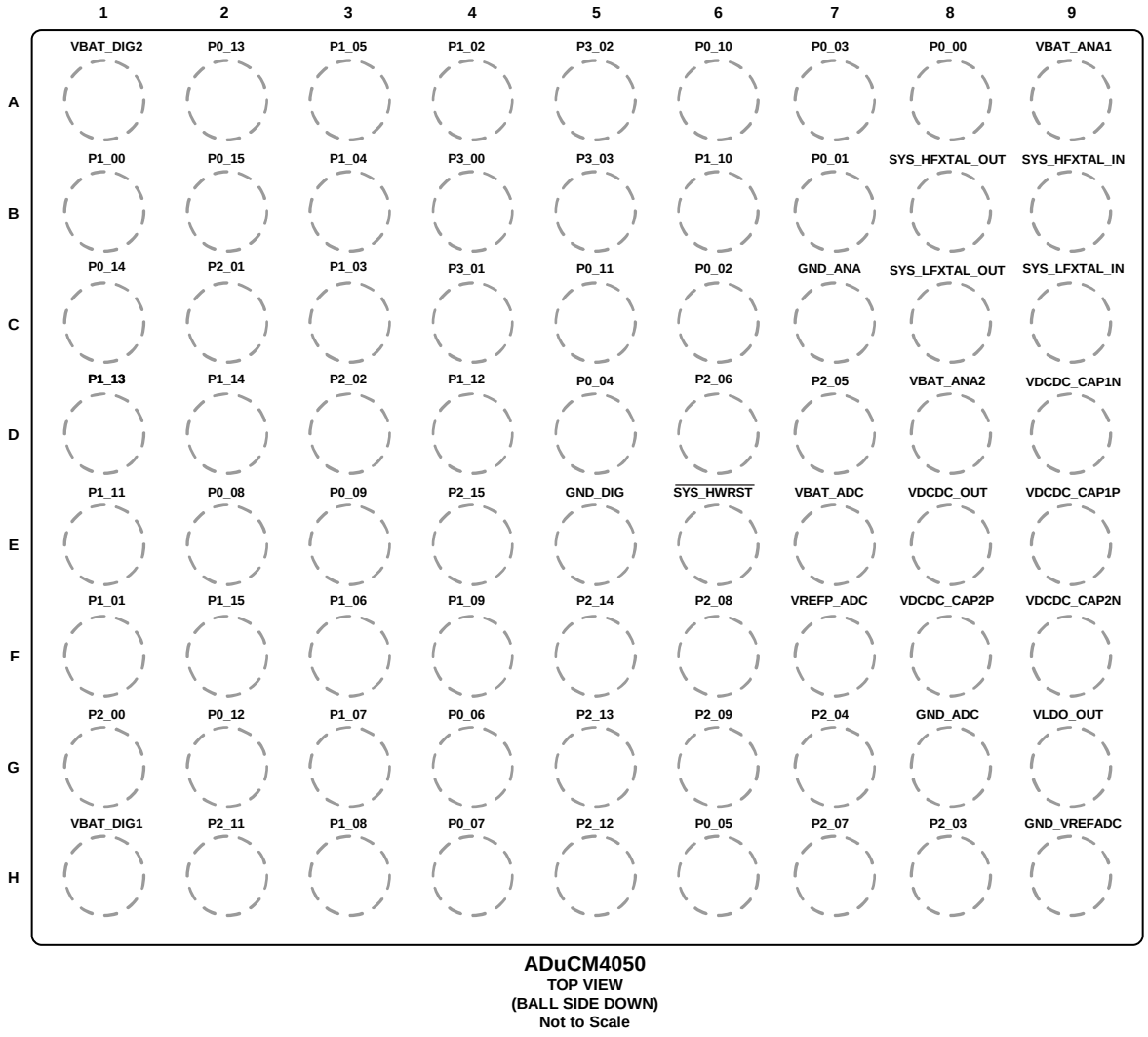

Figure 14. 72-Ball WLCSP Pin Configuration

Table 22. 72-Ball WLCSP Pin Function Descriptions

Pin No.	Mnemonic	Signal Names	Description
A1	VBAT_DIG2	Not applicable	External Supply for Digital Circuits in the MCU.
A2	P0_13	GPIO13/SYS_WAKE2	GPIO. See the GPIO Multiplexing section for more information.
A3	P1_05	GPIO21, SPI2_CS0	GPIO. See the GPIO Multiplexing section for more information.
A4	P1_02	GPIO18, SPI2_CLK	GPIO. See the GPIO Multiplexing section for more information.
A5	P3_02	GPIO50, RGB_TMR0_3, SPT0_AD0	GPIO. See the GPIO Multiplexing section for more information.
A6	P0_10	GPIO10, UART0_TX	GPIO. See the GPIO Multiplexing section for more information.
A7	P0_03	GPIO03, SPI0_CS0, SPT0_BCNV, SPI2_RDY	GPIO. See the GPIO Multiplexing section for more information.
A8	P0_00	GPIO00, SPI0_CLK, SPT0_BCLK	GPIO. See the GPIO Multiplexing section for more information.
A9	VBAT_ANA1	Not applicable	External Supply for Analog Circuits in the MCU.
B1	P1_00	GPIO16/SYS_WAKE1	GPIO. See the GPIO Multiplexing section for more information.
B2	P0_15	GPIO15/SYS_WAKE0	GPIO. See the GPIO Multiplexing section for more information.
B3	P1_04	GPIO20, SPI2_MISO	GPIO. See the GPIO Multiplexing section for more information.
B4	P3_00	GPIO48, RGB_TMR0_1, SPT0_ACLK	GPIO. See the GPIO Multiplexing section for more information.
B5	P3_03	GPIO51, SPT0_ACNV	GPIO. See the GPIO Multiplexing section for more information.

Pin No.	Mnemonic	Signal Names	Description
28	P0_06	SWD0_CLK, GPIO06	GPIO. See the GPIO Multiplexing section for more information.
29	P1_09	GPIO25, SPI1_CS0, SWV	GPIO. See the GPIO Multiplexing section for more information.
30	P1_08	GPIO24, SPI1_MISO, RGB_TMR0_3	GPIO. See the GPIO Multiplexing section for more information.
31	P1_07	GPIO23, SPI1_MOSI, RGB_TMR0_2	GPIO. See the GPIO Multiplexing section for more information.
32	P1_06	GPIO22, SPI1_CLK, RGB_TMR0_1	GPIO. See the GPIO Multiplexing section for more information.
33	P2_11	GPIO43, SPI1_CS1, SYS_CLKOUT, RTC1_SS1	GPIO. See the GPIO Multiplexing section for more information.
34	VBAT_DIG1	Not applicable	External Supply for Digital Circuits in the MCU.
35	P0_12	GPIO12, SPT0_AD0, UART0_SOUT_EN	GPIO. See the GPIO Multiplexing section for more information.
36	P2_00	GPIO32, SPT0_AFS, UART1_RX	GPIO. See the GPIO Multiplexing section for more information.
37	P1_15	GPIO31, SPT0_ACLK, UART1_TX	GPIO. See the GPIO Multiplexing section for more information.
38	P1_01	SYS_BMODE0, GPIO17	GPIO. See the GPIO Multiplexing section for more information.
39	P0_09	GPIO09, BPR0_TONE_P, SPI2_CS1	GPIO. See the GPIO Multiplexing section for more information.
40	P0_08	GPIO08, BPR0_TONE_N	GPIO. See the GPIO Multiplexing section for more information.
41	P1_11	GPIO27, TMR1_OUT	GPIO. See the GPIO Multiplexing section for more information.
42	P1_12	GPIO28, RTC1_SS2	GPIO. See the GPIO Multiplexing section for more information.
43	P1_13	GPIO29, TMR2_OUT	GPIO. See the GPIO Multiplexing section for more information.
44	P1_14	GPIO30, SPI0_RDY	GPIO. See the GPIO Multiplexing section for more information.
45	P2_02	GPIO34, SPT0_ACNV, SPI1_CS2	GPIO. See the GPIO Multiplexing section for more information.
46	P0_14	GPIO14, TMR0_OUT, SPI1_RDY	GPIO. See the GPIO Multiplexing section for more information.
47	P1_00	GPIO16/SYS_WAKE1	GPIO. See the GPIO Multiplexing section for more information.
48	GND_DIG	Not applicable	Ground Reference for Digital Circuits in the MCU.
49	VBAT_DIG2	Not applicable	External Supply for Digital Circuits in the MCU.
50	P0_15	GPIO15/SYS_WAKE0	GPIO. See the GPIO Multiplexing section for more information.
51	P0_13	GPIO13/SYS_WAKE2	GPIO. See the GPIO Multiplexing section for more information.
52	P2_01	GPIO33/SYS_WAKE3, TMR2_OUT	GPIO. See the GPIO Multiplexing section for more information.
53	P1_05	GPIO21, SPI2_CS0	GPIO. See the GPIO Multiplexing section for more information.
54	P1_04	GPIO20, SPI2_MISO	GPIO. See the GPIO Multiplexing section for more information.
55	P1_03	GPIO19, SPI2_MOSI	GPIO. See the GPIO Multiplexing section for more information.
56	P1_02	GPIO18, SPI2_CLK	GPIO. See the GPIO Multiplexing section for more information.
57	P0_11	GPIO11, UART0_RX	GPIO. See the GPIO Multiplexing section for more information.
58	P0_10	GPIO10, UART0_TX	GPIO. See the GPIO Multiplexing section for more information.
59	P1_10	GPIO26, SPI0_CS1, SYS_CLKIN, SPI1_CS3	GPIO. See the GPIO Multiplexing section for more information.
60	P0_03	GPIO03, SPI0_CS0, SPT0_BCNV, SPI2_RDY	GPIO. See the GPIO Multiplexing section for more information.
61	P0_02	GPIO02, SPI0_MISO, SPT0_BD0	GPIO. See the GPIO Multiplexing section for more information.
62	P0_01	GPIO01, SPI0_MOSI, SPT0_BFS	GPIO. See the GPIO Multiplexing section for more information.
63	P0_00	GPIO00, SPI0_CLK, SPT0_BCLK	GPIO. See the GPIO Multiplexing section for more information.
64	GND_ANA	Not applicable	Ground Reference for Analog Circuits in the MCU.
	EPAD	Not applicable	Exposed Pad. The exposed pad must be grounded.

TYPICAL PERFORMANCE CHARACTERISTICS

Figure 16 through Figure 21 show the typical current voltage characteristics for the output drivers of the MCU. The curves represent the current drive capability of the output drivers as a function of output voltage.

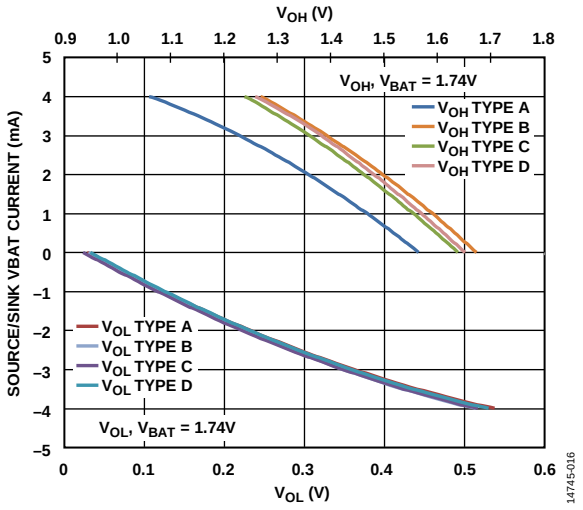

Figure 16. Output Double Drive Strength Characteristics (V_{BAT} = 1.74 V)

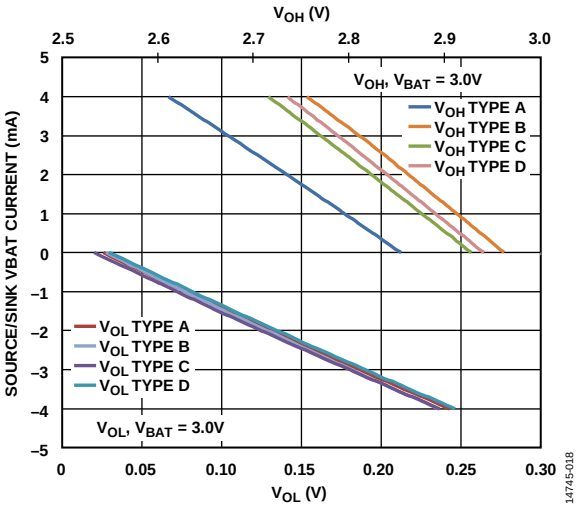

Figure 18. Output Double Drive Strength Characteristics (V_{BAT} = 3.0 V)

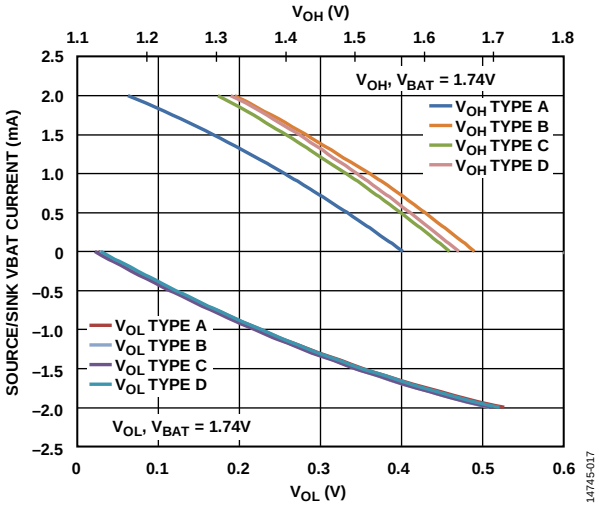

Figure 17. Output Single Drive Strength Characteristics (V_{BAT} = 1.74 V)

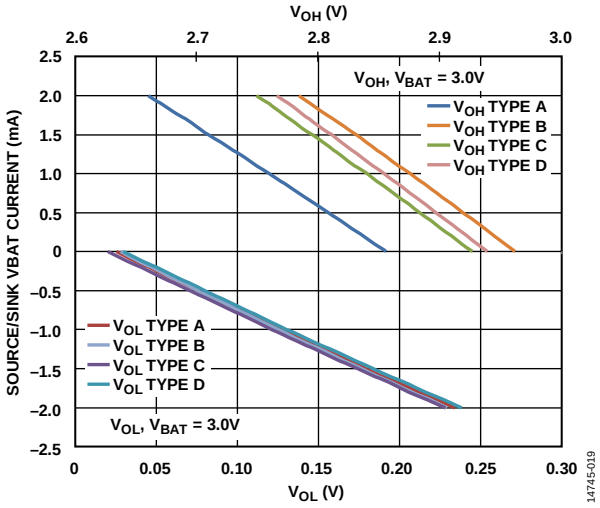

Figure 19. Output Single Drive Strength Characteristics (V_{BAT} = 3.0 V)

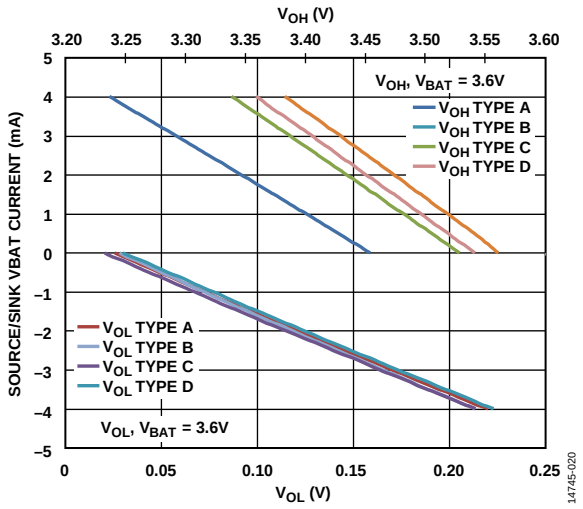

Figure 20. Output Double Drive Strength Characteristics (V_{BAT} = 3.6 V)

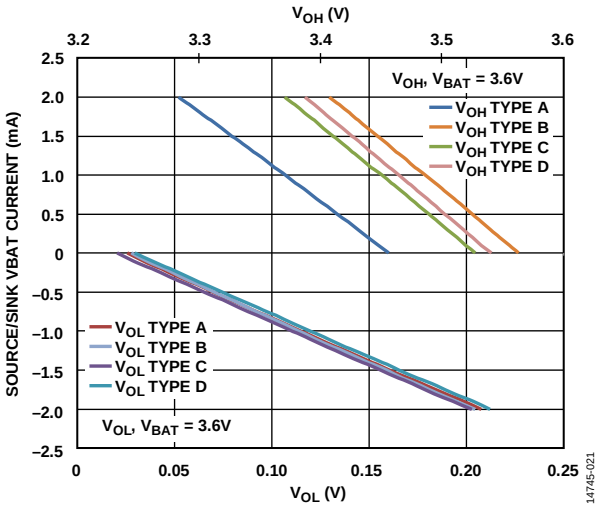

Figure 21. Output Single Drive Strength Characteristics (V_{BAT} = 3.6 V)

THEORY OF OPERATION

ARM CORTEX-M4F PROCESSOR

The ARM Cortex-M4F core is a 32-bit reduced instruction set computer (RISC). The length of the data can be 8 bits, 16 bits, or 32 bits. The length of the instruction word is 16 bits or 32 bits. The processor has the following features:

- ARM Cortex-M4F architecture
- Thumb-2 instruction set architecture (ISA) technology
- Three-stage pipeline with branch speculation
- Low latency interrupt processing with tail chaining
- Single-cycle multiply
- Hardware divide instructions
- Nested vectored interrupt controller (NVIC) (72 interrupts and 8 priorities)
- Six hardware breakpoints and one watchpoint (unlimited software breakpoints using the Segger JLink debug probe)
- Bit banding support
- Trace support—instruction trace macrocell (ITM), trace port interface unit (TPIU), and data watchpoint and trace (DWT) triggers and counters
- Memory protection unit (MPU)
- Eight-region MPU with subregions and background region
- Programmable clock generator unit
- Configurable for ultralow power operation
- Deep sleep modes, dynamic power management
- Programmable clock generator unit
- Floating point unit (FPU)
- Supports single-precision add, subtract, multiply, divide, multiply and accumulate, and square root operations
- Provides conversions between fixed point and floating point data formats, and floating point constant instructions

ARM Cortex-M4F Subsystem

The ADuCM4050 MCU memory map (see the ADuCM4050 Ultra Low Power ARM Cortex-M4F MCU with Integrated Power Management Hardware Reference) is based on the ARM Cortex-M4F memory model. By retaining the standardized memory mapping, it is easier to port applications across ARM Cortex-M4F platforms. The ADuCM4050 application development is based on memory blocks across code and SRAM regions. Sufficient internal memory is available via internal SRAM and internal flash.

Code Region

Accesses in the code region (0x0000_0000 to 0x0007_FFFF except 0x0007_F000 to 0x0007_FFFF, which is meant for protected key storage) are performed by the core and target the memory and cache resources.

SRAM Region

Accesses in the SRAM region (see Figure 22) are performed by the ARM Cortex-M4F core. The SRAM region of the core can act as a data region for an application.

- Internal SRAM data region. This space can contain read/write data. Internal SRAM can be partitioned between code and data (the SRAM region in the ARM Cortex-M4F space) in 32 kB blocks. Access to this region occurs at core clock speed with no wait states. The SRAM data region also supports read/write access by the ARM Cortex-M4F core and read/write DMA access by system devices.
- System memory mapped registers (MMRs). Various system MMRs reside in this region.

System Region

Accesses in this region (0xE000_0000 to 0xFFFF_FFFF) are performed by the ARM Cortex-M4F core and handled within the ARM Cortex-M4F platform. This system region includes the following components:

- CoreSight™ read only memory (ROM). The ROM table entries (see the ARM Cortex-M4F Technical Reference Manual) show the debug components of the processor.
- ARM advanced peripheral bus (APB) peripheral. This space is defined by ARM and occupies the bottom 256 kB of the system region (0xE000_0000 to 0xE004_0000). The space supports read/write access by the ARM Cortex-M4F core to the internal peripherals of the ARM core (NVIC, system control space (SCS), and wake-up interrupt controller (WIC)) and CoreSight ROM. It is not accessible by system DMA.
- Platform control register. This space has registers within the ARM Cortex-M4F platform component that control the ARM core, its memory, and the code cache. It is accessible by the ARM Cortex-M4F core (but not accessible by system DMA).

MEMORY ARCHITECTURE

The internal memory of the ADuCM4050 MCU is shown in Figure 22. It incorporates 512 kB of embedded flash memory for program code and nonvolatile data storage, 96 kB of data SRAM, and 32 kB of SRAM (configured as instruction space or data space).

SRAM Region

This memory space contains the application instructions and variables data, which must be accessed in real time. It supports read/write access by the ARM Cortex-M4F core and read/write DMA access by system peripherals. Byte, half-word and word accesses are supported.

SRAM is divided into 96 kB data SRAM and 32 kB instruction SRAM. If instruction SRAM is not enabled, then the associated 32 kB can be mapped as data SRAM, resulting in 128 kB of data SRAM.

When the cache controller is enabled, 4 kB of the instruction SRAM is reserved as cache memory. Optional parity bit error detection is available on all SRAM memories. Multiple parity bits are associated with each 32-bit word.

In hibernate mode, up to 124 kB of SRAM can be retained in the following ways:

- 124 kB of data SRAM
- 96 kB of data SRAM and 28 kB of instruction SRAM

MMRs (Peripheral Control and Status)

For the address space containing MMRs, refer to Figure 22. These registers provide control and status for on-chip peripherals of the ADuCM4050 MCU.

For more information about the MMRs, refer to the ADuCM4050 Ultra Low Power ARM Cortex-M4F MCU with Integrated Power Management Hardware Reference.

Flash Memory

The ADuCM4050 MCU includes 512 kB of embedded flash memory, which is accessed using a flash controller. The flash controller is coupled with a cache controller. A prefetch mechanism is implemented in the flash controller to optimize code performance.

Flash writes are supported by a keyhole mechanism via APB writes to MMRs. The flash controller provides support for DMA-based keyhole writes.

The device supports the following with consideration to flash integrity:

- A fixed user key required for running protected commands, including mass erase and page erase.
- An optional and user definable user failure analysis key (FAA key).
- An optional and user definable write protection for user-accessible memory.
- 8-bit ECC.

Cache Controller

The ADuCM4050 MCU has an optional 4 kB instruction cache. In certain applications, enabling the cache and executing the code can result in lower power consumption rather than operating directly from flash. When enabling the cache controller, 4 kB of instruction SRAM is reserved as cache memory. In hibernate mode, the cache memory is not retained.

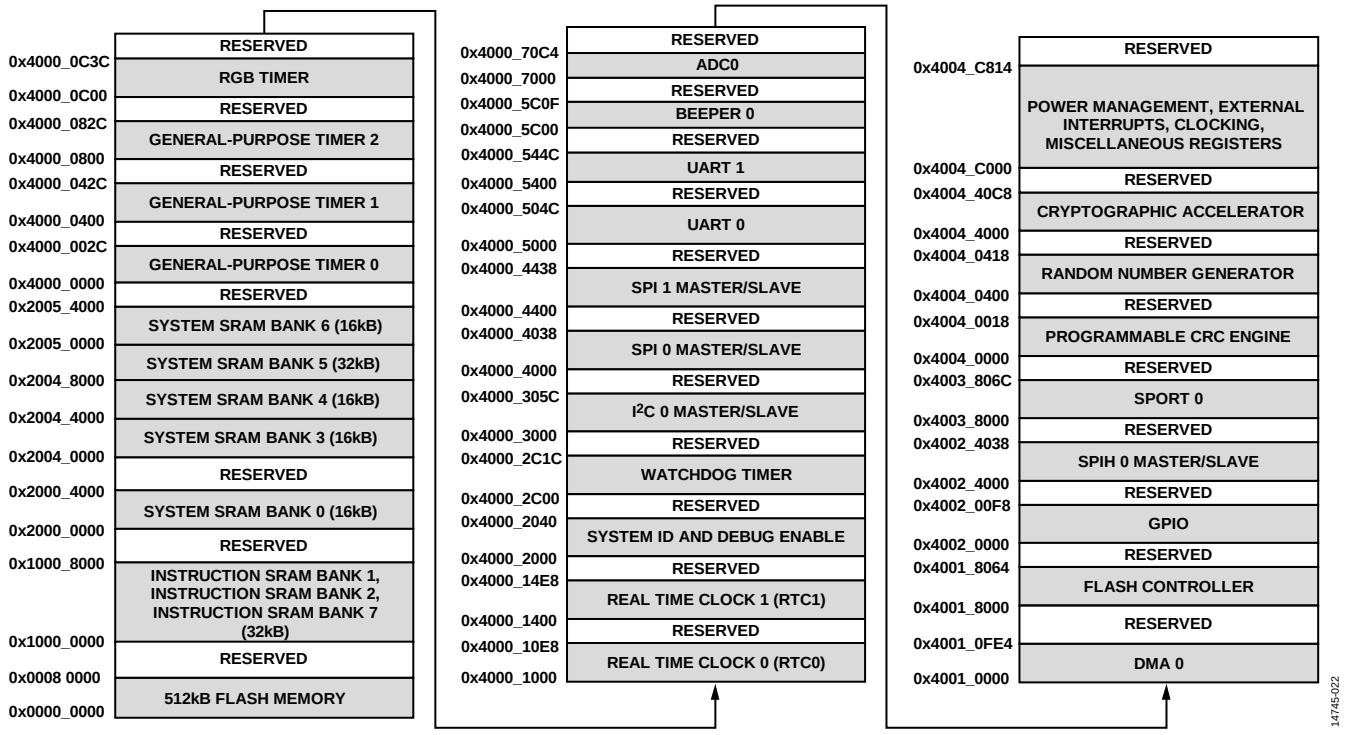

Figure 22. ADuCM4050 Memory Map—SRAM Mode 0

SYSTEM INTEGRATION FEATURES

The ADuCM4050 MCU provides several features for development of ultra low power, secure, and robust systems.

Reset

There are four kinds of resets: external, power-on, watchdog timeout, and software system reset. The software system reset is provided as part of the ARM Cortex-M4F core. The SYS_HWRST pin is toggled to perform a hardware reset.

Booting

The ADuCM4050 MCU supports two boot modes: booting from internal flash and upgrading software through UART download (see Table 24). If SYS_BMODE0 (Pin P1_01) is pulled low during power-up or a hard reset, the MCU enters into serial download mode. In this mode, an on-chip loader routine initiates in the kernel, which configures the UART port and communicates with the host to manage the firmware upgrade via a specific serial download protocol.

Table 24. Boot Modes

Boot Mode	Description
0	UART download mode.
1	Flash boot. Boot from integrated flash memory.

Power Management and Modes

The ADuCM4050 MCU has an integrated power management system that optimizes performance and extends the battery life of the device. The power management system consists of the following:

- Integrated 1.2 V low dropout regulator (LDO) and optional capacitive buck regulator
- Integrated power switches for low standby current in hibernate and shutdown modes

Additional power management features include the following:

- Customized clock gating for active modes
- Power gating to reduce leakage in hibernate and shutdown modes
- Flexible sleep modes
- Shutdown mode with no retention
- Optional high efficiency buck converter to reduce power
- Integrated low power oscillators

The PMU provides control of the ADuCM4050 MCU power modes and allows the ARM Cortex-M4F to control the clocks and power gating to reduce the power consumption. Several power modes are available, offering options to balance power consumption and functionality. The power modes available in the ADuCM4050 are described in the following sections.

Active Mode

In active mode, all peripherals can be enabled. Active power is managed by optimized clock management. See Table 3 for details on active mode current consumption.

Flexi Mode

In flexi mode, the ARM Cortex-M4F core is clock gated, but the remainder of the system is active. No instructions can be executed in this mode, but DMA transfers can continue between peripherals as well as memory to memory. See Table 4 for details on flexi mode current consumption.

Hibernate Mode

Hibernate mode provides state retention, configurable SRAM and port pin retention, a limited number of wake-up interrupts (SYS_WAKEx, UART0_RX, and optionally, RTC0 and RTC1 (FLEX_RTC™)).

Shutdown Mode

Shutdown mode is the deepest sleep mode, in which all the digital and analog circuits are powered down with an option to wake from four possible wake-up sources. The RTC0 can be (optionally) enabled in this mode, and the device can be periodically woken up by the RTC0 interrupt.

Shutdown Mode—Fast Wake-Up

This mode has a faster wake-up time than shutdown mode at the expense of higher power consumption. See Table 25 for wake-up time specifications.

Power Management and Control

The following features are available for power management and control:

- Voltage range of 1.74 V to 3.6 V using a single supply (such as the CR2032 coin cell battery).
- GPIOs are driven directly from the battery. The pin state is retained in hibernate and shutdown modes. The GPIO configuration is only retained in hibernate mode.
- Wake-up from external interrupts (via GPIOs), UART0_RX interrupt, and RTCs for hibernate mode.
- Wake-up from external interrupts (via GPIOs) and RTC0 for shutdown mode.
- Optional high power buck converter for 1.2 V full on support (MCU use only). See Figure 23 for suggested external circuitry.

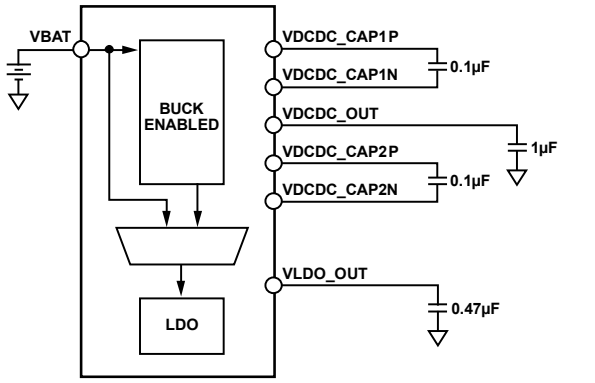

Figure 23. Buck Enable Design

CRC Accelerator

The CRC accelerator computes the CRC for a block of memory locations, that can be in the SRAM, flash, or any combination of MMRs. The CRC accelerator generates a checksum that can be compared with an expected signature. The main features of the CRC include the following:

- Generates a CRC signature for a block of data.
- Supports programmable polynomial length of up to 32 bits.
- Operates on 32 bits of data at a time, and generates CRC for any data length.
- Supports MSB first and LSB first CRC implementations.
- Various data mirroring capabilities.
- Initial seed to be programmed by user.
- DMA controller (memory to memory transfer) used for data transfer to offload the MCU.

Programmable GPIOs

The ADuCM4050 MCU has 44 and 51 GPIO pins in the LFCSP and WLCSP packages, respectively, with multiple, configurable functions defined by user code. They can be configured as input/output pins and have programmable pull-up resistors. All GPIO pins are functional over the full supply range. In deep sleep modes, GPIO pins retain their state. On reset, they tristate.

Timers

The ADuCM4050 MCU contains three general-purpose timers, a watchdog timer, and an RGB timer. All timers support event capture feature, where they can take 40 different interrupts.

General-Purpose Timers

The ADuCM4050 MCU has three identical general-purpose timers, each with a 16-bit up or down counter. The up or down counter can be clocked from one of four user-selectable clock sources. Any selected clock source can be scaled down using a prescaler of 1, 16, 64, or 256.

Watchdog Timer (WDT)

The watchdog timer (WDT) is a 16-bit count down timer with a programmable prescaler. The prescaler source is selectable and can be scaled by a factor of 1, 16, or 256. The WDT is clocked by the 32 kHz on-chip oscillator (LFOSC) and helps recover from an illegal software state. The WDT requires periodic servicing to prevent it from forcing a reset or interrupt to the MCU.

RGB Timer

The ADuCM4050 MCU has an RGB timer that supports a common anode RGB LED. It has a timer counter and three compare registers. It can generate three distinct pulse width modulation (PWM) waveforms on three GPIO pins simultaneously so different colors can be realized using a common anode RGB LED.

When the RGB timer is in operation, the other three timers are available for user software.

ADC Subsystem

The ADuCM4050 MCU integrates a 12-bit SAR ADC with up to eight external channels. Conversions can be performed in single or autocycle mode. In single mode, the ADC can be configured to convert on a particular channel by selecting one of the ADC channels. Autocycle mode is provided to convert over multiple channels with reduced MCU overhead of sampling and reading individual channel registers. The ADC can also be used for temperature sensing and measuring battery voltage using the ADC channels.

Temperature sensing and battery monitoring cannot be included in autocycle mode.

The digital comparator on the device allows an interrupt to be triggered if ADC input is above or below a programmable threshold. Use the following GPIO multiplexed channels with the digital comparator (see the GPIO Multiplexing section): ADC0_VIN0, ADC0_VIN1, ADC0_VIN2, and ADC0_VIN3.

Use the ADC in DMA mode to reduce MCU overhead by moving ADC results directly into SRAM with a single interrupt asserted when the required number of ADC conversions completely logs to memory. The main features of the ADC subsystem include the following:

- 12-bit resolution.
- Programmable ADC update rate from 10 kSPS to 1.8 MSPS.
- Integrated input mux that supports up to eight channels.
- Temperature sensing support.
- Battery monitoring support.
- Software selectable on-chip reference voltage generation—1.25 V or 2.50 V.
- Software-selectable internal or external reference.
- Autocycle mode provides the ability to automatically select a sequence of input channels for conversion.
- Multiple conversions over a single channel or multiple channels can be performed without core interruption.
- Averaging function—converted data on a single channel or multiple channels can be averaged up to 256 samples.
- Alert function that contains an internal digital comparator for the ADC0_VIN0, ADC0_VIN1, ADC0_VIN2, and ADC0_VIN3 channels. An interrupt is generated if the digital comparator detects an ADC result above or below a user defined threshold. In addition, up to eight cycles of hysteresis are built in.
- Dedicated DMA channel support.
- Each channel, including temperature sensor and battery monitoring, has a data register for conversion result.

Table 26. RTC Features

Features	RTC0	RTC1 (FLEX_RTC)
Resolution of Time Base (Prescaling)	Counts time at 1 Hz in units of seconds. Operationally, RTC0 always prescales to 1 Hz (for example, divide by 32,768) and always counts real time in units of seconds.	Can prescale the clock by any power of two from 0 to 15. It can count time in units of any of these 16 possible prescale settings. For example, the clock can be prescaled by 1, 2, 4, 8, …, 16,384, or 32,768.
Source Clock	LFXTAL.	Depending on the low frequency multiplexer configuration, the RTC is clocked by the LFXTAL or the LFOSC.
Wake-Up Timer	Wake-up time is specified in units of seconds.	Supports alarm times down to a resolution of 30.52 µs, that is, where the time is specified down to a specific 32 kHz clock cycle.
Number of Alarms	One alarm only. Uses an absolute, nonrepeating alarm time, specified in units of 1 sec.	Two alarms. One absolute alarm time and one periodic alarm, repeating every 60 prescaled time units.
SensorStrobe Mechanism	Not available.	Four independent channels with fine control on duty cycle and frequency (0.5 Hz to 16.384 kHz). SensorStrobe is an alarm function in the RTC that can send an output pulse via GPIOs to an external device to instruct that device to take a measurement or perform some action at a specific time. SensorStrobe events are scheduled at a specific target time relative to the real-time count of the RTC. SensorStrobe can be enabled in active, flexi, and hibernate modes.
Input Capture	Not available.	Input capture takes a snapshot of the RTC real-time count when an external device signals an event via a transition on one of the GPIO inputs to the ADuCM4050 MCU. Typically, an input capture event is triggered by an autonomous measurement or action on such a device, which then signals to the ADuCM4050 MCU that the RTC must take a snapshot of time corresponding to the event. Taking this snapshot can wake up the ADuCM4050 MCU and cause an interrupt to the CPU. The CPU can subsequently obtain information from the RTC on the exact 32 kHz cycle on which the input capture event occurred.
Input Sampling	Not available.	Each SensorStrobe channel has up to three separate GPIO inputs from an external device, which can be sampled based on the output pulse sent to the external device. Each channel can be configured to interrupt the ADuCM4050 MCU when any activity happens on these GPIO inputs from the external device. These inputs can broadcast sensor states such as first in, first out (FIFO) buffer full, switch open, and threshold crossed. This feature allows the ADuCM4050 MCU to remain in a low power state and wake up to process the data only when a specific programmed sequence from an external device is detected.

EEMBC ULPMARK™-CP SCORE

Using the following software configuration and the profile configuration shown in Table 28, the EEMBC ULPMark-CP score is 189.

- Compiler name and version: IAR EWARM 8.20.1
- Compiler flags:

```
--no_size_constraints --cpu=Cortex-M4 -D
__ADUCM4050__ --no_code_motion -Ohs -e --
fpu=VFPv4_sp --endian=little
```

- ULPBench Profile and Version: Core Profile v1.1
- EnergyMonitor Software Version: V2.0

Table 28. EEMBC ULPMark™-CP Profile Configuration

Profile Configuration	Value
Wake-Up Timer Module	RTC1
Wake-Up Timer Clock Source	External crystal
Wake-Up Timer Frequency	32768 Hz
Wake-Up Timer Accuracy	20 ppm
Active Power Mode Name	Active mode
Active Mode Clock Configuration	52 MHz (CPU), 32 kHz (RTC)
Active Mode Voltage Integrity	1.74 V
Inactive Power Mode Name	Hibernate
Inactive Clock Configuration	Off (CPU), 32 kHz (RTC)
Inactive Mode Voltage Integrity	1.74 V

Table 31. Signal Multiplexing for Port 2

Pin	Availability		Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3
	WLCSP	LFCSP				
P2_00	Yes	Yes	GPIO32	SPT0_AFS	UART1_RX	Not applicable
P2_01	Yes	Yes	GPIO33/SYS_WAKE3	Not applicable	TMR2_OUT	Not applicable
P2_02	Yes	Yes	GPIO34	SPT0_ACNV	SPI1_CS2	Not applicable
P2_03	Yes	Yes	GPIO35	ADC0_VIN0	Not applicable	Not applicable
P2_04	Yes	Yes	GPIO36	ADC0_VIN1	Not applicable	Not applicable
P2_05	Yes	Yes	GPIO37	ADC0_VIN2	Not applicable	Not applicable
P2_06	Yes	Yes	GPIO38	ADC0_VIN3	Not applicable	Not applicable
P2_07	Yes	Yes	GPIO39	ADC0_VIN4	SPI2_CS3	Not applicable
P2_08	Yes	Yes	GPIO40	ADC0_VIN5	SPI0_CS2	RTC1_SS3
P2_09	Yes	Yes	GPIO41	ADC0_VIN6	SPI0_CS3	Not applicable
P2_10	No	Yes	GPIO42	ADC0_VIN7	SPI2_CS2	Not applicable
P2_11	Yes	Yes	GPIO43	SPI1_CS1	SYS_CLKOUT	RTC1_SS1
P2_12	Yes	No	GPIO44	UART1_TX	SPI2_CS3	Not applicable
P2_13	Yes	No	GPIO45	UART1_RX	SPI0_CS2	Not applicable
P2_14	Yes	No	GPIO46	SPI0_CS3	Not applicable	Not applicable
P2_15	Yes	No	GPIO47	SPI2_CS2	SPI1_CS3	SPI0_CS1

Table 32. Signal Multiplexing for Port 3[1]

Pin	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3
P3_00	GPIO48	RGB_TMR0_1	SPT0_ACLK	Not applicable
P3_01	GPIO49	RGB_TMR0_2	SPT0_AFS	Not applicable
P3_02	GPIO50	RGB_TMR0_3	SPT0_AD0	Not applicable
P3_03	GPIO51	Not applicable	SPT0_ACNV	Not applicable

[1] Only available in WLCSP.

SILICON ANOMALY

This anomaly list describes the known bugs, anomalies, and workarounds for the ADuCM4050. These anomalies represent the currently known differences between revisions of the ADuCM4050 product and the functionality specified in the ADuCM4050 data sheet and the hardware reference manual.

Analog Devices, Inc., is committed, through future silicon revisions, to continuously improve silicon functionality. Analog Devices tries to ensure that these future silicon revisions remain compatible with your present software/systems by implementing the recommended workarounds outlined here.

ADuCM4050 FUNCTIONALITY ISSUES

Silicon Revision Identifier	Silicon Status	No. of Reported Anomalies
0.1	Released	3 (21000011, 21000016, 21000017)

A silicon revision number with the form x.y is branded on all devices. The silicon revision can be electronically determined by reading Bits[3:0] of the SYS_CHIPID register. SYS_CHIPID = 0x1 indicates Silicon Revision 0.1, and SYS_CHIPID = 0x0 indicates Silicon Revision 0.0.

FUNCTIONALITY ISSUES

Table 33. 21000011—I²C Master Mode Fails to Generate Clock when Clock Dividers are Too Small

Issue	When the I²C clock dividers are configured in master mode such that the sum of the low and high bit fields in the I2C_DIV register is less than 16, the I²C fails to generate a clock.
Workaround	Program the I²C clock dividers such that I2C_DIV.LOW + I2C_DIV.HIGH ≥ 16.
Revision	0.1

Table 34. 21000016—Possible Receive Data Loss with I²C Automatic Clock Stretching

Issue	When the I²C Rx FIFO is full and new I²C data is received, a data overflow occurs. When automatic clock stretching is enabled, the transaction is paused by holding the SCL (Pin P0_04) line low. This function works as expected when the next read happens after the clock is stretched (that is, after the overflow is detected). However, if the read occurs after the last bit of the I²C data is received but before the clock is stretched, the received data is not written to the Rx FIFO and is lost.
Workaround	When I²C automatic clock stretching is enabled, read the FIFO should only after the overflow flag is set in the status register to ensure that that Rx FIFO is never read at the same time that the overflow is asserted.
Revision	0.1

Table 35. 21000017—SPI Read Command Mode Does Not Work Properly when SPI_CNT is 1 and DMA is Enabled

Issue	When SPI master is enabled and uses the DMA mode with SPI_CNT = 1, the read command mode may not function properly. Consider the following configurations: SPI_RD_CTL = 0x07; SPI_CNT = 1; the transmit and receive DMA channels are configured for 1 half-word. In this configuration, the read command sent in the first byte on the MOSI output is repeated in the second byte (in the address slot). Therefore, the slave device responds on the MISO line with whatever content is at the address equivalent to the read command value (for example, if the read command is 0xB, the response is the data read from Slave Address 0xB).
Workaround	The following workarounds can be used. Utilize the overlap mode to align the transmit/receive SPI operations and discard the junk bytes, as follows: 1. Set SPI_RD_CTL.OVERLAP = 1 to enable overlap mode. 2. Set SPI_RD_CTL.TXBYTES = 1 to configure a single transmit byte (8-bit address register). 3. Set SPI_CNT.VALUE = 3 to configure the transfer count: one byte for the address register, one byte for the command, and one dummy byte to obtain the read value. 4. On the receive side, discard the first two junk bytes received during the transfer of the address and command bytes before processing the actual read value in the third byte. Alternatively, do not use Tx DMA operation on the SPI transmit side, by taking the following steps: 1. Enable only SPI RX DMA requests. 2. Fill the SPI Tx FIFO by using core accesses to write the SPI_TX register. 3. Perform a dummy read of the SPI_RX register to kick off the SPI transfers.
Revision	0.1

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADUCM4050BCBZ-RL	−40°C to +85°C	72-Ball Wafer Level Chip Scale Package [WLCSP], 13" Reel	CB-72-3
ADUCM4050BCBZ-R7	−40°C to +85°C	72-Ball Wafer Level Chip Scale Package [WLCSP], 7" Reel	CB-72-3
ADUCM4050BCPZ	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package [LFCSP]	CP-64-17
ADUCM4050BCPZ-RL	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package [LFCSP], 13" Reel	CP-64-17
ADUCM4050BCPZ-R7	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package [LFCSP], 7" Reel	CP-64-17
EV-COG-AD4050LZ		ADuCM4050 LFCSP Development Board	
EV-COG-AD4050WZ		ADuCM4050 WLCSP Development Board	

[1] Z = RoHS Compliant Part.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).