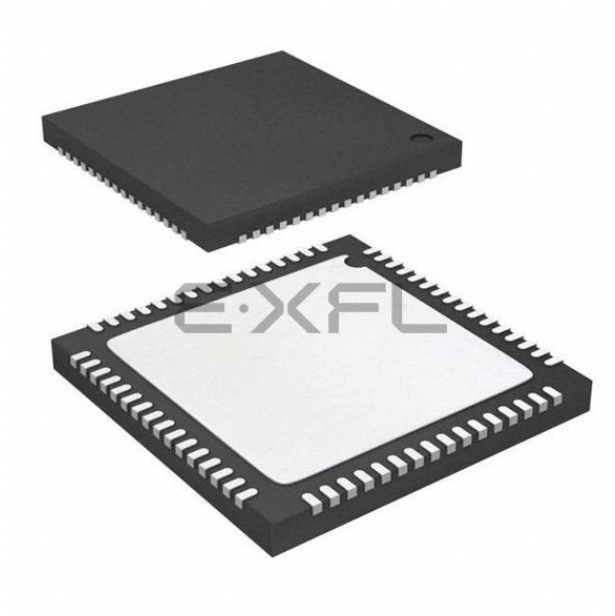

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	52MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	DMA, PWM, WDT
Number of I/O	51
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.74V ~ 3.6V
Data Converters	A/D 8x12b SAR
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-WFQFN Exposed Pad, CSP
Supplier Device Package	64-LFCSP (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aducm4050bcpz-rl

TABLE OF CONTENTS

REVISION HISTORY

6/2018—Revision 0: Initial Version

SPECIFICATIONS

OPERATING CONDITIONS AND ELECTRICAL CHARACTERISTICS

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
EXTERNAL BATTERY SUPPLY VOLTAGE[1, 2]	V_{BAT}	1.74	3.0	3.6	V	
INPUT VOLTAGE						
High Level	V_{IH}	2.5			V	V_{BAT} = 3.6 V
Low Level	V_{IL}			0.45	V	V_{BAT} = 1.74 V
ADC SUPPLY VOLTAGE	V_{BAT_ADC}	1.74	3.0	3.6	V	
OUTPUT VOLTAGE[3]						
High Level	V_{OH}	1.4			V	V_{BAT} = 1.74 V, I_{OH} = −1.0 mA
Low Level	V_{OL}			0.4	V	V_{BAT} = 1.74 V, I_{OL} = 1.0 mA
INPUT CURRENT PULL-UP[4]						
High Level	I_{IHPU}		0.01	0.2	µA	V_{BAT} = 3.6 V, V_{IN} = 3.6 V
Low Level	I_{ILPU}			100	µA	V_{BAT} = 3.6 V, V_{IN} = 0 V
THREE-STATE LEAKAGE CURRENT						
High Level[5]	I_{OZH}		0.01	0.15	µA	V_{BAT} = 3.6 V, V_{IN} = 3.6 V
Pull-Up[6]	I_{OZHPU}			0.30	µA	V_{BAT} = 3.6 V, V_{IN} = 3.6 V
Pull-Down[7]	I_{OZHPD}			100	µA	V_{BAT} = 3.6 V, V_{IN} = 3.6 V
Low Level[5]	I_{OZL}		0.01	0.15	µA	V_{BAT} = 3.6 V, V_{IN} = 0 V
Pull-Up[6]	I_{OZLPU}			100	µA	V_{BAT} = 3.6 V, V_{IN} = 0 V
Pull-Down[7]	I_{OZLPD}			0.15	µA	V_{BAT} = 3.6 V, V_{IN} = 0 V
INPUT CAPACITANCE	C_{IN}		10		pF	T_J = 25°C
V_{BAT} POWER-ON RESET	V_{VBAT_POR}	1.49	1.59	1.64	V	Power-on reset level on V_{BAT}; trip point is detected when battery is decaying[8]
Junction Temperature	T_J	−40		+85	°C	$T_{AMBIENT}$ = −40°C to +85°C

[1] Value applies to VBAT_ANA1, VBAT_ANA2, VBAT_DIG1, and VBAT_DIG2 pins.
[2] Must remain powered (even if the associated function is not used).
[3] Applies to the output and bidirectional pins: P0_00 to P0_15, P1_00 to P1_15, P2_00 to P2_15, and P3_00 to P3_03.
[4] Applies to the $\overline{\text{SYS\_HWRST}}$ input pin with pull-up.
[5] Applies to the three-state pins: P0_00 to P0_05, P0_08 to P0_15, P1_00 to P1_15, P2_00 to P2_15, P3_00 to P3_03.
[6] Applies to the three-state pins with pull-ups: P0_00 to P0_05, P0_07 to P0_15, P1_00 to P1_15, P2_00 to P2_15, and P3_00 to P3_03.
[7] Applies to the P0_06 three-state pin with pull-down.
[8] This specification is valid when the device is powered up; if the battery decays and falls below 1.71 V, power-on reset is detected. For safer operation of the device, adhere to the V_{BAT} specification.

EMBEDDED FLASH SPECIFICATIONS

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FLASH						
Endurance		10,000			Cycles	
Data Retention			10		Years	

Flexi Mode

Table 4.

Parameter	Min	Typ[1]	Max[2]	Unit	Test Conditions/Comments
FLEXI™ MODE					Current consumption when V_{BAT} = 3.0 V
Buck Enabled		0.40	1.85	mA	PCLK disabled, HCLK = 26 MHz
		0.54	1.98	mA	PCLK = 26 MHz, HCLK = 26 MHz
		0.62	2.06	mA	PCLK disabled, HCLK = 52 MHz
		0.88	2.33	mA	PCLK = 52 MHz, HCLK = 52 MHz
Buck Disabled		0.62	3.06	mA	PCLK disabled, HCLK = 26 MHz
		0.88	3.32	mA	PCLK = 26 MHz, HCLK = 26 MHz
		1.04	3.48	mA	PCLK disabled, HCLK = 52 MHz
		1.57	4.01	mA	PCLK = 52 MHz, HCLK = 52 MHz

[1] T_J = 25°C.
[2] T_J = 85°C.

Deep Sleep Modes—V_{BAT} = 1.8 V

Table 5.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
HIBERNATE MODE[1]					V_{BAT} = 1.8 V
T_J = 25°C		0.78		µA	Real-Time Clock 1 (RTC1) and Real-Time Clock 0 (RTC0) disabled, 16 kB SRAM retained, LFXTAL off
		0.89		µA	RTC1 and RTC0 disabled, 28 kB SRAM retained, LFXTAL off
		0.96		µA	RTC1 and RTC0 disabled, 48 kB SRAM retained, LFXTAL off
		1.06		µA	RTC1 and RTC0 disabled, 60 kB SRAM retained, LFXTAL off
		1.35		µA	RTC1 and RTC0 disabled, 80 kB SRAM retained, LFXTAL off
		1.44		µA	RTC1 and RTC0 disabled, 92 kB SRAM retained, LFXTAL off
		1.51		µA	RTC1 and RTC0 disabled, 112 kB SRAM retained, LFXTAL off
		1.60		µA	RTC1 and RTC0 disabled, 124 kB SRAM retained, LFXTAL off
		0.85		µA	RTC1 enabled, 16 kB SRAM retained, low frequency RC oscillator (LFOSC) as RTC1 source
		1.66		µA	RTC1 enabled, 124 kB SRAM retained, LFOSC as RTC1 source
		1.08		µA	RTC1 enabled, 16 kB SRAM retained, LFXTAL as RTC1 source
		1.11		µA	RTC0 enabled, 16 kB SRAM retained, LFXTAL as RTC0 source
		1.14		µA	RTC1 and RTC0 enabled, 16 kB SRAM retained, LFXTAL as RTC1 and RTC0 source
		1.82		µA	RTC1 enabled, 124 kB SRAM retained, LFXTAL as RTC1 source
		1.84		µA	RTC0 enabled, 124 kB SRAM retained, LFXTAL as RTC0 source
		1.87		µA	RTC1 and RTC0 enabled, 124 kB SRAM retained, LFXTAL as RTC1 and RTC0 source
T_J = 85°C		2.79	6.90	µA	RTC1 and RTC0 disabled, 16 kB SRAM retained, LFXTAL off
		3.46	9.00	µA	RTC1 and RTC0 disabled, 28 kB SRAM retained, LFXTAL off
		4.73	12.50	µA	RTC1 and RTC0 disabled, 48 kB SRAM retained, LFXTAL off
		5.38	14.80	µA	RTC1 and RTC0 disabled, 60 kB SRAM retained, LFXTAL off
		6.26	16.70	µA	RTC1 and RTC0 disabled, 80 kB SRAM retained, LFXTAL off
		6.85	18.70	µA	RTC1 and RTC0 disabled, 92 kB SRAM retained, LFXTAL off
		8.12	22.30	µA	RTC1 and RTC0 disabled, 112 kB SRAM retained, LFXTAL off
		8.74	24.50	µA	RTC1 and RTC0 disabled, 124 kB SRAM retained, LFXTAL off
		2.95	7.30	µA	RTC1 enabled, 16 kB SRAM retained, LFOSC as RTC1 source
		8.92	25.50	µA	RTC1 enabled, 124 kB SRAM retained, LFOSC as RTC1 source
		3.16	7.77	µA	RTC1 enabled, 16 kB SRAM retained, LFXTAL as RTC1 source
		3.16	7.78	µA	RTC0 enabled, 16 kB SRAM retained, LFXTAL as RTC0 source
		3.22	7.92	µA	RTC1 and RTC0 enabled, 16 kB SRAM retained, LFXTAL as RTC1 and RTC0 source
		9.07	25.70	µA	RTC1 enabled, 124 kB SRAM retained, LFXTAL as RTC1 source
		9.10	25.76	µA	RTC0 enabled, 124 kB SRAM retained, LFXTAL as RTC0 source
		9.15	25.91	µA	RTC1 and RTC0 enabled, 124 kB SRAM retained, LFXTAL as RTC1 and RTC0 source
SHUTDOWN MODE[1]					V_{BAT} = 1.8 V
T_J = 25°C		0.03		µA	RTC0 disabled
		0.37		µA	RTC0 enabled, LFXTAL as RTC0 source
T_J = 85°C		0.31	1.30	µA	RTC0 disabled
		0.78	2.93	µA	RTC0 enabled, LFXTAL as RTC0 source
FAST SHUTDOWN MODE[1]					V_{BAT} = 1.8 V
T_J = 25°C		0.17		µA	RTC0 disabled
		0.51		µA	RTC0 enabled, LFXTAL as RTC0 source
T_J = 85°C		0.47	1.50	µA	RTC0 disabled
		0.94	3.53	µA	RTC0 enabled, LFXTAL as RTC0 source

[1] Buck enable/disable does not affect power consumption.

TEMPERATURE SENSOR SPECIFICATIONS

Table 9.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
TEMPERATURE SENSOR					Internal reference = 1.25 V with C_{LOAD} = 0.1 µF and 4.7 µF on the VREFP_ADC pin
Accuracy		±2		°C	$T_{AMBIENT}$ = 25°C to +5°C
		±3		°C	$T_{AMBIENT}$ = −40°C to +85°C

SYSTEM CLOCKS

External Crystal Oscillator Specifications

Table 10.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
LOW FREQUENCY EXTERNAL CRYSTAL OSCILLATOR (LFXTAL)						
Frequency	f_{LFXTAL}		32,768		Hz	
External Capacitance from SYS_LFXTAL_IN Pin to Ground and from SYS_LFXTAL_OUT Pin to Ground	C_{LFXTAL}	6		10	pF	External capacitors on SYS_LFXTAL_IN and SYS_LFXTAL_OUT pins must be selected considering the printed circuit board (PCB) trace capacitance due to routing
Crystal Equivalent Series Resistance	ESR_{LFXTAL}	30		50	kΩ	
Crystal Drive Level[1]				50	nW	
Oscillator Transconductance[1]	gm_{LFXTAL}	8			µS	
HIGH FREQUENCY EXTERNAL CRYSTAL OSCILLATOR (HFXTAL)						
Frequency	f_{HFXTAL}		26		MHz	
External Capacitance from SYS_HFXTAL_IN Pin to Ground and from SYS_HFXTAL_OUT Pin to Ground	C_{HFXTAL}			20	pF	External capacitors on SYS_HFXTAL_IN and SYS_HFXTAL_OUT pins must be selected considering the PCB trace capacitance due to routing
Crystal Equivalent Series Resistance	ESR_{HFXTAL}			50	kΩ	

[1] Guaranteed by design.

On-Chip Resistor-Capacitor (RC) Oscillator Specifications

Table 11.

Parameter	Symbol	Min	Typ	Max	Unit
LOW FREQUENCY RC OSCILLATOR (LFOSC)					
Frequency	f_{LFOSC}	30,800	32,768	35,062	Hz
HIGH FREQUENCY RC OSCILLATOR (HFOSC)					
Frequency	f_{HFOSC}	25.03	26	27.07	MHz

System Clocks and Phase-Locked Loop (PLL) Specifications

Table 12.

Parameter	Symbol	Min	Typ	Max	Unit
PLL SPECIFICATIONS					
PLL Input Clock Frequency[1]	f_{PLLIN}	16		26	MHz
PLL Output Clock Frequency[2, 3]	f_{PLLOUT}	16		60	MHz
System Peripheral Clock (PCLK) Frequency	f_{PCLK}	0.8125		52	MHz
Advanced High Performance Bus Clock (HCLK) Frequency	f_{HCLK}	0.8125		52	MHz

[1] The input to the PLL can come from either the high frequency external crystal (HFXTAL), SYS_CLKIN pin or from the high frequency internal RC oscillator (HFOSC).
[2] For the maximum value, the recommended settings are PLL MSEL = 13, PLL NSEL = 16, PLL DIV2 = 1 for PLL input clock = 26 MHz; and PLL MSEL = 13, PLL NSEL = 26, PLL DIV2 = 1 for PLL input clock = 16 MHz; see the ADuCM4050 Ultra Low Power ARM Cortex-M4F MCU with Integrated Power Management Hardware Reference for more information on these configuration options.
[3] For the minimum value, the recommended settings are PLL MSEL = 13, PLL NSEL = 30, PLL DIV2 = 0 for PLL input clock = 26 MHz; and PLL MSEL = 8, PLL NSEL = 30, PLL DIV2 = 0 for 16 MHz.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
ENABLE AND THREE-STATE SERIAL PORTS						
Switching Characteristics						
Data Enable from Internal Transmit SPORT Clock[3]	t_{DDTIN}	5			ns	
Data Disable from Internal Transmit SPORT Clock[3]	t_{DDTTI}			160	ns	

[1] This specification is referenced to the sample edge.
[2] This specification indicates the minimum instantaneous width or period that can be tolerated due to duty cycle variation or jitter on the external SPORT Clock.
[3] These specifications are referenced to the drive edge.

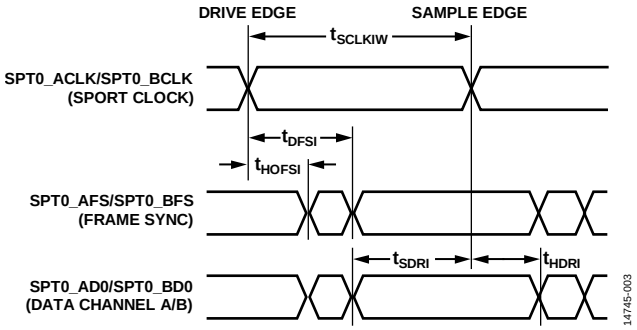

Figure 3. Serial Ports (Data Receive Mode through Internal Clock)

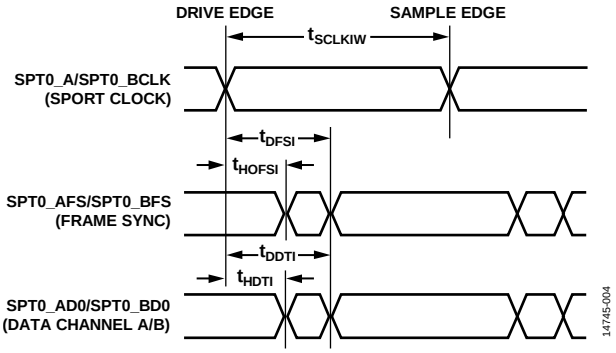

Figure 4. Serial Ports (Data Transmit Mode through Internal Clock)

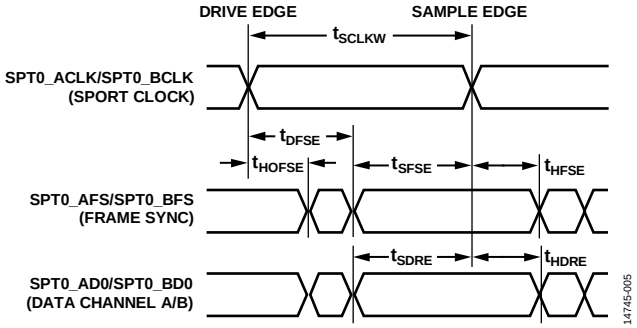

Figure 5. Serial Ports (Data Receive Mode through External Clock)

ABSOLUTE MAXIMUM RATINGS

Table 20.

Parameter	Rating
Supply	
VBAT_ANA1, VBAT_ANA2, VBAT_ADC, VBAT_DIG1, VBAT_DIG2, and VREFP_ADC	−0.3 V to +3.6 V
Analog	
VDCDC_CAP1N, VDCDC_CAP1P, VDCDC_OUT, VDCDC_CAP2N, and VDCDC_CAP2P	−0.3 V to +3.6 V
VLDO_OUT, SYS_HFXTAL_IN, SYS_HFXTAL_OUT, SYS_LFXTAL_IN, and SYS_LFXTAL_OUT	−0.3 V to +1.32 V
Digital Input/Output	
P0_xx, P1_xx, P2_xx, P3_xx, and $\overline{\text{SYS\_HWRST}}$	−0.3 V to +3.6 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required. θ_{JA} can be used for a first-order approximation of T_J by the following equation:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where:
T_A is ambient temperature (°C).
T_J is junction temperature (°C).
P_D is power dissipation (to calculate power dissipation.

Table 21. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
CP-64-17	26.3	1.0	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

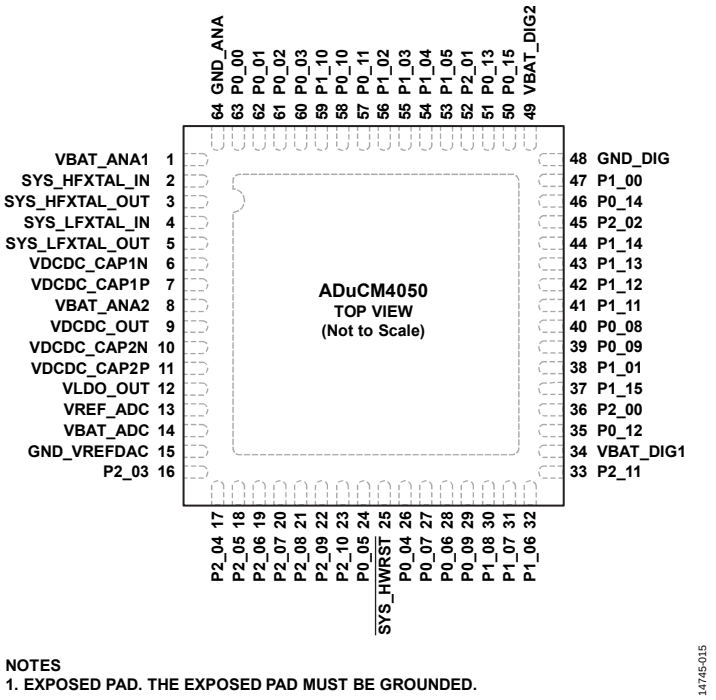

Figure 15. 64-Lead LFCSP Pin Configuration

Table 23. 64-Lead LFCSP Pin Function Descriptions

Pin No.	Mnemonic	Signal Names	Description
1	VBAT_ANA1	Not applicable	External Supply for Analog Circuits in the MCU.
2	SYS_HFXTAL_IN	Not applicable	High Frequency Crystal Input.
3	SYS_HFXTAL_OUT	Not applicable	High Frequency Crystal Output.
4	SYS_LFXTAL_IN	Not applicable	Low Frequency Crystal Input.
5	SYS_LFXTAL_OUT	Not applicable	Low Frequency Crystal Output.
6	VDCDC_CAP1N	Not applicable	Buck Converter Capacitor 1 Negative Terminal.
7	VDCDC_CAP1P	Not applicable	Buck Converter Capacitor 1 Positive Terminal.
8	VBAT_ANA2	Not applicable	External Supply for Analog Circuits in the MCU.
9	VDCDC_OUT	Not applicable	Buck Converter Output. This pin is only for connecting the decoupling capacitor. Do not connect to external load.
10	VDCDC_CAP2N	Not applicable	Buck Converter Capacitor 2 Negative Terminal.
11	VDCDC_CAP2P	Not applicable	Buck Converter Capacitor 2 Positive Terminal.
12	VLDO_OUT	Not applicable	Low Dropout Regulator Output. This pin is only for connecting the decoupling capacitor. Do not connect to external load.
13	VREF_ADC	Not applicable	External Reference Voltage for Internal ADC.
14	VBAT_ADC	Not applicable	External Supply for Internal ADC.
15	GND_VREFADC	Not applicable	Ground for Internal ADC.
16	P2_03	GPIO35, ADC0_VIN0	GPIO. See the GPIO Multiplexing section for more information.
17	P2_04	GPIO36, ADC0_VIN1	GPIO. See the GPIO Multiplexing section for more information.
18	P2_05	GPIO37, ADC0_VIN2	GPIO. See the GPIO Multiplexing section for more information.
19	P2_06	GPIO38, ADC0_VIN3	GPIO. See the GPIO Multiplexing section for more information.
20	P2_07	GPIO39, ADC0_VIN4, SPI2_CS3	GPIO. See the GPIO Multiplexing section for more information.
21	P2_08	GPIO40, ADC0_VIN5, SPI0_CS2, RTC1_SS3	GPIO. See the GPIO Multiplexing section for more information.
22	P2_09	GPIO41, ADC0_VIN6, SPI0_CS3	GPIO. See the GPIO Multiplexing section for more information.
23	P2_10	GPIO42, ADC0_VIN7, SPI2_CS2	GPIO.
24	P0_05	GPIO05, I2C0_SDA	GPIO. See the GPIO Multiplexing section for more information.
25	$\overline{\text{SYS\_HWRST}}$	Not applicable	Hardware Reset Pin.
26	P0_04	GPIO04, I2C0_SCL	GPIO. See the GPIO Multiplexing section for more information.
27	P0_07	SWD0_DATA, GPIO07	GPIO. See the GPIO Multiplexing section for more information.

THEORY OF OPERATION

ARM CORTEX-M4F PROCESSOR

The ARM Cortex-M4F core is a 32-bit reduced instruction set computer (RISC). The length of the data can be 8 bits, 16 bits, or 32 bits. The length of the instruction word is 16 bits or 32 bits. The processor has the following features:

- ARM Cortex-M4F architecture
- Thumb-2 instruction set architecture (ISA) technology
- Three-stage pipeline with branch speculation
- Low latency interrupt processing with tail chaining
- Single-cycle multiply
- Hardware divide instructions
- Nested vectored interrupt controller (NVIC) (72 interrupts and 8 priorities)
- Six hardware breakpoints and one watchpoint (unlimited software breakpoints using the Segger JLink debug probe)
- Bit banding support
- Trace support—instruction trace macrocell (ITM), trace port interface unit (TPIU), and data watchpoint and trace (DWT) triggers and counters
- Memory protection unit (MPU)
- Eight-region MPU with subregions and background region
- Programmable clock generator unit
- Configurable for ultralow power operation
- Deep sleep modes, dynamic power management
- Programmable clock generator unit
- Floating point unit (FPU)
- Supports single-precision add, subtract, multiply, divide, multiply and accumulate, and square root operations
- Provides conversions between fixed point and floating point data formats, and floating point constant instructions

ARM Cortex-M4F Subsystem

The ADuCM4050 MCU memory map (see the ADuCM4050 Ultra Low Power ARM Cortex-M4F MCU with Integrated Power Management Hardware Reference) is based on the ARM Cortex-M4F memory model. By retaining the standardized memory mapping, it is easier to port applications across ARM Cortex-M4F platforms. The ADuCM4050 application development is based on memory blocks across code and SRAM regions. Sufficient internal memory is available via internal SRAM and internal flash.

Code Region

Accesses in the code region (0x0000_0000 to 0x0007_FFFF except 0x0007_F000 to 0x0007_FFFF, which is meant for protected key storage) are performed by the core and target the memory and cache resources.

SRAM Region

Accesses in the SRAM region (see Figure 22) are performed by the ARM Cortex-M4F core. The SRAM region of the core can act as a data region for an application.

- Internal SRAM data region. This space can contain read/write data. Internal SRAM can be partitioned between code and data (the SRAM region in the ARM Cortex-M4F space) in 32 kB blocks. Access to this region occurs at core clock speed with no wait states. The SRAM data region also supports read/write access by the ARM Cortex-M4F core and read/write DMA access by system devices.
- System memory mapped registers (MMRs). Various system MMRs reside in this region.

System Region

Accesses in this region (0xE000_0000 to 0xFFFF_FFFF) are performed by the ARM Cortex-M4F core and handled within the ARM Cortex-M4F platform. This system region includes the following components:

- CoreSight™ read only memory (ROM). The ROM table entries (see the ARM Cortex-M4F Technical Reference Manual) show the debug components of the processor.
- ARM advanced peripheral bus (APB) peripheral. This space is defined by ARM and occupies the bottom 256 kB of the system region (0xE000_0000 to 0xE004_0000). The space supports read/write access by the ARM Cortex-M4F core to the internal peripherals of the ARM core (NVIC, system control space (SCS), and wake-up interrupt controller (WIC)) and CoreSight ROM. It is not accessible by system DMA.
- Platform control register. This space has registers within the ARM Cortex-M4F platform component that control the ARM core, its memory, and the code cache. It is accessible by the ARM Cortex-M4F core (but not accessible by system DMA).

MEMORY ARCHITECTURE

The internal memory of the ADuCM4050 MCU is shown in Figure 22. It incorporates 512 kB of embedded flash memory for program code and nonvolatile data storage, 96 kB of data SRAM, and 32 kB of SRAM (configured as instruction space or data space).

SRAM Region

This memory space contains the application instructions and variables data, which must be accessed in real time. It supports read/write access by the ARM Cortex-M4F core and read/write DMA access by system peripherals. Byte, half-word and word accesses are supported.

SRAM is divided into 96 kB data SRAM and 32 kB instruction SRAM. If instruction SRAM is not enabled, then the associated 32 kB can be mapped as data SRAM, resulting in 128 kB of data SRAM.

When the cache controller is enabled, 4 kB of the instruction SRAM is reserved as cache memory. Optional parity bit error detection is available on all SRAM memories. Multiple parity bits are associated with each 32-bit word.

In hibernate mode, up to 124 kB of SRAM can be retained in the following ways:

- 124 kB of data SRAM
- 96 kB of data SRAM and 28 kB of instruction SRAM

MMRs (Peripheral Control and Status)

For the address space containing MMRs, refer to Figure 22. These registers provide control and status for on-chip peripherals of the ADuCM4050 MCU.

For more information about the MMRs, refer to the ADuCM4050 Ultra Low Power ARM Cortex-M4F MCU with Integrated Power Management Hardware Reference.

Flash Memory

The ADuCM4050 MCU includes 512 kB of embedded flash memory, which is accessed using a flash controller. The flash controller is coupled with a cache controller. A prefetch mechanism is implemented in the flash controller to optimize code performance.

Flash writes are supported by a keyhole mechanism via APB writes to MMRs. The flash controller provides support for DMA-based keyhole writes.

The device supports the following with consideration to flash integrity:

- A fixed user key required for running protected commands, including mass erase and page erase.
- An optional and user definable user failure analysis key (FAA key).
- An optional and user definable write protection for user-accessible memory.
- 8-bit ECC.

Cache Controller

The ADuCM4050 MCU has an optional 4 kB instruction cache. In certain applications, enabling the cache and executing the code can result in lower power consumption rather than operating directly from flash. When enabling the cache controller, 4 kB of instruction SRAM is reserved as cache memory. In hibernate mode, the cache memory is not retained.

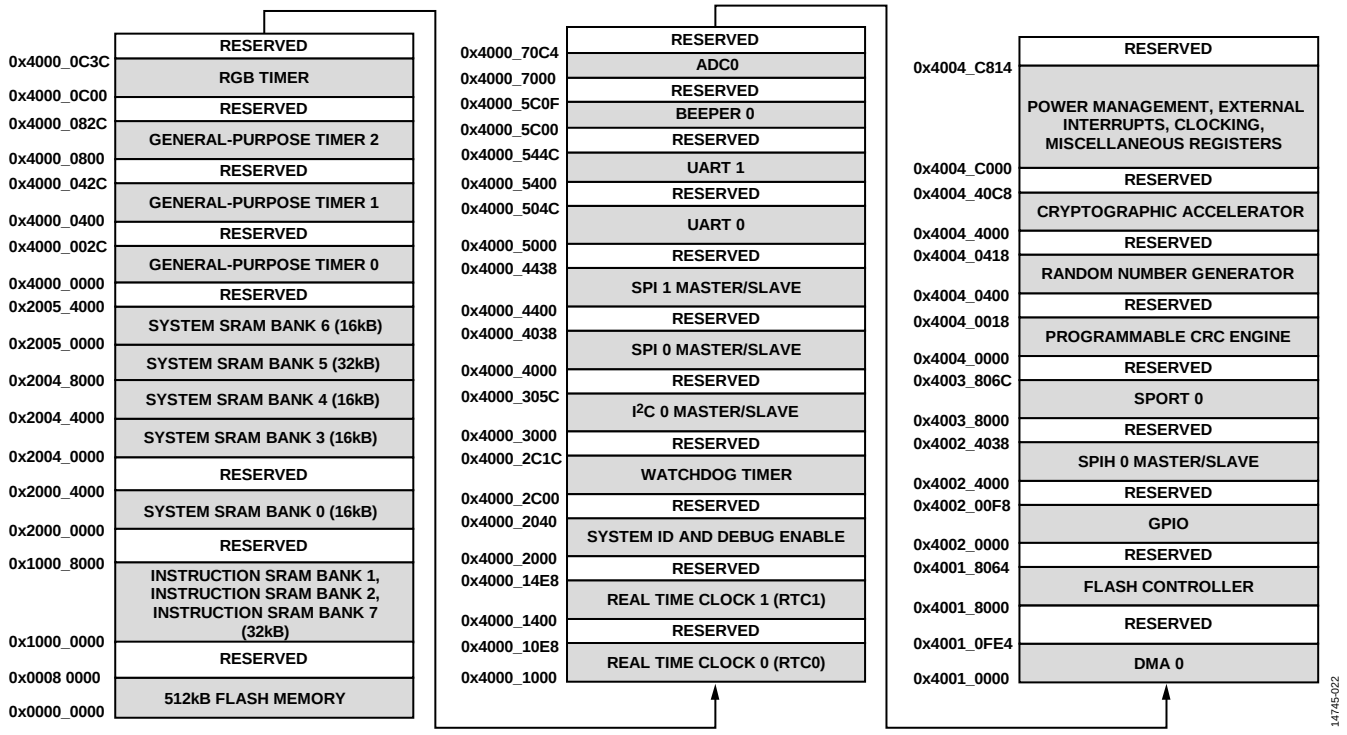

Figure 22. ADuCM4050 Memory Map—SRAM Mode 0

SYSTEM INTEGRATION FEATURES

The ADuCM4050 MCU provides several features for development of ultra low power, secure, and robust systems.

Reset

There are four kinds of resets: external, power-on, watchdog timeout, and software system reset. The software system reset is provided as part of the ARM Cortex-M4F core. The SYS_HWRST pin is toggled to perform a hardware reset.

Booting

The ADuCM4050 MCU supports two boot modes: booting from internal flash and upgrading software through UART download (see Table 24). If SYS_BMODE0 (Pin P1_01) is pulled low during power-up or a hard reset, the MCU enters into serial download mode. In this mode, an on-chip loader routine initiates in the kernel, which configures the UART port and communicates with the host to manage the firmware upgrade via a specific serial download protocol.

Table 24. Boot Modes

Boot Mode	Description
0	UART download mode.
1	Flash boot. Boot from integrated flash memory.

Power Management and Modes

The ADuCM4050 MCU has an integrated power management system that optimizes performance and extends the battery life of the device. The power management system consists of the following:

- Integrated 1.2 V low dropout regulator (LDO) and optional capacitive buck regulator
- Integrated power switches for low standby current in hibernate and shutdown modes

Additional power management features include the following:

- Customized clock gating for active modes
- Power gating to reduce leakage in hibernate and shutdown modes
- Flexible sleep modes
- Shutdown mode with no retention
- Optional high efficiency buck converter to reduce power
- Integrated low power oscillators

The PMU provides control of the ADuCM4050 MCU power modes and allows the ARM Cortex-M4F to control the clocks and power gating to reduce the power consumption. Several power modes are available, offering options to balance power consumption and functionality. The power modes available in the ADuCM4050 are described in the following sections.

Active Mode

In active mode, all peripherals can be enabled. Active power is managed by optimized clock management. See Table 3 for details on active mode current consumption.

Flexi Mode

In flexi mode, the ARM Cortex-M4F core is clock gated, but the remainder of the system is active. No instructions can be executed in this mode, but DMA transfers can continue between peripherals as well as memory to memory. See Table 4 for details on flexi mode current consumption.

Hibernate Mode

Hibernate mode provides state retention, configurable SRAM and port pin retention, a limited number of wake-up interrupts (SYS_WAKEx, UART0_RX, and optionally, RTC0 and RTC1 (FLEX_RTC™)).

Shutdown Mode

Shutdown mode is the deepest sleep mode, in which all the digital and analog circuits are powered down with an option to wake from four possible wake-up sources. The RTC0 can be (optionally) enabled in this mode, and the device can be periodically woken up by the RTC0 interrupt.

Shutdown Mode—Fast Wake-Up

This mode has a faster wake-up time than shutdown mode at the expense of higher power consumption. See Table 25 for wake-up time specifications.

Power Management and Control

The following features are available for power management and control:

- Voltage range of 1.74 V to 3.6 V using a single supply (such as the CR2032 coin cell battery).
- GPIOs are driven directly from the battery. The pin state is retained in hibernate and shutdown modes. The GPIO configuration is only retained in hibernate mode.
- Wake-up from external interrupts (via GPIOs), UART0_RX interrupt, and RTCs for hibernate mode.
- Wake-up from external interrupts (via GPIOs) and RTC0 for shutdown mode.
- Optional high power buck converter for 1.2 V full on support (MCU use only). See Figure 23 for suggested external circuitry.

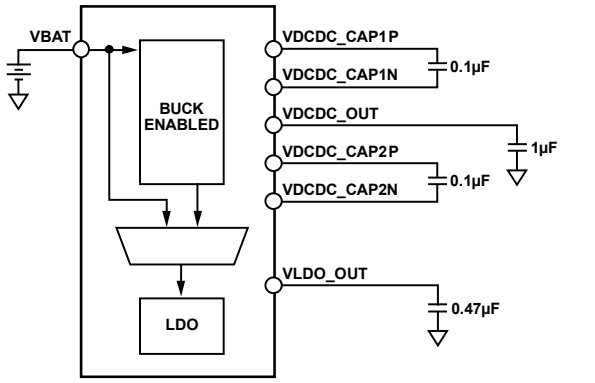

Figure 23. Buck Enable Design

Table 25. Power Modes Wake-Up Times

Mode	VTOR[1]	Root Clock	HCLK/PCLK	Wake-Up Time
Flexi	Flash	HFOSC	26 MHz	1.605 µs
Hibernate	Flash	HFOSC	26 MHz	10.356 µs
	SRAM	HFOSC	26 MHz	4.984 µs
	Flash	HFXTAL	26 MHz	686.452 µs
	Flash	PLL_HFOSC	26 MHz	14.487 µs
	Flash	PLL_HFXTAL	26 MHz	742.668 µs
	Flash	PLL_HFOSC	52 MHz	15.730 µs
	Flash	PLL_HFXTAL	52 MHz	726.101 µs
Shutdown	Flash	HFOSC	26 MHz	68.144 ms
Shutdown (Fast Wake-Up)	Flash	HFOSC	26 MHz	1.220 ms

[1] VTOR means vector table offset register.

Security Features

The ADuCM4050 MCU provides a combination of hardware and software protection mechanisms that lock out access to the device in secure mode, but grant access in open mode. These mechanisms include the password protected slave boot mode (UART), as well as password protected serial wire debug (SWD) interfaces. Mechanisms are provided to protect the device contents (flash, SRAM, CPU registers, and peripheral registers) from being read through an external interface by an unauthorized user. This is referred to as read protection.

It is possible to protect the device from being reprogrammed in circuit with unauthorized code. This is referred to as in circuit write protection.

The device can be configured with no protection, read protection, or read and in circuit write protection. It is not necessary to provide in circuit write protection without read protection.

This product includes security features that can be used to protect embedded nonvolatile memory contents and prevent execution of unauthorized code. When security is enabled on this device (either by the ordering party or the subsequent receiving parties), the ability of Analog Devices to conduct failure analysis on returned devices is limited. Contact Analog Devices for details on the failure analysis limitations for this device.

Cryptographic Accelerator

The cryptographic accelerator is a 32-bit APB DMA capable peripheral. There are two 128-bit buffers provided for data input/output operations. These buffers read in or read out 128 bits in four data accesses. Big endian and little endian data formats are supported, as are the following modes:

- ECB mode—AES mode
- CTR mode
- CBC mode
- Message authentication code (MAC) mode
- CCM/CCM* mode
- SHA-256 modes
- Protected key storage with key wrap and unwrap—HMAC signature generation

True Random Number Generator (TRNG)

The TRNG is used during operations where nondeterministic values are required. This can include generating challenges for secure communication or keys used for an encrypted communication channel. The generator can run multiple times to generate a sufficient number of bits for the strength of the intended operation. The true random number generator can seed a deterministic random bit generator.

Reliability and Robustness Features

The ADuCM4050 MCU provides several features that can enhance or help achieve certain levels of system safety and reliability. Whereas the level of safety is mainly dominated by system considerations, the following features are provided to enhance robustness.

ECC Enabled Flash Memory

The entire flash array is protected to either correct single-bit errors or detect two bit errors per 64-bit flash data.

Multiparity Bit Protected SRAM

Each word of the SRAM and cache memory is protected by multiple parity bits to allow detection of random soft errors.

Software Watchdog

The on-chip watchdog timer can provide software-based supervision of the ADuCM4050 core.

Table 26. RTC Features

Features	RTC0	RTC1 (FLEX_RTC)
Resolution of Time Base (Prescaling)	Counts time at 1 Hz in units of seconds. Operationally, RTC0 always prescales to 1 Hz (for example, divide by 32,768) and always counts real time in units of seconds.	Can prescale the clock by any power of two from 0 to 15. It can count time in units of any of these 16 possible prescale settings. For example, the clock can be prescaled by 1, 2, 4, 8, …, 16,384, or 32,768.
Source Clock	LFXTAL.	Depending on the low frequency multiplexer configuration, the RTC is clocked by the LFXTAL or the LFOSC.
Wake-Up Timer	Wake-up time is specified in units of seconds.	Supports alarm times down to a resolution of 30.52 µs, that is, where the time is specified down to a specific 32 kHz clock cycle.
Number of Alarms	One alarm only. Uses an absolute, nonrepeating alarm time, specified in units of 1 sec.	Two alarms. One absolute alarm time and one periodic alarm, repeating every 60 prescaled time units.
SensorStrobe Mechanism	Not available.	Four independent channels with fine control on duty cycle and frequency (0.5 Hz to 16.384 kHz). SensorStrobe is an alarm function in the RTC that can send an output pulse via GPIOs to an external device to instruct that device to take a measurement or perform some action at a specific time. SensorStrobe events are scheduled at a specific target time relative to the real-time count of the RTC. SensorStrobe can be enabled in active, flexi, and hibernate modes.
Input Capture	Not available.	Input capture takes a snapshot of the RTC real-time count when an external device signals an event via a transition on one of the GPIO inputs to the ADuCM4050 MCU. Typically, an input capture event is triggered by an autonomous measurement or action on such a device, which then signals to the ADuCM4050 MCU that the RTC must take a snapshot of time corresponding to the event. Taking this snapshot can wake up the ADuCM4050 MCU and cause an interrupt to the CPU. The CPU can subsequently obtain information from the RTC on the exact 32 kHz cycle on which the input capture event occurred.
Input Sampling	Not available.	Each SensorStrobe channel has up to three separate GPIO inputs from an external device, which can be sampled based on the output pulse sent to the external device. Each channel can be configured to interrupt the ADuCM4050 MCU when any activity happens on these GPIO inputs from the external device. These inputs can broadcast sensor states such as first in, first out (FIFO) buffer full, switch open, and threshold crossed. This feature allows the ADuCM4050 MCU to remain in a low power state and wake up to process the data only when a specific programmed sequence from an external device is detected.

Table 31. Signal Multiplexing for Port 2

Pin	Availability		Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3
	WLCSP	LFCSP				
P2_00	Yes	Yes	GPIO32	SPT0_AFS	UART1_RX	Not applicable
P2_01	Yes	Yes	GPIO33/SYS_WAKE3	Not applicable	TMR2_OUT	Not applicable
P2_02	Yes	Yes	GPIO34	SPT0_ACNV	SPI1_CS2	Not applicable
P2_03	Yes	Yes	GPIO35	ADC0_VIN0	Not applicable	Not applicable
P2_04	Yes	Yes	GPIO36	ADC0_VIN1	Not applicable	Not applicable
P2_05	Yes	Yes	GPIO37	ADC0_VIN2	Not applicable	Not applicable
P2_06	Yes	Yes	GPIO38	ADC0_VIN3	Not applicable	Not applicable
P2_07	Yes	Yes	GPIO39	ADC0_VIN4	SPI2_CS3	Not applicable
P2_08	Yes	Yes	GPIO40	ADC0_VIN5	SPI0_CS2	RTC1_SS3
P2_09	Yes	Yes	GPIO41	ADC0_VIN6	SPI0_CS3	Not applicable
P2_10	No	Yes	GPIO42	ADC0_VIN7	SPI2_CS2	Not applicable
P2_11	Yes	Yes	GPIO43	SPI1_CS1	SYS_CLKOUT	RTC1_SS1
P2_12	Yes	No	GPIO44	UART1_TX	SPI2_CS3	Not applicable
P2_13	Yes	No	GPIO45	UART1_RX	SPI0_CS2	Not applicable
P2_14	Yes	No	GPIO46	SPI0_CS3	Not applicable	Not applicable
P2_15	Yes	No	GPIO47	SPI2_CS2	SPI1_CS3	SPI0_CS1

Table 32. Signal Multiplexing for Port 3[1]

Pin	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3
P3_00	GPIO48	RGB_TMR0_1	SPT0_ACLK	Not applicable
P3_01	GPIO49	RGB_TMR0_2	SPT0_AFS	Not applicable
P3_02	GPIO50	RGB_TMR0_3	SPT0_AD0	Not applicable
P3_03	GPIO51	Not applicable	SPT0_ACNV	Not applicable

[1] Only available in WLCSP.

APPLICATIONS INFORMATION

This section contains circuit diagrams that show the recommended external components for proper operation of the ADuCM4050 in example application scenarios.

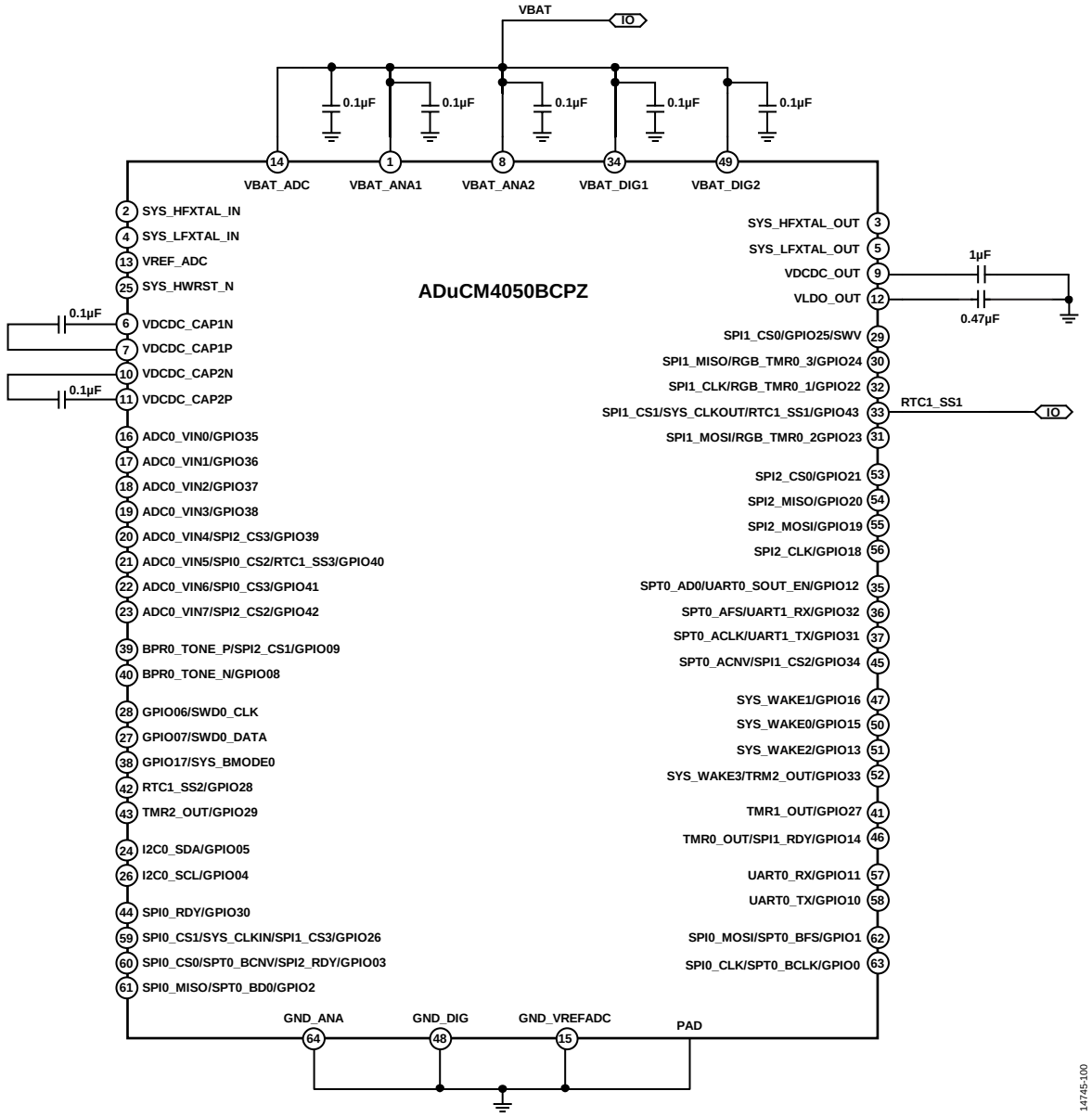

Figure 26. Recommended External Components when Using the Internal Buck Converter

Figure 27. Recommended External Components when Using LFXTAL and HFXTAL

SILICON ANOMALY

This anomaly list describes the known bugs, anomalies, and workarounds for the ADuCM4050. These anomalies represent the currently known differences between revisions of the ADuCM4050 product and the functionality specified in the ADuCM4050 data sheet and the hardware reference manual.

Analog Devices, Inc., is committed, through future silicon revisions, to continuously improve silicon functionality. Analog Devices tries to ensure that these future silicon revisions remain compatible with your present software/systems by implementing the recommended workarounds outlined here.

ADuCM4050 FUNCTIONALITY ISSUES

Silicon Revision Identifier	Silicon Status	No. of Reported Anomalies
0.1	Released	3 (21000011, 21000016, 21000017)

A silicon revision number with the form x.y is branded on all devices. The silicon revision can be electronically determined by reading Bits[3:0] of the SYS_CHIPID register. SYS_CHIPID = 0x1 indicates Silicon Revision 0.1, and SYS_CHIPID = 0x0 indicates Silicon Revision 0.0.

FUNCTIONALITY ISSUES

Table 33. 21000011—I²C Master Mode Fails to Generate Clock when Clock Dividers are Too Small

Issue	When the I²C clock dividers are configured in master mode such that the sum of the low and high bit fields in the I2C_DIV register is less than 16, the I²C fails to generate a clock.
Workaround	Program the I²C clock dividers such that I2C_DIV.LOW + I2C_DIV.HIGH ≥ 16.
Revision	0.1

Table 34. 21000016—Possible Receive Data Loss with I²C Automatic Clock Stretching

Issue	When the I²C Rx FIFO is full and new I²C data is received, a data overflow occurs. When automatic clock stretching is enabled, the transaction is paused by holding the SCL (Pin P0_04) line low. This function works as expected when the next read happens after the clock is stretched (that is, after the overflow is detected). However, if the read occurs after the last bit of the I²C data is received but before the clock is stretched, the received data is not written to the Rx FIFO and is lost.
Workaround	When I²C automatic clock stretching is enabled, read the FIFO should only after the overflow flag is set in the status register to ensure that that Rx FIFO is never read at the same time that the overflow is asserted.
Revision	0.1

Table 35. 21000017—SPI Read Command Mode Does Not Work Properly when SPI_CNT is 1 and DMA is Enabled

Issue	When SPI master is enabled and uses the DMA mode with SPI_CNT = 1, the read command mode may not function properly. Consider the following configurations: SPI_RD_CTL = 0x07; SPI_CNT = 1; the transmit and receive DMA channels are configured for 1 half-word. In this configuration, the read command sent in the first byte on the MOSI output is repeated in the second byte (in the address slot). Therefore, the slave device responds on the MISO line with whatever content is at the address equivalent to the read command value (for example, if the read command is 0xB, the response is the data read from Slave Address 0xB).
Workaround	The following workarounds can be used. Utilize the overlap mode to align the transmit/receive SPI operations and discard the junk bytes, as follows: 1. Set SPI_RD_CTL.OVERLAP = 1 to enable overlap mode. 2. Set SPI_RD_CTL.TXBYTES = 1 to configure a single transmit byte (8-bit address register). 3. Set SPI_CNT.VALUE = 3 to configure the transfer count: one byte for the address register, one byte for the command, and one dummy byte to obtain the read value. 4. On the receive side, discard the first two junk bytes received during the transfer of the address and command bytes before processing the actual read value in the third byte. Alternatively, do not use Tx DMA operation on the SPI transmit side, by taking the following steps: 1. Enable only SPI RX DMA requests. 2. Fill the SPI Tx FIFO by using core accesses to write the SPI_TX register. 3. Perform a dummy read of the SPI_RX register to kick off the SPI transfers.
Revision	0.1

SECTION 1. ADuCM4050 FUNCTIONALITY ISSUES

Reference No.	Description	Status
21000011	I^2C master mode fails to generate clock when clock dividers are too small	Identified
21000016	Possible receive data loss with I^2C automatic clock stretching	Identified
21000017	SPI read command mode does not work properly when SPI_CNT is 1 and DMA is enabled	Identified

This completes the Silicon Anomaly section.

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADUCM4050BCBZ-RL	−40°C to +85°C	72-Ball Wafer Level Chip Scale Package [WLCSP], 13" Reel	CB-72-3
ADUCM4050BCBZ-R7	−40°C to +85°C	72-Ball Wafer Level Chip Scale Package [WLCSP], 7" Reel	CB-72-3
ADUCM4050BCPZ	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package [LFCSP]	CP-64-17
ADUCM4050BCPZ-RL	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package [LFCSP], 13" Reel	CP-64-17
ADUCM4050BCPZ-R7	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package [LFCSP], 7" Reel	CP-64-17
EV-COG-AD4050LZ		ADuCM4050 LFCSP Development Board	
EV-COG-AD4050WZ		ADuCM4050 WLCSP Development Board	

[1] Z = RoHS Compliant Part.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).