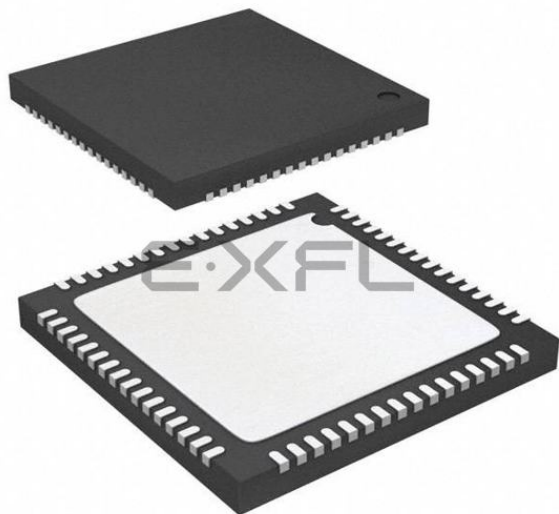




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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	52MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	DMA, PWM, WDT
Number of I/O	51
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.74V ~ 3.6V
Data Converters	A/D 8x12b SAR
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-WFQFN Exposed Pad, CSP
Supplier Device Package	64-LFCSP (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aducm4050bcpz

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REVISION HISTORY

6/2018—Revision 0: Initial Version

GENERAL DESCRIPTION

The ADuCM4050 microcontroller unit (MCU) is an ultra low power integrated microcontroller system with integrated power management for processing, control, and connectivity. The MCU system is based on the ARM® Cortex®-M4F processor. The MCU also has a collection of digital peripherals, embedded static random access memory (SRAM) and embedded flash memory, and an analog subsystem that provides clocking, reset, and power management capabilities in addition to an analog-to-digital converter (ADC) subsystem.

This data sheet describes the ARM Cortex-M4F core and memory architecture used on the ADuCM4050 MCU. It does not provide detailed programming information about the ARM processor.

The system features include an up to 52 MHz ARM Cortex-M4F processor, 512 kB of embedded flash memory with error correction code (ECC), an optional 4 kB cache for lower active power, and 128 kB system SRAM with parity. The ADuCM4050 features a power management unit (PMU), multilayer advanced microcontroller bus architecture (AMBA) bus matrix, central direct memory access (DMA) controller, and beeper interface.

The ADuCM4050 features cryptographic hardware supporting advanced encryption standard (AES)-128 and AES-256 with secure hash algorithm (SHA)-256 and the following modes: electronic code book (ECB), cipher block chaining (CBC), counter (CTR), and cipher block chaining-message authentication code (CCM/CCM*) modes.

The ADuCM4050 has protected key storage with key wrap/unwrap, and keyed hashed message authentication code (HMAC) with key unwrap.

The ADuCM4050 supports serial port (SPORT), serial peripheral interface (SPI), I²C, and universal asynchronous receiver/transmitter (UART) peripheral interfaces.

The ADuCM4050 features a real-time clock (RTC), general-purpose and watchdog timers, and programmable general-purpose input/output (GPIO) pins. There is a hardware cyclic redundancy check (CRC) calculator with programmable generator polynomial. The device also features a power on reset (POR) and power supply monitor (PSM), a 12-bit successive approximation register (SAR) ADC, a red/green/blue (RGB) timer for driving RGB LED, and a true random number generator (TRNG).

To support low dynamic and hibernate power management, the ADuCM4050 MCU provides a collection of power modes and features such as dynamic- and software-controlled clock gating and power gating.

For full details on the ADuCM4050 MCU, refer to the [ADuCM4050 Ultra Low Power ARM Cortex-M4F MCU with Integrated Power Management Hardware Reference](#).

PRODUCT HIGHLIGHTS

1. Ultra low power consumption.
2. Robust operation.
3. Full voltage monitoring in deep sleep modes.
4. ECC support on flash.
5. Parity error detection on SRAM memory.
6. Leading edge security.
7. Fast encryption provides read protection to user algorithms.
8. Write protection prevents device reprogramming by unauthorized code.
9. Failure detection of 32 kHz low frequency external crystal oscillator (LFX TAL) via interrupt.
10. SensorStrobe™ for precise time synchronized sampling of external sensors. Works in hibernate mode, resulting in drastic current reduction in system solutions. Current consumption reduces by 10 times when using, for example, the [ADXL363](#) accelerometer. Software intervention is not required after setup. No pulse drift due to software execution.

POWER SUPPLY CURRENT SPECIFICATIONS

Active Mode

Table 3.

Parameter	Min	Typ ¹	Max ²	Unit	Test Conditions/Comments
ACTIVE MODE ³					Current consumption when $V_{BAT} = 3.0\text{ V}$
Buck Enabled		1.27	2.71	mA	Code executing from flash, cache enabled, system peripheral clock (PCLK) disabled, advanced high performance clock (HCLK) = 26 MHz ⁴
		1.83	3.28	mA	Code executing from flash, cache disabled, PCLK disabled, HCLK = 26 MHz ⁴
		1.40	2.84	mA	Code executing from flash, cache enabled, PCLK = 26 MHz, HCLK = 26 MHz ⁴
		1.97	3.41	mA	Code executing from flash, cache disabled, PCLK = 26 MHz, HCLK = 26 MHz ⁴
		2.33	3.78	mA	Code executing from flash, cache enabled, PCLK disabled, HCLK = 52 MHz ⁵
		2.94	4.39	mA	Code executing from flash, cache disabled, PCLK disabled, HCLK = 52 MHz ⁵
		2.59	4.04	mA	Code executing from flash, cache enabled, PCLK = 52 MHz, HCLK = 52 MHz ⁵
		3.21	4.65	mA	Code executing from flash, cache disabled, PCLK = 52 MHz, HCLK = 52 MHz ⁵
		1.43	2.87	mA	Code executing from SRAM, PCLK disabled, HCLK = 26 MHz ⁴
		1.56	3.00	mA	Code executing from SRAM, PCLK = 26 MHz, HCLK = 26 MHz ⁴
		2.64	4.09	mA	Code executing from SRAM, PCLK disabled, HCLK = 52 MHz ⁵
		2.90	4.35	mA	Code executing from SRAM, PCLK = 52 MHz, HCLK = 52 MHz ⁵
Dynamic Current		41		μA/MHz	Code executing from flash, cache enabled
Buck Disabled		2.34	4.78	mA	Code executing from flash, cache enabled, PCLK disabled, HCLK = 26 MHz ⁴
		3.38	5.82	mA	Code executing from flash, cache disabled, PCLK disabled, HCLK = 26 MHz ⁴
		2.60	5.04	mA	Code executing from flash, cache enabled, PCLK = 26 MHz, HCLK = 26 MHz ⁴
		3.65	6.09	mA	Code executing from flash, cache disabled, PCLK = 26 MHz, HCLK = 26 MHz ⁴
		4.46	6.90	mA	Code executing from flash, cache enabled, PCLK disabled, HCLK = 52 MHz ⁵
		5.61	8.05	mA	Code executing from flash, cache disabled, PCLK disabled, HCLK = 52 MHz ⁵
		4.98	7.42	mA	Code executing from flash, cache enabled, PCLK = 52 MHz, HCLK = 52 MHz ⁵
		6.14	8.58	mA	Code executing from flash, cache disabled, PCLK = 52 MHz, HCLK = 52 MHz ⁵
		2.66	5.10	mA	Code executing from SRAM, PCLK disabled, HCLK = 26 MHz ⁴
		2.92	5.36	mA	Code executing from SRAM, PCLK = 26 MHz, HCLK = 26 MHz ⁴
		5.08	7.52	mA	Code executing from SRAM, PCLK disabled, HCLK = 52 MHz ⁵
		5.60	8.04	mA	Code executing from SRAM, PCLK = 52 MHz, HCLK = 52 MHz ⁵
Dynamic Current		82		μA/MHz	Code executing from flash, cache enabled

¹ $T_J = 25^\circ\text{C}$ ² $T_J = 85^\circ\text{C}$ ³ The code being executed is a prime number generation in a continuous loop, with high frequency RC oscillator (HFOSC) as the system clock source.⁴ Zero wait states and low buck load.⁵ One wait state and high buck load.

Flexi Mode

Table 4.

Parameter	Min	Typ ¹	Max ²	Unit	Test Conditions/Comments
FLEXI™ MODE					Current consumption when $V_{BAT} = 3.0\text{ V}$
Buck Enabled		0.40	1.85	mA	PCLK disabled, HCLK = 26 MHz
		0.54	1.98	mA	PCLK = 26 MHz, HCLK = 26 MHz
		0.62	2.06	mA	PCLK disabled, HCLK = 52 MHz
		0.88	2.33	mA	PCLK = 52 MHz, HCLK = 52 MHz
Buck Disabled		0.62	3.06	mA	PCLK disabled, HCLK = 26 MHz
		0.88	3.32	mA	PCLK = 26 MHz, HCLK = 26 MHz
		1.04	3.48	mA	PCLK disabled, HCLK = 52 MHz
		1.57	4.01	mA	PCLK = 52 MHz, HCLK = 52 MHz

¹ $T_J = 25^\circ\text{C}$.² $T_J = 85^\circ\text{C}$.

ADC SPECIFICATIONS

Table 8.

Parameter ^{1, 2}	Min	Typ ³	Max	Unit	Test Conditions/Comments
INTEGRAL NONLINEARITY ERROR					
64-Lead LFCSP		±1.6		LSB	1.8 V (V _{BAT})/1.25 V (internal/external V _{REF}) ⁴
64-Lead LFCSP		−1.7 to +1.3		LSB	3.0 V (V _{BAT})/2.5 V (internal/external V _{REF}) ⁴
72-Ball WLCSP		±1.4		LSB	1.8 V (V _{BAT})/1.25 V (internal/external V _{REF}) ⁴
DIFFERENTIAL NONLINEARITY ERROR					
64-Lead LFCSP		−0.7 to +1.15		LSB	1.8 V (V _{BAT})/1.25 V (internal/external V _{REF}) ⁴
64-Lead LFCSP		−0.7 to +1.1		LSB	3.0 V (V _{BAT})/2.5 V (internal/external V _{REF}) ⁴
72-Ball WLCSP		−0.75 to +1.0		LSB	1.8 V (V _{BAT})/1.25 V (internal/external V _{REF}) ⁴
OFFSET ERROR					
64-Lead LFCSP		±0.5		LSB	1.8 V (V _{BAT})/1.25 V (external V _{REF}) ⁴
64-Lead LFCSP		±0.5		LSB	3.0 V (V _{BAT})/2.5 V (external V _{REF}) ⁴
72-Ball WLCSP		±0.5		LSB	1.8 V (V _{BAT})/1.25 V (external V _{REF}) ⁴
GAIN ERROR					
64-Lead LFCSP		±2.5		LSB	1.8 V (V _{BAT})/1.25 V (external V _{REF}) ⁴
64-Lead LFCSP		±0.5		LSB	3.0 V (V _{BAT})/2.5 V (external V _{REF}) ⁴
72-Ball WLCSP		±3.0		LSB	1.8 V (V _{BAT})/1.25 V (external V _{REF}) ⁴
I _{V_{BAT}_ADC} ⁵					
64-Lead LFCSP		129		μA	1.8 V (V _{BAT})/1.25 V (internal V _{REF}) ⁶
64-Lead LFCSP		157		μA	3.0 V (V _{BAT})/2.5 V (internal V _{REF}) ⁶
72-Ball WLCSP		124		μA	1.8 V (V _{BAT})/1.25 V (internal V _{REF}) ⁶
64-Lead LFCSP		47		μA	1.8 V (V _{BAT})/1.25 V (external V _{REF}) ⁷
64-Lead LFCSP		51		μA	3.0 V (V _{BAT})/2.5 V (external V _{REF}) ⁷
72-Ball WLCSP		46		μA	1.8 V (V _{BAT})/1.25 V (external V _{REF}) ⁷
INTERNAL REFERENCE VOLTAGE		1.25 2.50		V V	Internal reference, 1.25 V selected Internal reference, 2.5 V selected
ADC SAMPLING FREQUENCY (f _s) ⁸	0.01		1.8	MSPS	

¹ The ADC is characterized in standalone mode without core activity and minimal or no switching on the adjacent ADC channels and digital inputs/outputs.² The specifications are characterized after performing internal ADC offset calibration.³ T_J = 25°C.⁴ f_{IN} = 1068 Hz, f_s = 100 kSPS, internal reference in low power mode, 400,000 samples end point method used.⁵ Current consumption from V_{BAT}_ADC supply when ADC is performing the conversion.⁶ f_{IN} = 1068 Hz, f_s = 100 kSPS, internal reference in low power mode.⁷ f_{IN} = 1068 Hz, f_s = 100 kSPS, sine wave with 1.25 V p-p applied at ADC0_VIN1 channel input.⁸ Effects of analog source impedance must be considered when selecting ADC sampling frequency.

SYSTEM CLOCKS

External Crystal Oscillator Specifications

Table 10.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
LOW FREQUENCY EXTERNAL CRYSTAL OSCILLATOR (LFXTAL)						
Frequency	f_{LFXTAL}		32,768		Hz	External capacitors on SYS_LFXTAL_IN and SYS_LFXTAL_OUT pins must be selected considering the printed circuit board (PCB) trace capacitance due to routing
External Capacitance from SYS_LFXTAL_IN Pin to Ground and from SYS_LFXTAL_OUT Pin to Ground	C_{LFXTAL}	6		10	pF	
Crystal Equivalent Series Resistance	ESR_{LFXTAL}	30		50	k Ω	
Crystal Drive Level ¹				50	nW	
Oscillator Transconductance ¹	gm_{LFXTAL}	8			μS	
HIGH FREQUENCY EXTERNAL CRYSTAL OSCILLATOR (HFXTAL)						
Frequency	f_{HFXTAL}		26		MHz	External capacitors on SYS_HFXTAL_IN and SYS_HFXTAL_OUT pins must be selected considering the PCB trace capacitance due to routing
External Capacitance from SYS_HFXTAL_IN Pin to Ground and from SYS_HFXTAL_OUT Pin to Ground	C_{HFXTAL}			20	pF	
Crystal Equivalent Series Resistance	ESR_{HFXTAL}			50	k Ω	

¹ Guaranteed by design.

On-Chip Resistor-Capacitor (RC) Oscillator Specifications

Table 11.

Parameter	Symbol	Min	Typ	Max	Unit
LOW FREQUENCY RC OSCILLATOR (LFOSC)					
Frequency	f_{LFOSC}	30,800	32,768	35,062	Hz
HIGH FREQUENCY RC OSCILLATOR (HFOSC)					
Frequency	f_{HFOSC}	25.03	26	27.07	MHz

System Clocks and Phase-Locked Loop (PLL) Specifications

Table 12.

Parameter	Symbol	Min	Typ	Max	Unit
PLL SPECIFICATIONS					
PLL Input Clock Frequency ¹	f_{PLLIN}	16		26	MHz
PLL Output Clock Frequency ^{2, 3}	f_{PLLOUT}	16		60	MHz
System Peripheral Clock (PCLK) Frequency	f_{PCLK}	0.8125		52	MHz
Advanced High Performance Bus Clock (HCLK) Frequency	f_{HCLK}	0.8125		52	MHz

¹ The input to the PLL can come from either the high frequency external crystal (HFXTAL), SYS_CLKIN pin or from the high frequency internal RC oscillator (HFOSC).² For the maximum value, the recommended settings are PLL MSEL = 13, PLL NSEL = 16, PLL DIV2 = 1 for PLL input clock = 26 MHz; and PLL MSEL = 13, PLL NSEL = 26, PLL DIV2 = 1 for PLL input clock = 16 MHz; see the [ADuCM4050 Ultra Low Power ARM Cortex-M4F MCU with Integrated Power Management Hardware Reference](#) for more information on these configuration options.³ For the minimum value, the recommended settings are PLL MSEL = 13, PLL NSEL = 30, PLL DIV2 = 0 for PLL input clock = 26 MHz; and PLL MSEL = 8, PLL NSEL = 30, PLL DIV2 = 0 for 16 MHz.

SPI Timing**Table 15.**

Parameter ¹	Symbol	Min	Typ	Max	Unit
SPI MASTER MODE TIMING					
Timing Requirements					
Chip Select (CS) to Serial Clock (SCLK) Edge	t_{CS}	$(2 \times t_{PCLK}) - 6.5$			ns
SCLK Low Pulse Width	t_{SL}	$t_{PCLK} - 3.5$			ns
SCLK High Pulse Width	t_{SH}	$t_{PCLK} - 3.5$			ns
Data Input Setup Time Before SCLK Edge	t_{DSU}	5			ns
Data Input Hold Time After SCLK Edge	t_{DHD}	20			ns
Switching Characteristics					
Data Output Valid After SCLK Edge	t_{DAV}			25	ns
Data Output Setup Before SCLK Edge	t_{DOSU}	$t_{PCLK} - 2.2$			ns
CS High After SCLK Edge	t_{SFS}	$t_{PCLK} + 2$			ns
High Speed SPI (SPIH) MASTER MODE TIMING					
Timing Requirements					
CS to SCLK Edge	t_{CS}	$(2 \times t_{PCLK}) - 6.5$			ns
SCLK Low Pulse Width	t_{SL}	$t_{PCLK} - 2$			ns
SCLK High Pulse Width	t_{SH}	$t_{PCLK} - 2$			ns
Data Input Setup Time Before SCLK Edge	t_{DSU}	3.5			ns
Data Input Hold Time After SCLK Edge	t_{DHD}	12			ns
Switching Characteristics					
Data Output Valid After SCLK Edge	t_{DAV}			12.5	ns
Data Output Setup Before SCLK Edge	t_{DOSU}	$t_{PCLK} - 2.2$			ns
CS High After SCLK Edge	t_{SFS}	$t_{PCLK} + 2$			ns
SPI SLAVE MODE TIMING					
Timing Requirements					
CS to SCLK Edge	t_{CS}	38.5			ns
SCLK Low Pulse Width	t_{SL}	38.5			ns
SCLK High Pulse Width	t_{SH}	38.5			ns
Data Input Setup Time Before SCLK Edge	t_{DSU}	6			ns
Data Input Hold Time After SCLK Edge	t_{DHD}	8			ns
Switching Characteristics					
Data Output Valid After SCLK Edge	t_{DAV}			20	ns
Data Output Valid After CS Edge	t_{DOCS}			20	ns
CS High After SCLK Edge	t_{SFS}	38.5			ns
SPIH SLAVE MODE TIMING					
Timing Requirements					
CS to SCLK Edge	t_{CS}	19.23			ns
SCLK Low Pulse Width	t_{SL}	19.23			ns
SCLK High Pulse Width	t_{SH}	19.23			ns
Data Input Setup Time Before SCLK Edge	t_{DSU}	1			
Data Input Hold Time After SCLK Edge	t_{DHD}	1			
Switching Characteristics					
Data Output Valid After SCLK Edge	t_{DAV}			15	ns
Data Output Valid After CS Edge	t_{DOCS}			15	ns
CS High After SCLK Edge	t_{SFS}	19.23			ns

¹ These specifications are characterized with respect to double drive strength.

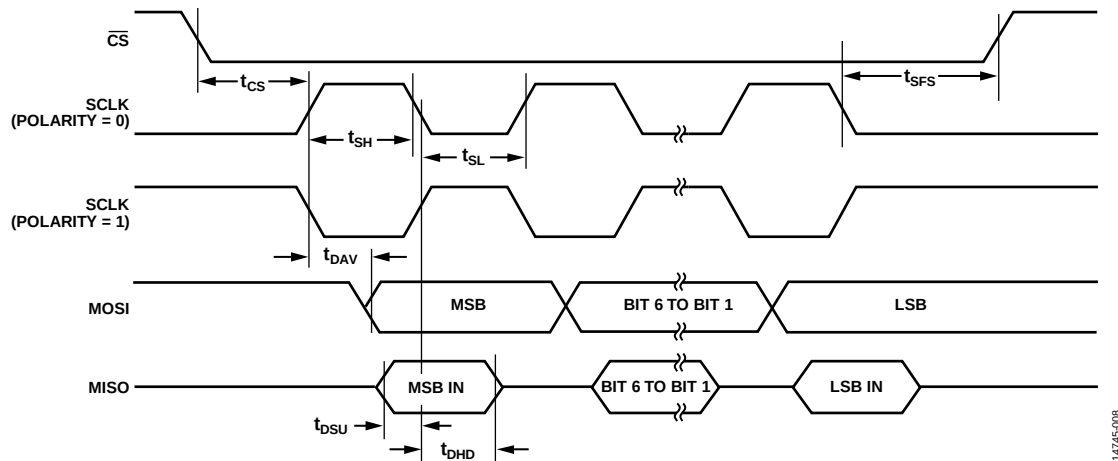


Figure 8. SPI Master Mode Timing (Phase Mode = 1)

14745-008

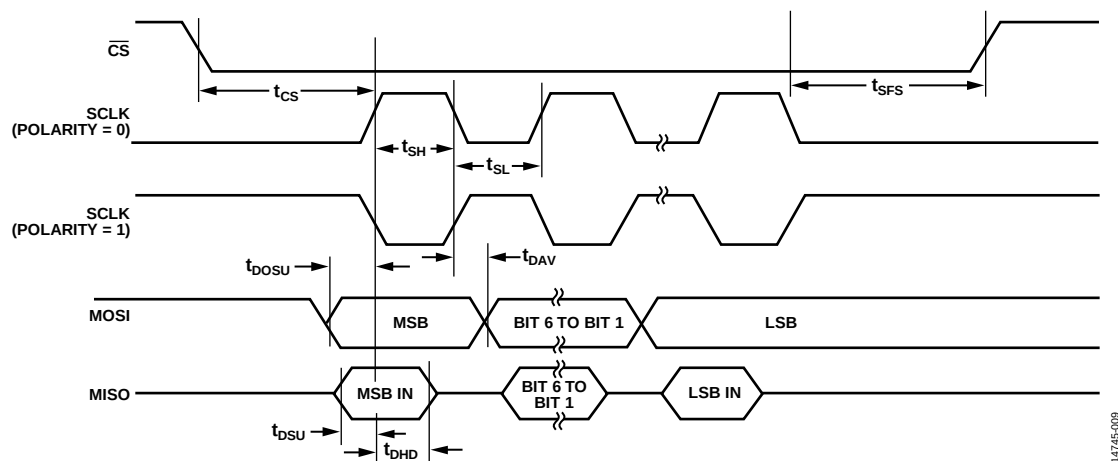


Figure 9. SPI Master Mode Timing (Phase Mode = 0)

14745-009

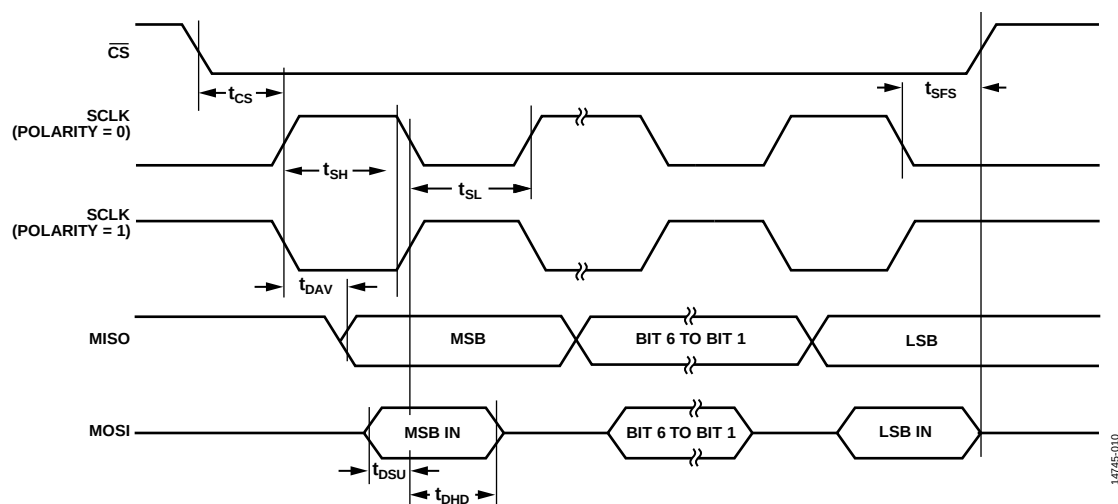
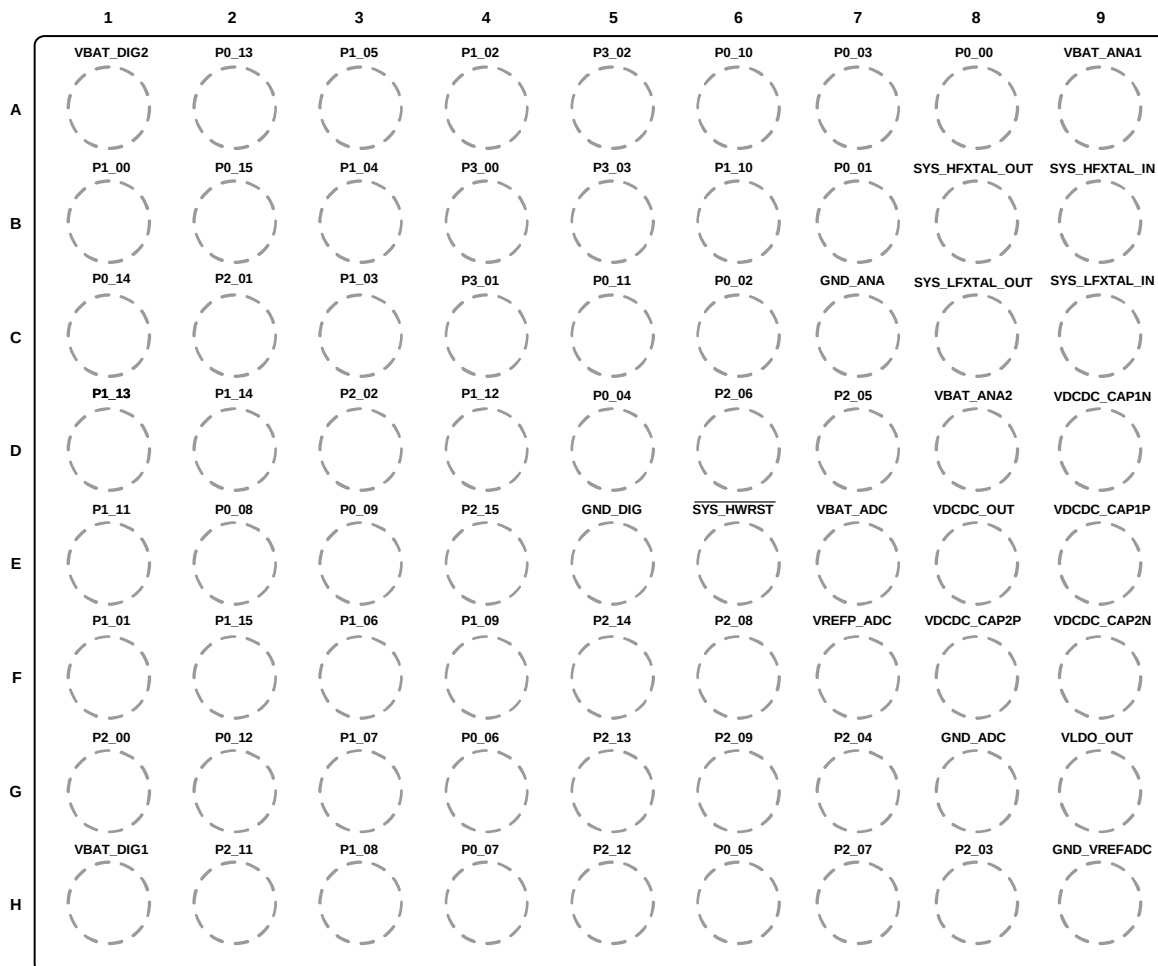


Figure 10. SPI Slave Mode Timing (Phase Mode = 1)

14745-010

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



ADuCM4050
TOP VIEW
(BALL SIDE DOWN)
Not to Scale

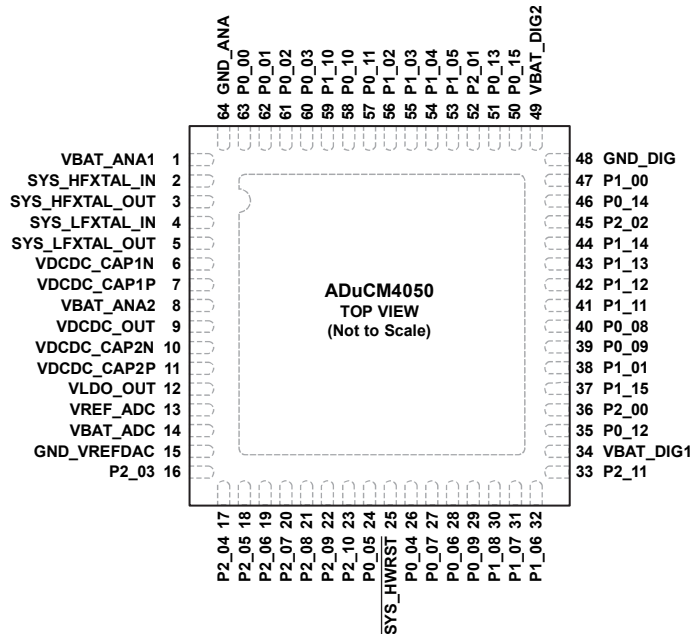
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Figure 14. 72-Ball WLCSP Pin Configuration

Table 22. 72-Ball WLCSP Pin Function Descriptions

Pin No.	Mnemonic	Signal Names	Description
A1	VBAT_DIG2	Not applicable	External Supply for Digital Circuits in the MCU.
A2	P0_13	GPIO13/SYS_WAKE2	GPIO. See the GPIO Multiplexing section for more information.
A3	P1_05	GPIO21, SPI2_CS0	GPIO. See the GPIO Multiplexing section for more information.
A4	P1_02	GPIO18, SPI2_CLK	GPIO. See the GPIO Multiplexing section for more information.
A5	P3_02	GPIO50, RGB_TMR0_3, SPT0_AD0	GPIO. See the GPIO Multiplexing section for more information.
A6	P0_10	GPIO10, UART0_TX	GPIO. See the GPIO Multiplexing section for more information.
A7	P0_03	GPIO03, SPI0_CS0, SPT0_BCNV, SPI2_RDY	GPIO. See the GPIO Multiplexing section for more information.
A8	P0_00	GPIO00, SPI0_CLK, SPT0_BCLK	GPIO. See the GPIO Multiplexing section for more information.
A9	VBAT_ANA1	Not applicable	External Supply for Analog Circuits in the MCU.
B1	P1_00	GPIO16/SYS_WAKE1	GPIO. See the GPIO Multiplexing section for more information.
B2	P0_15	GPIO15/SYS_WAKE0	GPIO. See the GPIO Multiplexing section for more information.
B3	P1_04	GPIO20, SPI2_MISO	GPIO. See the GPIO Multiplexing section for more information.
B4	P3_00	GPIO48, RGB_TMR0_1, SPT0_ACLK	GPIO. See the GPIO Multiplexing section for more information.
B5	P3_03	GPIO51, SPT0_ACNV	GPIO. See the GPIO Multiplexing section for more information.

Pin No.	Mnemonic	Signal Names	Description
B6	P1_10	GPIO26, SPI0_CS1, SYS_CLKIN, SPI1_CS3	GPIO. See the GPIO Multiplexing section for more information.
B7	P0_01	GPIO01, SPI0_MOSI, SPT0_BFS	GPIO. See the GPIO Multiplexing section for more information.
B8	SYS_HFXTAL_OUT	Not applicable	High Frequency Crystal Output.
B9	SYS_HFXTAL_IN	Not applicable	High Frequency Crystal Input.
C1	P0_14	GPIO14, TMR0_OUT, SPI1_RDY	GPIO. See the GPIO Multiplexing section for more information.
C2	P2_01	GPIO33/SYS_WAKE3, TMR2_OUT	GPIO. See the GPIO Multiplexing section for more information.
C3	P1_03	GPIO19, SPI2_MOSI	GPIO. See the GPIO Multiplexing section for more information.
C4	P3_01	GPIO49, RGB_TMR0_2, SPT0_AFS	GPIO. See the GPIO Multiplexing section for more information.
C5	P0_11	GPIO11, UART0_RX	GPIO. See the GPIO Multiplexing section for more information.
C6	P0_02	GPIO02, SPI0_MISO, SPT0_BD0	GPIO. See the GPIO Multiplexing section for more information.
C7	GND_ANA	Not applicable	Ground Reference for Analog Circuits in the MCU.
C8	SYS_LFXTAL_OUT	Not applicable	Low Frequency Crystal Output.
C9	SYS_LFXTAL_IN	Not applicable	Low Frequency Crystal Input.
D1	P1_13	GPIO29, TMR2_OUT	GPIO. See the GPIO Multiplexing section for more information.
D2	P1_14	GPIO30, SPI0_RDY	GPIO. See the GPIO Multiplexing section for more information.
D3	P2_02	GPIO34, SPT0_ACNV, SPI1_CS2	GPIO. See the GPIO Multiplexing section for more information.
D4	P1_12	GPIO28, RTC1_SS2	GPIO. See the GPIO Multiplexing section for more information.
D5	P0_04	GPIO04, I2C0_SCL	GPIO. See the GPIO Multiplexing section for more information.
D6	P2_06	GPIO38, ADC0_VIN3	GPIO. See the GPIO Multiplexing section for more information.
D7	P2_05	GPIO37, ADC0_VIN2	GPIO. See the GPIO Multiplexing section for more information.
D8	VBAT_ANA2	Not applicable	External Supply for Analog Circuits in the MCU.
D9	VDCDC_CAP1N	Not applicable	Buck Converter Capacitor 1 Negative Terminal.
E1	P1_11	GPIO27, TMR1_OUT	GPIO. See the GPIO Multiplexing section for more information.
E2	P0_08	GPIO08, BPR0_TONE_N	GPIO. See the GPIO Multiplexing section for more information.
E3	P0_09	GPIO09, BPR0_TONE_P, SPI2_CS1	GPIO. See the GPIO Multiplexing section for more information.
E4	P2_15	GPIO47, SPI2_CS2, SPI1_CS3, SPI0_CS1	GPIO. See the GPIO Multiplexing section for more information.
E5	GND_DIG	Not applicable	Ground Reference for Digital Circuits in the MCU.
E6	SYS_HWRST	Not applicable	Hardware Reset Pin.
E7	VBAT_ADC	Not applicable	External Supply for Internal ADC.
E8	VDCDC_OUT	Not applicable	Buck Converter Output. This pin is only for connecting the decoupling capacitor. Do not connect to external load.
E9	VDCDC_CAP1P	Not applicable	Buck Converter Capacitor 1 Positive Terminal.
F1	P1_01	SYS_BMODE0, GPIO17	GPIO. See the GPIO Multiplexing section for more information.
F2	P1_15	GPIO31, SPT0_ACLK, UART1_TX	GPIO. See the GPIO Multiplexing section for more information.
F3	P1_06	GPIO22, SPI1_CLK, RGB_TMR0_1	GPIO. See the GPIO Multiplexing section for more information.
F4	P1_09	GPIO25, SPI1_CS0, SWV	GPIO. See the GPIO Multiplexing section for more information.
F5	P2_14	GPIO46, SPI0_CS3	GPIO. See the GPIO Multiplexing section for more information.
F6	P2_08	GPIO40, ADC0_VIN5, SPI0_CS2, RTC1_SS3	GPIO. See the GPIO Multiplexing section for more information.
F7	VREFP_ADC	Not applicable	External Reference Voltage for Internal ADC.
F8	VDCDC_CAP2P	Not applicable	Buck Converter Capacitor 2 Positive Terminal.
F9	VDCDC_CAP2N	Not applicable	Buck Converter Capacitor 2 Negative Terminal.
G1	P2_00	GPIO32, SPT0_AFS, UART1_RX	GPIO. See the GPIO Multiplexing section for more information.
G2	P0_12	GPIO12, SPT0_AD0, UART0_SOUT_EN	GPIO. See the GPIO Multiplexing section for more information.
G3	P1_07	GPIO23, SPI1_MOSI, RGB_TMR0_2	GPIO. See the GPIO Multiplexing section for more information.
G4	P0_06	SWD0_CLK, GPIO06	GPIO. See the GPIO Multiplexing section for more information.
G5	P2_13	GPIO45, UART1_RX, SPI0_CS2	GPIO. See the GPIO Multiplexing section for more information.
G6	P2_09	GPIO41, ADC0_VIN6, SPI0_CS3	GPIO. See the GPIO Multiplexing section for more information.



NOTES
1. EXPOSED PAD. THE EXPOSED PAD MUST BE GROUNDED.

Figure 15. 64-Lead LFCSP Pin Configuration

14746-015

Table 23. 64-Lead LFCSP Pin Function Descriptions

Pin No.	Mnemonic	Signal Names	Description
1	VBAT_ANA1	Not applicable	External Supply for Analog Circuits in the MCU.
2	SYS_HFXTAL_IN	Not applicable	High Frequency Crystal Input.
3	SYS_HFXTAL_OUT	Not applicable	High Frequency Crystal Output.
4	SYS_LFXTAL_IN	Not applicable	Low Frequency Crystal Input.
5	SYS_LFXTAL_OUT	Not applicable	Low Frequency Crystal Output.
6	VDCDC_CAP1N	Not applicable	Buck Converter Capacitor 1 Negative Terminal.
7	VDCDC_CAP1P	Not applicable	Buck Converter Capacitor 1 Positive Terminal.
8	VBAT_ANA2	Not applicable	External Supply for Analog Circuits in the MCU.
9	VDCDC_OUT	Not applicable	Buck Converter Output. This pin is only for connecting the decoupling capacitor. Do not connect to external load.
10	VDCDC_CAP2N	Not applicable	Buck Converter Capacitor 2 Negative Terminal.
11	VDCDC_CAP2P	Not applicable	Buck Converter Capacitor 2 Positive Terminal.
12	VLDO_OUT	Not applicable	Low Dropout Regulator Output. This pin is only for connecting the decoupling capacitor. Do not connect to external load.
13	VREF_ADC	Not applicable	External Reference Voltage for Internal ADC.
14	VBAT_ADC	Not applicable	External Supply for Internal ADC.
15	GND_VREFDAC	Not applicable	Ground for Internal ADC.
16	P2_03	GPIO35, ADC0_VIN0	GPIO. See the GPIO Multiplexing section for more information.
17	P2_04	GPIO36, ADC0_VIN1	GPIO. See the GPIO Multiplexing section for more information.
18	P2_05	GPIO37, ADC0_VIN2	GPIO. See the GPIO Multiplexing section for more information.
19	P2_06	GPIO38, ADC0_VIN3	GPIO. See the GPIO Multiplexing section for more information.
20	P2_07	GPIO39, ADC0_VIN4, SPI2_CS3	GPIO. See the GPIO Multiplexing section for more information.
21	P2_08	GPIO40, ADC0_VIN5, SPI0_CS2, RTC1_SS3	GPIO. See the GPIO Multiplexing section for more information.
22	P2_09	GPIO41, ADC0_VIN6, SPI0_CS3	GPIO. See the GPIO Multiplexing section for more information.
23	P2_10	GPIO42, ADC0_VIN7, SPI2_CS2	GPIO.
24	P0_05	GPIO05, I2C0_SDA	GPIO. See the GPIO Multiplexing section for more information.
25	SYS_HWRST	Not applicable	Hardware Reset Pin.
26	P0_04	GPIO04, I2C0_SCL	GPIO. See the GPIO Multiplexing section for more information.
27	P0_07	SWD0_DATA, GPIO07	GPIO. See the GPIO Multiplexing section for more information.

THEORY OF OPERATION

ARM CORTEX-M4F PROCESSOR

The ARM Cortex-M4F core is a 32-bit reduced instruction set computer (RISC). The length of the data can be 8 bits, 16 bits, or 32 bits. The length of the instruction word is 16 bits or 32 bits. The processor has the following features:

- ARM Cortex-M4F architecture
- Thumb-2 instruction set architecture (ISA) technology
- Three-stage pipeline with branch speculation
- Low latency interrupt processing with tail chaining
- Single-cycle multiply
- Hardware divide instructions
- Nested vectored interrupt controller (NVIC) (72 interrupts and 8 priorities)
- Six hardware breakpoints and one watchpoint (unlimited software breakpoints using the Segger JLink debug probe)
- Bit banding support
- Trace support—instruction trace macrocell (ITM), trace port interface unit (TPIU), and data watchpoint and trace (DWT) triggers and counters
- Memory protection unit (MPU)
- Eight-region MPU with subregions and background region
- Programmable clock generator unit
- Configurable for ultralow power operation
- Deep sleep modes, dynamic power management
- Programmable clock generator unit
- Floating point unit (FPU)
- Supports single-precision add, subtract, multiply, divide, multiply and accumulate, and square root operations
- Provides conversions between fixed point and floating point data formats, and floating point constant instructions

ARM Cortex-M4F Subsystem

The ADuCM4050 MCU memory map (see the [ADuCM4050 Ultra Low Power ARM Cortex-M4F MCU with Integrated Power Management Hardware Reference](#)) is based on the ARM Cortex-M4F memory model. By retaining the standardized memory mapping, it is easier to port applications across ARM Cortex-M4F platforms. The ADuCM4050 application development is based on memory blocks across code and SRAM regions. Sufficient internal memory is available via internal SRAM and internal flash.

Code Region

Accesses in the code region (0x0000_0000 to 0x0007_FFFF except 0x0007_F000 to 0x0007_FFFF, which is meant for protected key storage) are performed by the core and target the memory and cache resources.

SRAM Region

Accesses in the SRAM region (see Figure 22) are performed by the ARM Cortex-M4F core. The SRAM region of the core can act as a data region for an application.

- Internal SRAM data region. This space can contain read/write data. Internal SRAM can be partitioned between code and data (the SRAM region in the ARM Cortex-M4F space) in 32 kB blocks. Access to this region occurs at core clock speed with no wait states. The SRAM data region also supports read/write access by the ARM Cortex-M4F core and read/write DMA access by system devices.
- System memory mapped registers (MMRs). Various system MMRs reside in this region.

System Region

Accesses in this region (0xE000_0000 to 0xFFFF_FFFF) are performed by the ARM Cortex-M4F core and handled within the ARM Cortex-M4F platform. This system region includes the following components:

- CoreSight™ read only memory (ROM). The ROM table entries (see the ARM Cortex-M4F Technical Reference Manual) show the debug components of the processor.
- ARM advanced peripheral bus (APB) peripheral. This space is defined by ARM and occupies the bottom 256 kB of the system region (0xE000_0000 to 0xE004_0000). The space supports read/write access by the ARM Cortex-M4F core to the internal peripherals of the ARM core (NVIC, system control space (SCS), and wake-up interrupt controller (WIC)) and CoreSight ROM. It is not accessible by system DMA.
- Platform control register. This space has registers within the ARM Cortex-M4F platform component that control the ARM core, its memory, and the code cache. It is accessible by the ARM Cortex-M4F core (but not accessible by system DMA).

Clocking

The ADuCM4050 MCU has the following clocking options:

- High frequency clocks
 - Internal high frequency oscillator (HFOSC) at 26 MHz
 - High frequency external crystal oscillator (HFXTAL) at 26 MHz or 16 MHz
 - GPIO clock in (SYS_CLKIN)
 - Phase-locked loop (PLL)
- Low frequency clocks at 32 kHz
 - Internal low frequency oscillator (LFOSC)
 - Low frequency external crystal oscillator (LFXTAL)

The clock options have software configurability with the following exceptions: the HFOSC cannot be disabled when using an internal buck regulator, and the LFOSC cannot be disabled even if using LFXTAL.

Clock sources with a frequency greater than 26 MHz can be achieved by using a PLL. The maximum frequency sourced from the PLL is 52 MHz.

When core frequency is greater than 26 MHz, program the flash wait states to 1.

As PLL is disabled and relock is transparent to user software, hibernate mode can enter and exit seamlessly when the system frequency is sourced from PLL.

Clock Fail Detection

The LFOSC clock continuously monitors the LFXTAL in hibernate, active, and flexi power modes. If the LFXTAL stops running, there is an option to detect and generate an interrupt and/or automatically switch to the LFOSC without software intervention. The HFOSC clock monitors the HFXTAL clock, GPIO clock, and the PLL clock. If using any of these clocks as the system clock and it fails to toggle, the clock can be detected through an interrupt. There is an option to automatically switch to the HFOSC.

Real-Time Clock (RTC)

The ADuCM4050 MCU has two RTC blocks: RTC0 and RTC1, also called flexible real-time clock (FLEX_RTC™). The RTC blocks share a low power crystal oscillation circuit that operates in conjunction with a 32,768 Hz external crystal.

The RTC has an alarm that interrupts the core when the programmed alarm value matches the RTC count. The software enables and configures the RTC.

The RTC also has a digital trim capability to allow a positive or negative adjustment to the RTC count at fixed intervals.

The FLEX_RTC supports three SensorStrobe outputs: RTC1_SS1, RTC1_SS2, and RTC1_SS3 (see the [ADuCM4050 Ultra Low Power ARM Cortex-M4F MCU with Integrated Power Management Hardware Reference](#)). Using this mechanism, the ADuCM4050 MCU can be used as a programmable clock generator in all power modes except shutdown mode. In this way, the external sensors can have their timing domains mastered by the ADuCM4050 MCU, as the SensorStrobe output is a programmable divider from the FLEX_RTC, which can operate at 0.5 Hz to 16.384 kHz. The sensors and MCU are in sync, which removes the need for additional resampling of data to time align it.

In the absence of the SensorStrobe mechanism, the external sensor uses an RC oscillator (approximately $\pm 30\%$ typical variation). The MCU must sample the data and resample it on the time domain of the MCU before using it.

Alternatively, the MCU remains in a higher power state and drives each data conversion on the sensor side.

The SensorStrobe mechanism allows the ADuCM4050 MCU to be in a lower power state for a long duration and avoids unnecessary data processing, extending the battery life of the end product. The key differences between RTC0 and RTC1 are shown in Table 26.

Table 26. RTC Features

Features	RTC0	RTC1 (FLEX_RTC)
Resolution of Time Base (Prescaling)	Counts time at 1 Hz in units of seconds. Operationally, RTC0 always prescales to 1 Hz (for example, divide by 32,768) and always counts real time in units of seconds.	Can prescale the clock by any power of two from 0 to 15. It can count time in units of any of these 16 possible prescale settings. For example, the clock can be prescaled by 1, 2, 4, 8, ..., 16,384, or 32,768.
Source Clock	LFXTAL.	Depending on the low frequency multiplexer configuration, the RTC is clocked by the LFXTAL or the LFOSC.
Wake-Up Timer	Wake-up time is specified in units of seconds.	Supports alarm times down to a resolution of 30.52 μ s, that is, where the time is specified down to a specific 32 kHz clock cycle.
Number of Alarms	One alarm only. Uses an absolute, nonrepeating alarm time, specified in units of 1 sec.	Two alarms. One absolute alarm time and one periodic alarm, repeating every 60 prescaled time units.
SensorStrobe Mechanism	Not available.	Four independent channels with fine control on duty cycle and frequency (0.5 Hz to 16.384 kHz). SensorStrobe is an alarm function in the RTC that can send an output pulse via GPIOs to an external device to instruct that device to take a measurement or perform some action at a specific time. SensorStrobe events are scheduled at a specific target time relative to the real-time count of the RTC. SensorStrobe can be enabled in active, flexi, and hibernate modes.
Input Capture	Not available.	Input capture takes a snapshot of the RTC real-time count when an external device signals an event via a transition on one of the GPIO inputs to the ADuCM4050 MCU. Typically, an input capture event is triggered by an autonomous measurement or action on such a device, which then signals to the ADuCM4050 MCU that the RTC must take a snapshot of time corresponding to the event. Taking this snapshot can wake up the ADuCM4050 MCU and cause an interrupt to the CPU. The CPU can subsequently obtain information from the RTC on the exact 32 kHz cycle on which the input capture event occurred.
Input Sampling	Not available.	Each SensorStrobe channel has up to three separate GPIO inputs from an external device, which can be sampled based on the output pulse sent to the external device. Each channel can be configured to interrupt the ADuCM4050 MCU when any activity happens on these GPIO inputs from the external device. These inputs can broadcast sensor states such as first in, first out (FIFO) buffer full, switch open, and threshold crossed. This feature allows the ADuCM4050 MCU to remain in a low power state and wake up to process the data only when a specific programmed sequence from an external device is detected.

DEVELOPMENT SUPPORT

Development support for the ADuCM4050 MCU includes documentation, evaluation hardware, and development software tools.

Documentation

The [ADuCM4050 Ultra Low Power ARM Cortex-M4F MCU with Integrated Power Management Hardware Reference](#) details the functionality of each block on the ADuCM4050 MCU. It includes power management, clocking, memories, and peripherals.

The [ADuCM4050 Ultra Low Power ARM Cortex-M4F MCU with Integrated Power Management Hardware Reference](#) can be ordered from any Analog Devices sales office or accessed electronically on the Analog Devices website at www.analog.com.

Hardware

The [EV-COG-AD4050LZ](#) is available to prototype sensor configuration with the ADuCM4050 MCU.

Software

The [EV-COG-AD4050LZ](#) includes a complete development and debug environment for the ADuCM4050 MCU. The device family pack for the ADuCM4050 MCU is provided for the IAR Embedded Workbench for ARM, Keil™, and CrossCore® embedded studio (CCES) environments.

The device family pack also includes operating system (OS) aware drivers and example code for peripherals on the device.

REFERENCE DESIGNS

The [Circuits from the Lab®](#) web page provides the following for the ADuCM4050 reference design:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

SECURITY FEATURES DISCLAIMER

To the knowledge of Analog Devices, the security features, when used in accordance with the data sheet and hardware reference manual specifications, provide a secure method of implementing code and data safeguards. However, Analog Devices does not guarantee that this technology provides absolute security. Accordingly, analog devices hereby disclaims any and all express and implied warranties that the security features cannot be breached, compromised, or otherwise circumvented and in no event is Analog Devices liable for any loss, damage, destruction, or release of data, information, physical property, or intellectual property.

MCU TEST CONDITIONS

The ac signal specifications (timing parameters) appearing in this data sheet include output disable time, output enable time, and others. Timing is measured on signals when they cross the voltage threshold (V_{MEAS}) level as described in Figure 24. All delays (in nanoseconds or microseconds) are measured between the point that the first signal reaches V_{MEAS} and the point that the second signal reaches V_{MEAS} . The value of V_{MEAS} is set to $V_{BAT}/2$. The tester pin electronics is shown in Figure 25.

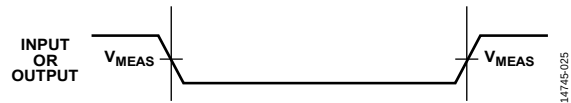
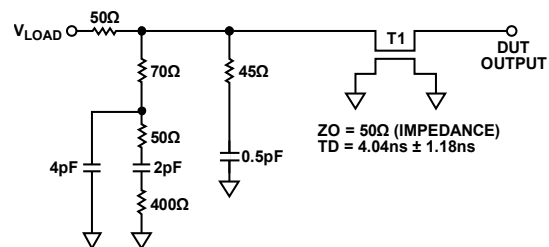


Figure 24. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)



NOTES

1. THE WORST-CASE TRANSMISSION LINE DELAY (TD) IS SHOWN AND CAN BE USED FOR THE OUTPUT TIMING ANALYSIS TO REFLECT THE TRANSMISSION LINE EFFECT AND MUST BE CONSIDERED. TRANSMISSION LINE IS FOR LOAD ONLY AND DOES NOT AFFECT THE DATA SHEET TIMING SPECIFICATIONS.
2. ANALOG DEVICES RECOMMENDS USING THE IBIS MODEL TIMING FOR A GIVEN SYSTEM REQUIREMENT. IF NECESSARY, A SYSTEM CAN INCORPORATE EXTERNAL DRIVERS TO COMPENSATE FOR ANY TIMING DIFFERENCES.

Figure 25. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

DRIVER TYPES

Table 27 shows the driver types.

Table 27. Driver Types

Driver Type ^{1,2,3}	Associated Pins
Type A	P0_00 to P0_03, P0_07, P0_10 to P0_13, P0_15, P1_00 to P1_10, P1_15, P2_00, P2_01, P2_04 to P2_14, P3_00 to P3_03, and SYS_HWRST
Type B	P0_08, P0_09, P0_14, P1_11 to P1_14, and P2_02
Type C	P0_04 and P0_05
Type D	P0_06

¹ In single drive mode, the maximum source/sink capacity is 2 mA.

² In double drive mode, the maximum source/sink capacity is 4 mA.

³ At maximum drive capacity, only 16 GPIOs are allowed to switch at any given point in time.

EEMBC ULPMARK™-CP SCORE

Using the following software configuration and the profile configuration shown in Table 28, the EEMBC ULPMark-CP score is 189.

- Compiler name and version: IAR EWARM 8.20.1
- Compiler flags:

```
--no_size_constraints --cpu=Cortex-M4 -D
__ADUCM4050__ --no_code_motion -Ohs -e --
fpu=VFPv4_sp --endian=little
```
- ULPBench Profile and Version: Core Profile v1.1
- EnergyMonitor Software Version: V2.0

Table 28. EEMBC ULPMark™-CP Profile Configuration

Profile Configuration	Value
Wake-Up Timer Module	RTC1
Wake-Up Timer Clock Source	External crystal
Wake-Up Timer Frequency	32768 Hz
Wake-Up Timer Accuracy	20 ppm
Active Power Mode Name	Active mode
Active Mode Clock Configuration	52 MHz (CPU), 32 kHz (RTC)
Active Mode Voltage Integrity	1.74 V
Inactive Power Mode Name	Hibernate
Inactive Clock Configuration	Off (CPU), 32 kHz (RTC)
Inactive Mode Voltage Integrity	1.74 V

APPLICATIONS INFORMATION

This section contains circuit diagrams that show the recommended external components for proper operation of the ADuCM4050 in example application scenarios.

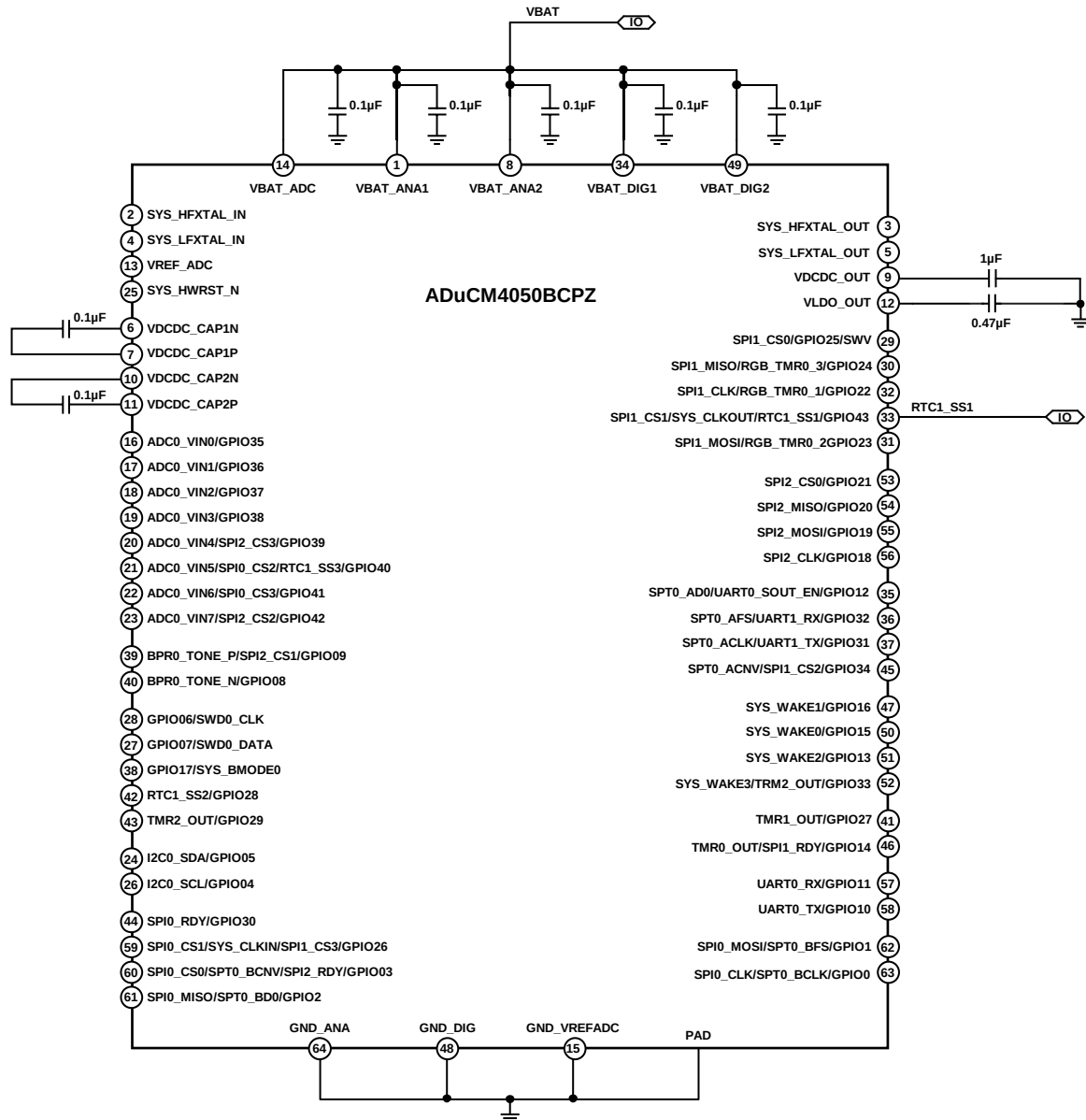


Figure 26. Recommended External Components when Using the Internal Buck Converter

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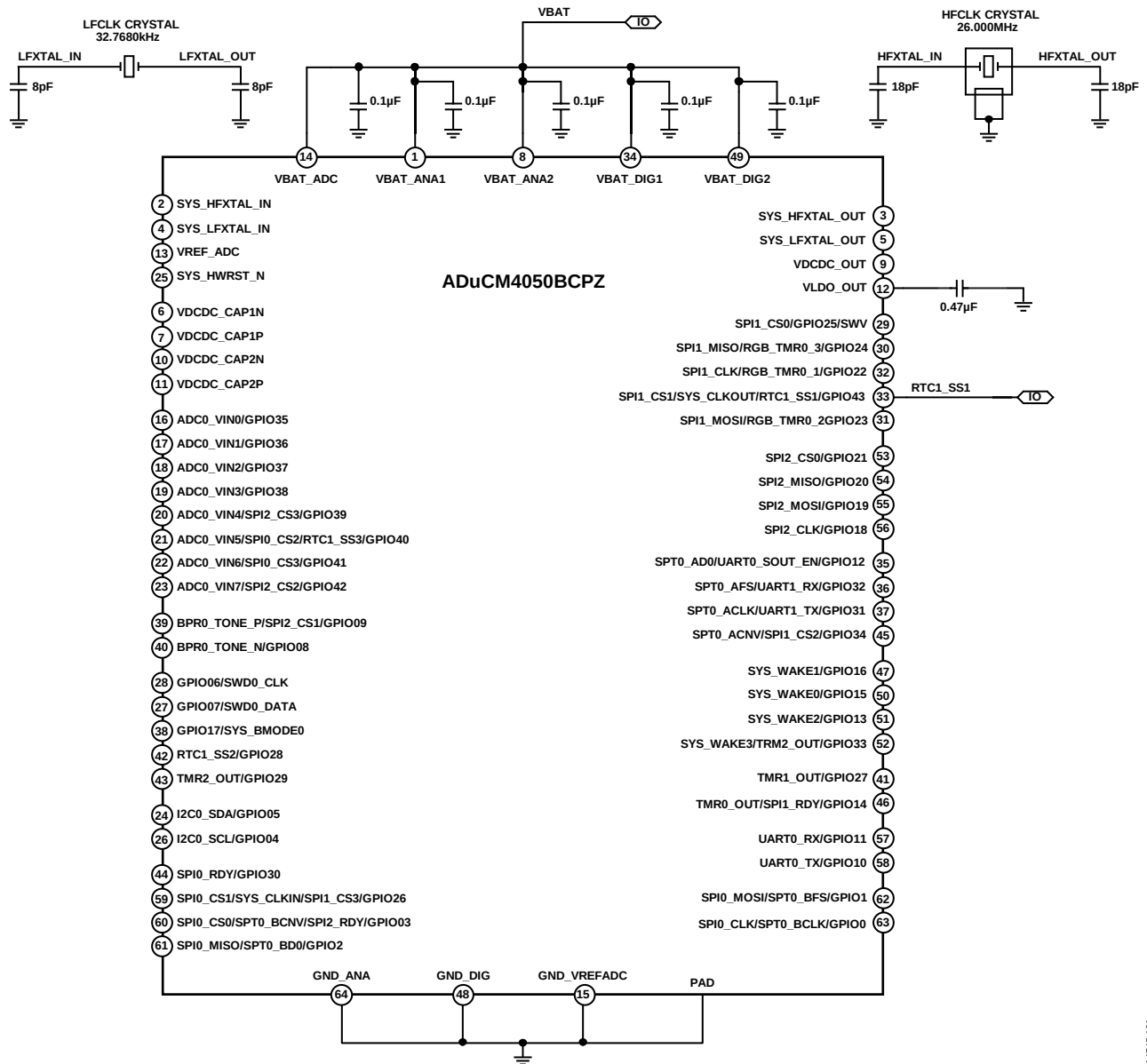


Figure 27. Recommended External Components when Using LFXTAL and HFXTAL

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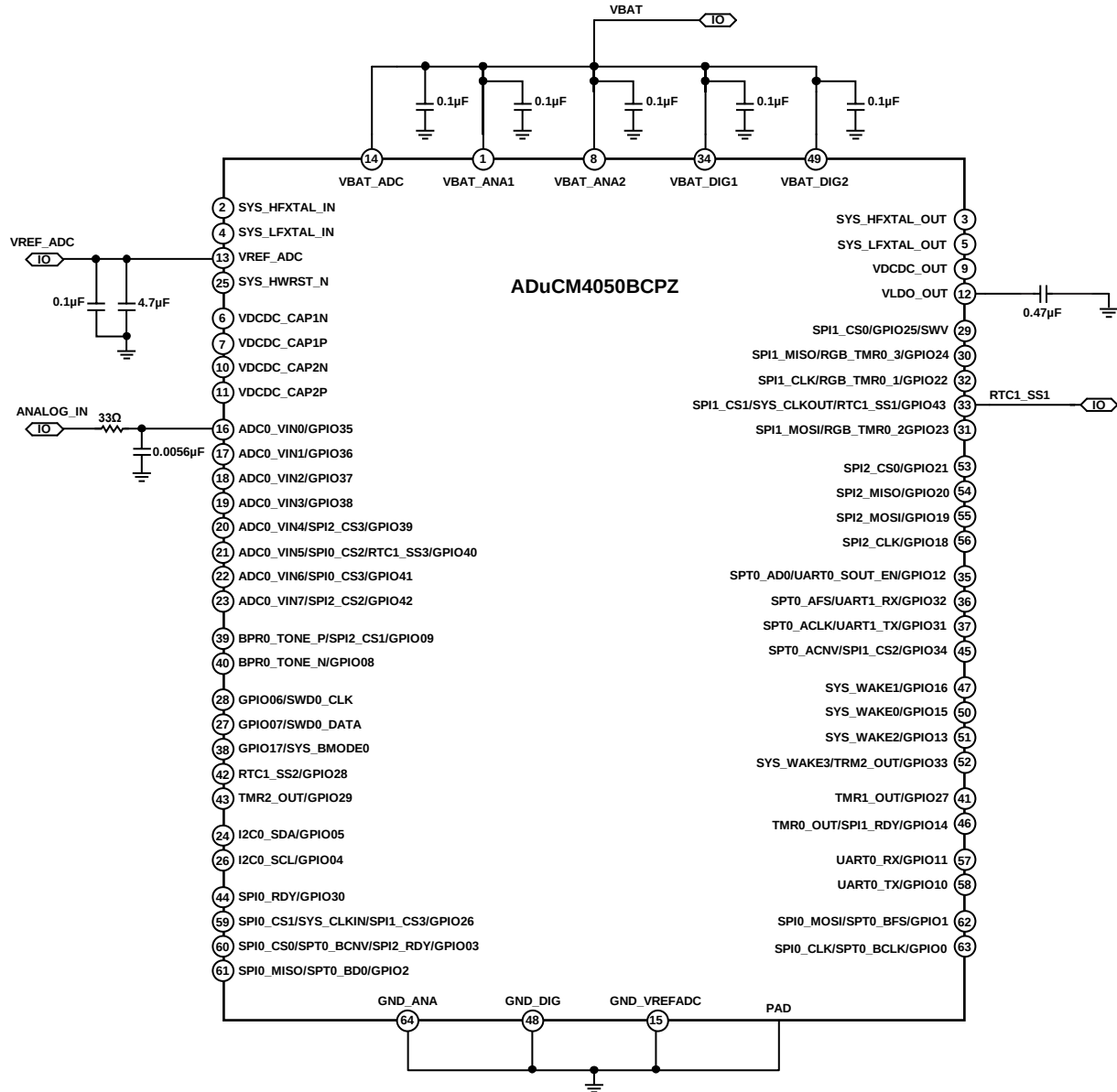


Figure 28. Recommended External Components on VREF_ADC Pin and ADC Input Channel (ADC0_VIN0 Used as Example) when Using the Internal ADC

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SECTION 1. ADuCM4050 FUNCTIONALITY ISSUES

Reference No.	Description	Status
21000011	I ² C master mode fails to generate clock when clock dividers are too small	Identified
21000016	Possible receive data loss with I ² C automatic clock stretching	Identified
21000017	SPI read command mode does not work properly when SPI_CNT is 1 and DMA is enabled	Identified

This completes the Silicon Anomaly section.