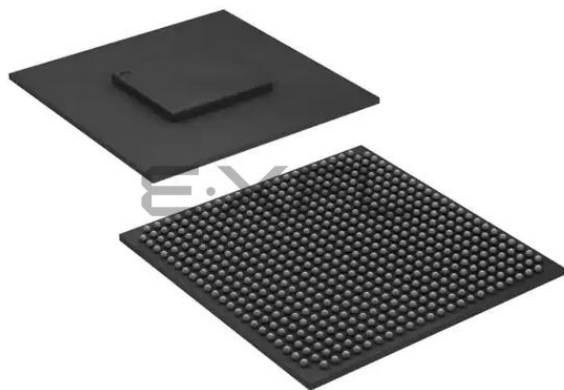




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	4964
Number of Logic Elements/Cells	118143
Total RAM Bits	8315904
Number of I/O	260
Number of Gates	-
Voltage - Supply	0.87V ~ 0.93V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	572-BGA, FCBGA
Supplier Device Package	572-FBGA, FC (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2agx125df25i3



Conditions beyond those listed in Table 1–1 and Table 1–2 may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Table 1–1 lists the absolute maximum ratings for Arria II GX devices.

Table 1–1. Absolute Maximum Ratings for Arria II GX Devices

Symbol	Description	Minimum	Maximum	Unit
V_{CC}	Supplies power to the core, periphery, I/O registers, PCI Express® (PIPE) (PCIe) HIP block, and transceiver PCS	–0.5	1.35	V
V_{CCCB}	Supplies power for the configuration RAM bits	–0.5	1.8	V
V_{CCBAT}	Battery back-up power supply for design security volatile key register	–0.5	3.75	V
V_{CCPD}	Supplies power to the I/O pre-drivers, differential input buffers, and MSEL circuitry	–0.5	3.75	V
V_{CCIO}	Supplies power to the I/O banks	–0.5	3.9	V
V_{CCD_PLL}	Supplies power to the digital portions of the PLL	–0.5	1.35	V
V_{CCA_PLL}	Supplies power to the analog portions of the PLL and device-wide power management circuitry	–0.5	3.75	V
V_I	DC input voltage	–0.5	4.0	V
I_{OUT}	DC output current, per pin	–25	40	mA
V_{CCA}	Supplies power to the transceiver PMA regulator	—	3.75	V
V_{CCL_GXB}	Supplies power to the transceiver PMA TX, PMA RX, and clocking	—	1.21	V
V_{CCH_GXB}	Supplies power to the transceiver PMA output (TX) buffer	—	1.8	V
T_J	Operating junction temperature	–55	125	°C
T_{STG}	Storage temperature (no bias)	–65	150	°C

Table 1–2 lists the absolute maximum ratings for Arria II GZ devices.

Table 1–2. Absolute Maximum Ratings for Arria II GZ Devices (Part 1 of 2)

Symbol	Description	Minimum	Maximum	Unit
V_{CC}	Supplies power to the core, periphery, I/O registers, PCIe HIP block, and transceiver PCS	–0.5	1.35	V
V_{CCCB}	Power supply to the configuration RAM bits	–0.5	1.8	V
V_{CCPGM}	Supplies power to the configuration pins	–0.5	3.75	V
V_{CCAUX}	Auxiliary supply	–0.5	3.75	V
V_{CCBAT}	Supplies battery back-up power for design security volatile key register	–0.5	3.75	V
V_{CCPD}	Supplies power to the I/O pre-drivers, differential input buffers, and MSEL circuitry	–0.5	3.75	V
V_{CCIO}	Supplies power to the I/O banks	–0.5	3.9	V
V_{CC_CLKIN}	Supplies power to the differential clock input	–0.5	3.75	V
V_{CCD_PLL}	Supplies power to the digital portions of the PLL	–0.5	1.35	V
V_{CCA_PLL}	Supplies power to the analog portions of the PLL and device-wide power management circuitry	–0.5	3.75	V
V_I	DC input voltage	–0.5	4.0	V
I_{OUT}	DC output current, per pin	–25	40	mA

Table 1–3. Maximum Allowed Overshoot During Transitions for Arria II Devices

Symbol	Description	Condition (V)	Overshoot Duration as % of High Time	Unit
V_I (AC)	AC Input Voltage	4.0	100.000	%
		4.05	79.330	%
		4.1	46.270	%
		4.15	27.030	%
		4.2	15.800	%
		4.25	9.240	%
		4.3	5.410	%
		4.35	3.160	%
		4.4	1.850	%
		4.45	1.080	%
		4.5	0.630	%
		4.55	0.370	%
		4.6	0.220	%

Maximum Allowed I/O Operating Frequency

Table 1–4 lists the maximum allowed I/O operating frequency for Arria II GX I/Os using the specified I/O standards to ensure device reliability.

Table 1–4. Maximum Allowed I/O Operating Frequency for Arria II GX Devices

I/O Standard	I/O Frequency (MHz)
HSTL-18 and HSTL-15	333
SSTL -15	400
SSTL-18	333
2.5-V LVCMOS	260
3.3-V and 3.0-V LVTTTL	250
3.3-V, 3.0-V, 1.8-V, and 1.5-V LVCMOS	
PCI and PCI-X	
SSTL-2	
1.2-V LVCMOS HSTL-12	200

Recommended Operating Conditions

This section lists the functional operation limits for AC and DC parameters for Arria II GX and GZ devices. All supplies are required to monotonically reach their full-rail values without plateaus within t_{RAMP} .

Table 1–5 lists the recommended operating conditions for Arria II GX devices.

Table 1–5. Recommended Operating Conditions for Arria II GX Devices (Note 1) (Part 1 of 2)

Symbol	Description	Condition	Minimum	Typical	Maximum	Unit
V_{CC}	Supplies power to the core, periphery, I/O registers, PCIe HIP block, and transceiver PCS	—	0.87	0.90	0.93	V
V_{CCCB}	Supplies power to the configuration RAM bits	—	1.425	1.50	1.575	V
V_{CCBAT} (2)	Battery back-up power supply for design security volatile key registers	—	1.2	—	3.3	V
V_{CCPD} (3)	Supplies power to the I/O pre-drivers, differential input buffers, and MSEL circuitry	—	3.135	3.3	3.465	V
		—	2.85	3.0	3.15	V
		—	2.375	2.5	2.625	V
V_{CCIO}	Supplies power to the I/O banks (4)	—	3.135	3.3	3.465	V
		—	2.85	3.0	3.15	V
		—	2.375	2.5	2.625	V
		—	1.71	1.8	1.89	V
		—	1.425	1.5	1.575	V
		—	1.14	1.2	1.26	V
V_{CCD_PLL}	Supplies power to the digital portions of the PLL	—	0.87	0.90	0.93	V
V_{CCA_PLL}	Supplies power to the analog portions of the PLL and device-wide power management circuitry	—	2.375	2.5	2.625	V
V_I	DC Input voltage	—	–0.5	—	3.6	V
V_O	Output voltage	—	0	—	V_{CCIO}	V
V_{CCA}	Supplies power to the transceiver PMA regulator	—	2.375	2.5	2.625	V
V_{CCL_GXB}	Supplies power to the transceiver PMA TX, PMA RX, and clocking	—	1.045	1.1	1.155	V
V_{CCH_GXB}	Supplies power to the transceiver PMA output (TX) buffer	—	1.425	1.5	1.575	V
T_J	Operating junction temperature	Commercial	0	—	85	°C
		Industrial	–40	—	100	°C

Use the following with Equation 1-1:

- R_{SCAL} is the OCT resistance value at power up.
- ΔT is the variation of temperature with respect to the temperature at power up.
- ΔV is the variation of voltage with respect to the V_{CCIO} at power up.
- dR/dT is the percentage change of R_{SCAL} with temperature.
- dR/dV is the percentage change of R_{SCAL} with voltage.

Table 1-14 lists the OCT variation with temperature and voltage after power-up calibration for Arria II GX devices.

Table 1-14. OCT Variation after Power-up Calibration for Arria II GX Devices

Nominal Voltage V_{CCIO} (V)	dR/dT (%/°C)	dR/dV (%/mV)
3.0	0.262	0.035
2.5	0.234	0.039
1.8	0.219	0.086
1.5	0.199	0.136
1.2	0.161	0.288

Table 1-15 lists the OCT variation with temperature and voltage after power-up calibration for Arria II GZ devices.

Table 1-15. OCT Variation after Power-Up Calibration for Arria II GZ Devices (Note 1)

Nominal Voltage, V_{CCIO} (V)	dR/dT (%/°C)	dR/dV (%/mV)
3.0	0.189	0.0297
2.5	0.208	0.0344
1.8	0.266	0.0499
1.5	0.273	0.0744
1.2	0.317	0.1241

Note to Table 1-15:

(1) Valid for V_{CCIO} range of $\pm 5\%$ and temperature range of 0° to 85°C.

Pin Capacitance

Table 1-16 lists the pin capacitance for Arria II GX devices.

Table 1-16. Pin Capacitance for Arria II GX Devices

Symbol	Description	Typical	Unit
C_{IO}	Input capacitance on I/O pins, dual-purpose pins (differential I/O, clock, R_{up} , R_{dn}), and dedicated clock input pins	7	pF

I/O Standard Specifications

Table 1-22 through Table 1-35 list input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards supported by the Arria II device family. They also show the Arria II device family I/O standard specifications. V_{OL} and V_{OH} values are valid at the corresponding I_{OH} and I_{OL} , respectively.



For an explanation of terms used in Table 1-22 through Table 1-35, refer to “Glossary” on page 1-74.

Table 1-22 lists the single-ended I/O standards for Arria II GX devices.

Table 1-22. Single-Ended I/O Standards for Arria II GX Devices

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
3.3 V LVTTTL	3.135	3.3	3.465	-0.3	0.8	1.7	3.6	0.45	2.4	4	-4
3.3 V LVCMOS	3.135	3.3	3.465	-0.3	0.8	1.7	3.6	0.2	$V_{CCIO} - 0.2$	2	-2
3.0 V LVTTTL	2.85	3	3.15	-0.3	0.8	1.7	$V_{CCIO} + 0.3$	0.45	2.4	4	-4
3.0 V LVCMOS	2.85	3	3.15	-0.3	0.8	1.7	$V_{CCIO} + 0.3$	0.2	$V_{CCIO} - 0.2$	0.1	-0.1
2.5 V LVCMOS	2.375	2.5	2.625	-0.3	0.7	1.7	$V_{CCIO} + 0.3$	0.4	2	1	-1
1.8 V LVCMOS	1.71	1.8	1.89	-0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	0.45	$V_{CCIO} - 0.45$	2	-2
1.5 V LVCMOS	1.425	1.5	1.575	-0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	2	-2
1.2 V LVCMOS	1.14	1.2	1.26	-0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	2	-2
3.0-V PCI	2.85	3	3.15	—	$0.3 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.1 \times V_{CCIO}$	$0.9 \times V_{CCIO}$	1.5	-0.5
3.0-V PCI-X	2.85	3	3.15	—	$0.35 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.1 \times V_{CCIO}$	$0.9 \times V_{CCIO}$	1.5	-0.5

Table 1-23 lists the single-ended I/O standards for Arria II GZ devices.

Table 1-23. Single-Ended I/O Standards for Arria II GZ Devices (Part 1 of 2)

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
LVTTTL	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.4	2.4	2	-2
LVCMOS	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.2	$V_{CCIO} - 0.2$	0.1	-0.1
2.5 V	2.375	2.5	2.625	-0.3	0.7	1.7	3.6	0.4	2	1	-1
1.8 V	1.71	1.8	1.89	-0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	0.45	$V_{CCIO} - 0.45$	2	-2
1.5 V	1.425	1.5	1.575	-0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	2	-2

Table 1–33 lists the differential I/O standard specifications for Arria II GZ devices.

Table 1–33. Differential I/O Standard Specifications for Arria II GZ Devices (Note 1)

I/O Standard (2)	V _{CCIO} (V)			V _{ID} (mV)			V _{ICM(DC)} (V)		V _{OD} (V) (3)			V _{OCM} (V) (3)		
	Min	Typ	Max	Min	Cond.	Max	Min	Max	Min	Typ	Max	Min	Typ	Max
2.5 V LVDS (HIO)	2.375	2.5	2.625	100	V _{CM} = 1.25 V	—	0.05	1.8	0.247	—	0.6	1.125	1.25	1.375
2.5 V LVDS (VIO)	2.375	2.5	2.625	100	V _{CM} = 1.25 V	—	0.05	1.8	0.247	—	0.6	1	1.25	1.5
RSDS (HIO)	2.375	2.5	2.625	100	V _{CM} = 1.25 V	—	0.3	1.4	0.1	0.2	0.6	0.5	1.2	1.4
RSDS (VIO)	2.375	2.5	2.625	100	V _{CM} = 1.25 V	—	0.3	1.4	0.1	0.2	0.6	0.5	1.2	1.5
Mini-LVDS (HIO)	2.375	2.5	2.625	200	—	600	0.4	1.32 5	0.25	—	0.6	1	1.2	1.4
Mini-LVDS (VIO)	2.375	2.5	2.625	200	—	600	0.4	1.32 5	0.25	—	0.6	1	1.2	1.5
LVPECL	2.375	2.5	2.625	300	—	—	0.6	1.8	—	—	—	—	—	—
BLVDS (4)	2.375	2.5	2.625	100	—	—	—	—	—	—	—	—	—	—

Notes to Table 1–33:

- (1) 1.4-V/1.5-V PCML transceiver I/O standard specifications are described in “Transceiver Performance Specifications” on page 1–21.
- (2) Vertical I/O (VIO) is top and bottom I/Os; horizontal I/O (HIO) is left and right I/Os.
- (3) R_L range: 90 ≤ R_L ≤ 110 Ω.
- (4) There are no fixed V_{ICM}, V_{OD}, and V_{OCM} specifications for BLVDS. These specifications depend on the system topology.

Power Consumption for the Arria II Device Family

Altera offers two ways to estimate power for a design:

- Using the Microsoft Excel-based Early Power Estimator
- Using the Quartus® II PowerPlay Power Analyzer feature

The interactive Microsoft Excel-based Early Power Estimator is typically used prior to designing the FPGA in order to get a magnitude estimate of the device power. The Quartus II PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after place-and-route is complete. The PowerPlay Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities which, when combined with detailed circuit models, can yield very accurate power estimates.



For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in volume 3 of the *Quartus II Handbook*.

Table 1–34. Transceiver Specifications for Arria II GX Devices (Note 1) (Part 3 of 7)

Symbol/ Description	Condition	I3			C4			C5 and I5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
fixedclk clock frequency	PCIe Receiver Detect	—	125	—	—	125	—	—	125	—	—	125	—	MHz
reconfig_clk clock frequency	Dynamic reconfig. clock frequency	2.5/ 37.5 (4)	—	50	2.5/ 37.5 (4)	—	50	2.5/ 37.5 (4)	—	50	2.5/ 37.5 (4)	—	50	MHz
Delta time between reconfig_clks (5)	—	—	—	2	—	—	2	—	—	2	—	—	2	ms
Transceiver block minimum power-down pulse width	—	—	1	—	—	1	—	—	1	—	—	1	—	μs
Receiver														
Supported I/O Standards	1.4-V PCML, 1.5-V PCML, 2.5-V PCML, 2.5-V PCML, LVPECL, and LVDS													
Data rate (13)	—	600	—	6375	600	—	3750	600	—	3750	600	—	3125	Mbps
Absolute V _{MAX} for a receiver pin (6)	—	—	—	1.5	—	—	1.5	—	—	1.5	—	—	1.5	V
Absolute V _{MIN} for a receiver pin	—	-0.4	—	—	-0.4	—	—	-0.4	—	—	-0.4	—	—	V
Maximum peak-to-peak differential input voltage V _{ID} (diff p-p)	V _{ICM} = 0.82 V setting	—	—	2.7	—	—	2.7	—	—	2.7	—	—	2.7	V
	V _{ICM} = 1.1 V setting (7)	—	—	1.6	—	—	1.6	—	—	1.6	—	—	1.6	V

Table 1–39. Transmitter Pre-Emphasis Levels for Arria II GZ Devices (Part 2 of 2)

Pre-Emphasis 1st Post-Tap Setting	V _{OD} Setting							
	0	1	2	3	4	5	6	7
29	N/A	N/A	N/A	12.5	9.6	7.7	6.3	4.3
30	N/A	N/A	N/A	N/A	11.4	9	7.4	N/A
31	N/A	N/A	N/A	N/A	12.9	10	8.2	N/A

Table 1–40 lists the transceiver jitter specifications for all supported protocols for Arria II GX devices.

Table 1–40. Transceiver Block Jitter Specifications for Arria II GX Devices (Note 1) (Part 1 of 10)

Symbol/ Description	Conditions	I3			C4			C5, I5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SONET/SDH Transmit Jitter Generation (2)														
Peak-to-peak jitter at 622.08 Mbps	Pattern = PRBS15	—	—	0.1	—	—	0.1	—	—	0.1	—	—	0.1	UI
RMS jitter at 622.08 Mbps	Pattern = PRBS15	—	—	0.01	—	—	0.01	—	—	0.01	—	—	0.01	UI
Peak-to-peak jitter at 2488.32 Mbps	Pattern = PRBS15	—	—	0.1	—	—	0.1	—	—	0.1	—	—	0.1	UI
RMS jitter at 2488.32 Mbps	Pattern = PRBS15	—	—	0.01	—	—	0.01	—	—	0.01	—	—	0.01	UI
SONET/SDH Receiver Jitter Tolerance (2)														
Jitter tolerance at 622.08 Mbps	Jitter frequency = 0.03 KHz Pattern = PRBS15	> 15			> 15			> 15			> 15			UI
	Jitter frequency = 25 KHZ Pattern = PRBS15	> 1.5			> 1.5			> 1.5			> 1.5			UI
	Jitter frequency = 250 KHz Pattern = PRBS15	> 0.15			> 0.15			> 0.15			> 0.15			UI

Table 1-40. Transceiver Block Jitter Specifications for Arria II GX Devices (Note 1) (Part 7 of 10)

Symbol/ Description	Conditions	I3			C4			C5, I5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SSC modulation deviation at 1.5 Gbps (G1)	Compliance pattern	5700			5700			5700			5700			ppm
RX differential skew at 1.5 Gbps (G1)	Compliance pattern	80			80			80			80			ps
RX AC common mode voltage at 1.5 Gbps (G1)	Compliance pattern	150			150			150			150			mV
Total jitter tolerance at 3.0 Gbps (G2)	Compliance pattern	> 0.65			> 0.65			> 0.65			> 0.65			UI
Deterministic jitter tolerance at 3.0 Gbps (G2)	Compliance pattern	> 0.35			> 0.35			> 0.35			> 0.35			UI
SSC modulation frequency at 3.0 Gbps (G2)	Compliance pattern	33			33			33			33			kHz
SSC modulation deviation at 3.0 Gbps (G2)	Compliance pattern	5700			5700			5700			5700			ppm
RX differential skew at 3.0 Gbps (G2)	Compliance pattern	75			75			75			75			ps
RX AC common mode voltage at 3.0 Gbps (G2)	Compliance pattern	150			150			150			150			mV
Total jitter tolerance at 6.0 Gbps (G3)	Compliance pattern	> 0.60			> 0.60			> 0.60			> 0.60			UI
Random jitter tolerance at 6.0 Gbps (G3)	Compliance pattern	> 0.18			> 0.18			> 0.18			> 0.18			UI
SSC modulation frequency at 6.0 Gbps (G3)	Compliance pattern	33			33			33			33			kHz
SSC modulation deviation at 6.0 Gbps (G3)	Compliance pattern	5700			5700			5700			5700			ppm
RX differential skew at 6.0 Gbps (G3)	Compliance pattern	30			30			30			30			ps
RX AC common mode voltage at 6.0 Gbps (G3)	Compliance pattern	100			100			100			100			mV

Table 1-40. Transceiver Block Jitter Specifications for Arria II GX Devices (Note 1) (Part 9 of 10)

Symbol/ Description	Conditions	I3			C4			C5, I5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OBSAI Receiver Jitter Tolerance (12)														
Deterministic jitter tolerance at 768 Mbps, 1536 Mbps, and 3072 Mbps	Pattern = CJPAT	> 0.37			> 0.37			> 0.37			> 0.37			UI
Combined deterministic and random jitter tolerance at 768 Mbps, 1536 Mbps, and 3072 Mbps	Pattern = CJPAT	> 0.55			> 0.55			> 0.55			> 0.55			UI
Sinusoidal jitter tolerance at 768 Mbps	Jitter frequency = 5.4 KHz Pattern = CJPAT	> 8.5			> 8.5			> 8.5			> 8.5			UI
	Jitter frequency = 460.8 KHz to 20 MHz Pattern = CJPAT	> 0.1			> 0.1			> 0.1			> 0.1			UI
Sinusoidal jitter tolerance at 1536 Mbps	Jitter frequency = 10.9 KHz Pattern = CJPAT	> 8.5			> 8.5			> 8.5			> 8.5			UI
	Jitter frequency = 921.6 KHz to 20 MHz Pattern = CJPAT	> 0.1			> 0.1			> 0.1			> 0.1			UI

Table 1–41. Transceiver Block Jitter Specifications for Arria II GZ Devices (Note 1), (2) (Part 5 of 7)

Symbol/ Description	Conditions	–C3 and –I3			–C4 and –I4			Unit
		Min	Typ	Max	Min	Typ	Max	
Sinusoidal jitter tolerance (peak-to-peak)	Jitter Frequency = 38.2 KHz Data rate = 6.375 Gbps Pattern = PRBS31 BER = 10 ⁻¹²	> 0.5			—	—	—	UI
	Jitter Frequency = 3.82 MHz Data rate = 6.375 Gbps Pattern = PRBS31 BER = 10 ⁻¹²	> 0.05			—	—	—	UI
	Jitter Frequency = 20 MHz Data rate = 6.375 Gbps Pattern = PRBS31 BER = 10 ⁻¹²	> 0.05			—	—	—	UI
SDI Transmitter Jitter Generation (12)								
Alignment jitter (peak-to-peak)	Data rate = 1.485 Gbps (HD) Pattern = color bar Low-frequency roll-off = 100 KHz	0.2	—	—	0.2	—	—	UI
	Data rate = 2.97 Gbps (3G) Pattern = color bar Low-frequency roll-off = 100 KHz	0.3	—	—	0.3	—	—	UI
SDI Receiver Jitter Tolerance (12)								
Sinusoidal jitter tolerance (peak-to-peak)	Jitter frequency = 15 KHz Data rate = 2.97 Gbps (3G) Pattern = single line scramble color bar	> 2			> 2			UI
	Jitter frequency = 100 KHz Data rate = 2.97 Gbps (3G) Pattern = single line scramble color bar	> 0.3			> 0.3			UI
	Jitter frequency = 148.5 MHz Data rate = 2.97 Gbps (3G) Pattern = single line scramble color bar	> 0.3			> 0.3			UI
Sinusoidal jitter tolerance (peak-to-peak)	Jitter frequency = 20 KHz Data rate = 1.485 Gbps (HD) pattern = 75% color bar	> 1			> 1			UI
	Jitter frequency = 100 KHz Data rate = 1.485 Gbps (HD) Pattern = 75% color bar	> 0.2			> 0.2			UI
	Jitter frequency = 148.5 MHz Data rate = 1.485 Gbps (HD) Pattern = 75% color bar	> 0.2			> 0.2			UI
SAS Transmit Jitter Generation (13)								
Total jitter at 1.5 Gbps (G1)	Pattern = CJPAT	—	—	0.55	—	—	0.55	UI
Deterministic jitter at 1.5 Gbps (G1)	Pattern = CJPAT	—	—	0.35	—	—	0.35	UI
Total jitter at 3.0 Gbps (G2)	Pattern = CJPAT	—	—	0.55	—	—	0.55	UI

Table 1–41. Transceiver Block Jitter Specifications for Arria II GZ Devices (Note 1), (2) (Part 7 of 7)

Symbol/ Description	Conditions	–C3 and –I3			–C4 and –I4			Unit
		Min	Typ	Max	Min	Typ	Max	
OBSAI Receiver Jitter Tolerance (15)								
Deterministic jitter tolerance at 768 Mbps, 1536 Mbps, and 3072 Mbps	Pattern = CJPAT	> 0.37			> 0.37			UI
Combined deterministic and random jitter tolerance at 768 Mbps, 1536 Mbps, and 3072 Mbps	Pattern = CJPAT	> 0.55			> 0.55			UI
Sinusoidal jitter tolerance at 768 Mbps	Jitter frequency = 5.4 KHz Pattern = CJPAT	> 8.5			> 8.5			UI
	Jitter frequency = 460 MHz to 20 MHz Pattern = CJPAT	> 0.1			> 0.1			UI
Sinusoidal jitter tolerance at 1536 Mbps	Jitter frequency = 10.9 KHz Pattern = CJPAT	> 8.5			> 8.5			UI
	Jitter frequency = 921.6 MHz to 20 MHz Pattern = CJPAT	> 0.1			> 0.1			UI
Sinusoidal jitter tolerance at 3072 Mbps	Jitter frequency = 21.8 KHz Pattern = CJPAT	> 8.5			> 8.5			UI
	Jitter frequency = 1843.2 MHz to 20 MHz Pattern = CJPAT	> 0.1			> 0.1			UI

Notes to Table 1–41:

- (1) Dedicated `refclk` pins were used to drive the input reference clocks.
- (2) The jitter numbers are valid for the stated conditions only.
- (3) The jitter numbers for SONET/SDH are compliant to the GR-253-CORE Issue 3 Specification.
- (4) The jitter numbers for Fibre Channel are compliant to the FC-P1-4 Specification revision 6.10.
- (5) The Fibre Channel transmitter jitter generation numbers are compliant to the specification at the δ_T inter operability point.
- (6) The Fibre Channel receiver jitter tolerance numbers are compliant to the specification at the δ_R interpretability point.
- (7) The jitter numbers for XAUI are compliant to the IEEE802.3ae-2002 Specification.
- (8) The jitter numbers for PCIe are compliant to the PCIe Base Specification 2.0.
- (9) Arria II GZ PCIe receivers are compliant to this specification provided the $V_{TX-CM-DC-ACTIVEIDLE-DELTA}$ of the upstream transmitter is less than 50 mV.
- (10) The jitter numbers for SRIO are compliant to the RapidIO Specification 1.3.
- (11) The jitter numbers for GIGE are compliant to the IEEE802.3-2002 Specification.
- (12) The HD-SDI and 3G-SDI jitter numbers are compliant to the SMPTE292M and SMPTE424M Specifications.
- (13) The jitter numbers for Serial Attached SCSI (SAS) are compliant to the SAS-2.1 Specification.
- (14) The jitter numbers for CPRI are compliant to the CPRI Specification V3.0.
- (15) The jitter numbers for OBSAI are compliant to the OBSAI RP3 Specification V4.1.

Core Performance Specifications for the Arria II Device Family

This section describes the clock tree, phase-locked loop (PLL), digital signal processing (DSP), embedded memory, configuration, and JTAG specifications for Arria II GX and GZ devices.

Clock Tree Specifications

Table 1-42 lists the clock tree specifications for Arria II GX devices.

Table 1-42. Clock Tree Performance for Arria II GX Devices

Clock Network	Performance			Unit
	I3, C4	C5,I5	C6	
GCLK and RCLK	500	500	400	MHz
PCLK	420	350	280	MHz

Table 1-43 lists the clock tree specifications for Arria II GZ devices.

Table 1-43. Clock Tree Performance for Arria II GZ Devices

Clock Network	Performance		Unit
	-C3 and -I3	-C4 and -I4	
GCLK and RCLK	700	500	MHz
PCLK	500	450	MHz

PLL Specifications

Table 1-44 lists the PLL specifications for Arria II GX devices.

Table 1-44. PLL Specifications for Arria II GX Devices (Part 1 of 3)

Symbol	Description	Min	Typ	Max	Unit
f_{IN}	Input clock frequency (from clock input pins residing in right/top/bottom banks) (-4 Speed Grade)	5	—	670 (1)	MHz
	Input clock frequency (from clock input pins residing in right/top/bottom banks) (-5 Speed Grade)	5	—	622 (1)	MHz
	Input clock frequency (from clock input pins residing in right/top/bottom banks) (-6 Speed Grade)	5	—	500 (1)	MHz
f_{INPFD}	Input frequency to the PFD	5	—	325	MHz
f_{VCO}	PLL VCO operating Range (2)	600	—	1,400	MHz
f_{INDUTY}	Input clock duty cycle	40	—	60	%
$f_{EINDUTY}$	External feedback clock input duty cycle	40	—	60	%
t_{INCCJ} (3), (4)	Input clock cycle-to-cycle jitter (Frequency ≥ 100 MHz)	—	—	0.15	UI (p-p)
	Input clock cycle-to-cycle jitter (Frequency ≤ 100 MHz)	—	—	± 750	ps (p-p)

Table 1–44. PLL Specifications for Arria II GX Devices (Part 2 of 3)

Symbol	Description	Min	Typ	Max	Unit
f_{OUT}	Output frequency for internal global or regional clock (–4 Speed Grade)	—	—	500	MHz
	Output frequency for internal global or regional clock (–5 Speed Grade)	—	—	500	MHz
	Output frequency for internal global or regional clock (–6 Speed Grade)	—	—	400	MHz
f_{OUT_EXT}	Output frequency for external clock output (–4 Speed Grade)	—	—	670 (5)	MHz
	Output frequency for external clock output (–5 Speed Grade)	—	—	622 (5)	MHz
	Output frequency for external clock output (–6 Speed Grade)	—	—	500 (5)	MHz
$t_{OUTDUTY}$	Duty cycle for external clock output (when set to 50%)	45	50	55	%
t_{OUTPJ_DC}	Dedicated clock output period jitter ($f_{OUT} \geq 100$ MHz)	—	—	300	ps (p–p)
	Dedicated clock output period jitter ($f_{OUT} < 100$ MHz)	—	—	30	mUI (p–p)
t_{OUTCCJ_DC}	Dedicated clock output cycle-to-cycle jitter ($f_{OUT} \geq 100$ MHz)	—	—	300	ps (p–p)
	Dedicated clock output cycle-to-cycle jitter ($f_{OUT} < 100$ MHz)	—	—	30	mUI (p–p)
f_{OUTPJ_IO}	Regular I/O clock output period jitter ($f_{OUT} \geq 100$ MHz)	—	—	650	ps (p–p)
	Regular I/O clock output period jitter ($f_{OUT} < 100$ MHz)	—	—	65	mUI (p–p)
f_{OUTCCJ_IO}	Regular I/O clock output cycle-to-cycle jitter ($f_{OUT} \geq 100$ MHz)	—	—	650	ps (p–p)
	Regular I/O clock output cycle-to-cycle jitter ($f_{OUT} < 100$ MHz)	—	—	65	mUI (p–p)
$t_{CONFIGPLL}$	Time required to reconfigure PLL scan chains	—	3.5	—	SCANCLK cycles
$t_{CONFIGPHASE}$	Time required to reconfigure phase shift	—	1	—	SCANCLK cycles
$f_{SCANCLK}$	SCANCLK frequency	—	—	100	MHz
t_{LOCK}	Time required to lock from end of device configuration	—	—	1	ms
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	1	ms
$f_{CL\ BW}$	PLL closed-loop low bandwidth	—	0.3	—	MHz
	PLL closed-loop medium bandwidth	—	1.5	—	MHz
	PLL closed-loop high bandwidth	—	4	—	MHz
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	±50	ps
t_{ARESET}	Minimum pulse width on areset signal	10	—	—	ns

Table 1–47. DSP Block Performance Specifications for Arria II GZ Devices (Note 1) (Part 2 of 2)

Mode	Resources Used	Performance		Unit
	Number of Multipliers	–3	–4	
Double mode	1	440	380	MHz

Notes to Table 1–47:

- (1) Maximum is for fully pipelined block with **Round** and **Saturation** disabled.
- (2) Maximum for loopback input registers disabled, **Round** and **Saturation** disabled, and pipeline and output registers enabled.

Embedded Memory Block Specifications

Table 1–48 lists the embedded memory block specifications for Arria II GX devices.

Table 1–48. Embedded Memory Block Performance Specifications for Arria II GX Devices

Memory	Mode	Resources Used		Performance				Unit
		ALUTs	Embedded Memory	I3	C4	C5,I5	C6	
Memory Logic Array Block (MLAB)	Single port 64 × 10	0	1	450	500	450	378	MHz
	Simple dual-port 32 × 20 single clock	0	1	270	500	450	378	MHz
	Simple dual-port 64 × 10 single clock	0	1	428	500	450	378	MHz
M9K Block	Single-port 256 × 36	0	1	360	400	360	310	MHz
	Single-port 256 × 36, with the read-during-write option set to Old Data	0	1	250	280	250	210	MHz
	Simple dual-port 256 × 36 single CLK	0	1	360	400	360	310	MHz
	Single-port 256 × 36 single CLK, with the read-during-write option set to Old Data	0	1	250	280	250	210	MHz
	True dual port 512 × 18 single CLK	0	1	360	400	360	310	MHz
	True dual-port 512 × 18 single CLK, with the read-during-write option set to Old Data	0	1	250	280	250	210	MHz
	Min Pulse Width (clock high time)	—	—	900	850	950	1130	ps
	Min Pulse Width (clock low time)	—	—	730	690	770	920	ps

Table 1–53. High-Speed I/O Specifications for Arria II GX Devices (Part 2 of 4)

Symbol	Conditions	I3		C4		C5,I5		C6		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Transmitter										
f _{HSDR_TX} (true LVDS output data rate)	SERDES factor, J = 3 to 10 (using dedicated SERDES)	150	1250 (2)	150	1250 (2)	150	1050 (2)	150	840	Mbps
	SERDES factor, J = 4 to 10 (using logic elements as SERDES)	(3)	945	(3)	945	(3)	840	(3)	740	Mbps
	SERDES factor, J = 2 (using DDR registers) and J = 1 (using SDR register)	(3)	(3)	(3)	(3)	(3)	(3)	(3)	(3)	Mbps
f _{HSDR_TX_E3R} (emulated LVDS_E_3R output data rate) (7)	SERDES factor, J = 4 to 10	(3)	945	(3)	945	(3)	840	(3)	740	Mbps

Table 1-54. High-Speed I/O Specifications for Arria II GZ Devices (Note 1), (2), (10) (Part 2 of 3)

Symbol	Conditions	C3, I3			C4, I4			Unit
		Min	Typ	Max	Min	Typ	Max	
$f_{\text{HCLK_OUT}}$ (output clock frequency)	—	5	—	717 (7)	5	—	717 (7)	MHz
Transmitter								
f_{HSDR} (true LVDS output data rate)	SERDES factor, J = 3 to 10 (using dedicated SERDES) (8)	(4)	—	1250	(4)	—	1250	Mbps
	SERDES factor J = 2, (using DDR registers)	(4)	—	(5)	(4)	—	(5)	Mbps
	SERDES factor J = 1, (uses an SDR register)	(4)	—	(5)	(4)	—	(5)	Mbps
f_{HSDR} (emulated LVDS_E_3R output data rate) (5)	SERDES factor J = 4 to 10	(4)	—	1152	(4)	—	800	Mbps
f_{HSDR} (emulated LVDS_E_1R output data rate)		(4)	—	200	(4)	—	200	Mbps
$t_{\text{x Jitter}}$	Total jitter for data rate, 600 Mbps to 1.6 Gbps	—	—	160	—	—	160	ps
	Total jitter for data rate, < 600 Mbps	—	—	0.1	—	—	0.1	UI
$t_{\text{x Jitter}}$ - emulated differential I/O standards with three external output resistor network	Total jitter for data rate, 600 Mbps to 1.25 Gbps	—	—	300	—	—	325	ps
	Total jitter for data rate < 600 Mbps	—	—	0.2	—	—	0.25	UI
$t_{\text{x Jitter}}$ - emulated differential I/O standards with one external output resistor network	—	—	—	0.15	—	—	0.15	UI
t_{DUTY}	TX output clock duty cycle for both True and emulated differential I/O standards	45	50	55	45	50	55	%

Figure 1-6 shows the LVDS soft-CDR/DPA sinusoidal jitter tolerance specification for Arria II GZ devices at 1.25 Gbps data rate.

Figure 1-6. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for Arria II GZ Devices at a 1.25 Gbps Data Rate

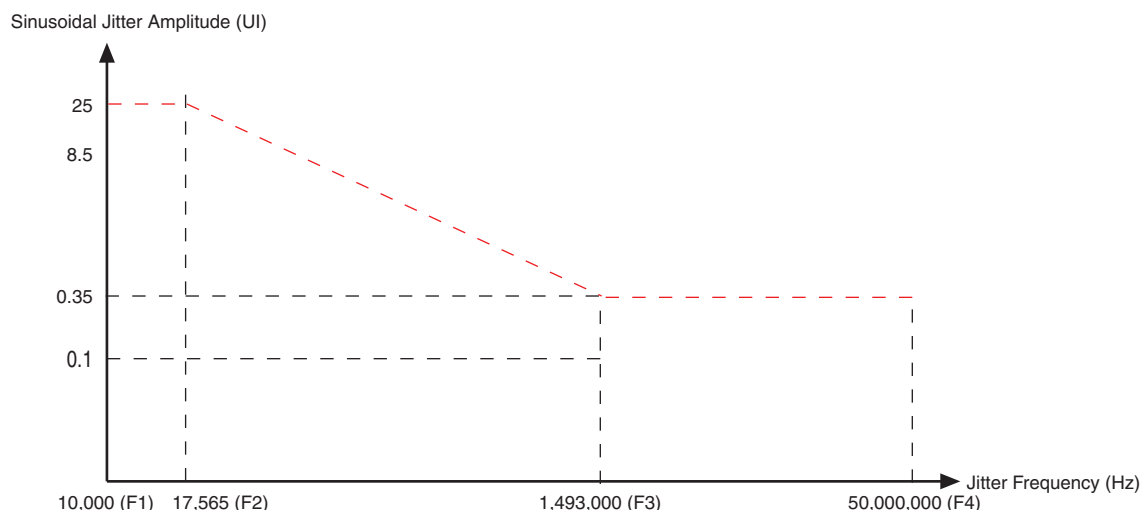


Table 1-56 lists the LVDS soft-CDR/DPA sinusoidal jitter tolerance specification for Arria II GZ devices at 1.25 Gbps data rate.

Table 1-56. LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for Arria II GZ Devices at 1.25 Gbps Data Rate

Jitter Frequency (Hz)		Sinusoidal Jitter (UI)
F1	10,000	25.000
F2	17,565	25.000
F3	1,493,000	0.350
F4	50,000,000	0.350

External Memory Interface Specifications

 For the maximum clock rate supported for Arria II GX and GZ device family, refer to the [External Memory Interface Spec Estimator](#) page on the Altera website.

Table 1-57 lists the external memory interface specifications for Arria II GX devices.

Table 1-57. External Memory Interface Specifications for Arria II GX Devices (Part 1 of 2)

Frequency Mode	Frequency Range (MHz)			Resolution (°)	DQS Delay Buffer Mode ⁽¹⁾	Number of Delay Chains
	C4	I3, C5, I5	C6			
0	90-140	90-130	90-110	22.5	Low	16
1	110-180	110-170	110-150	30	Low	12
2	140-220	140-210	140-180	36	Low	10
3	170-270	170-260	170-220	45	Low	8
4	220-340	220-310	220-270	30	High	12

Glossary

Table 1-68 lists the glossary for this chapter.

Table 1-68. Glossary (Part 1 of 4)

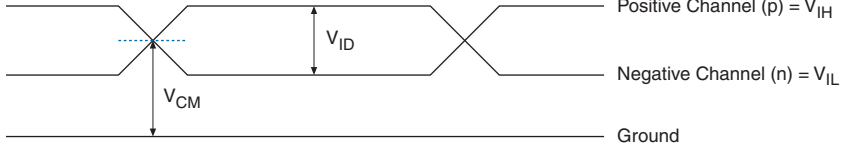
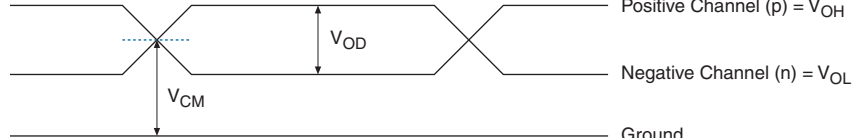
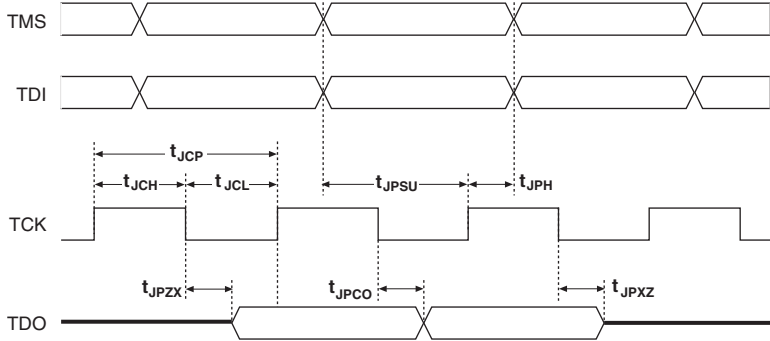
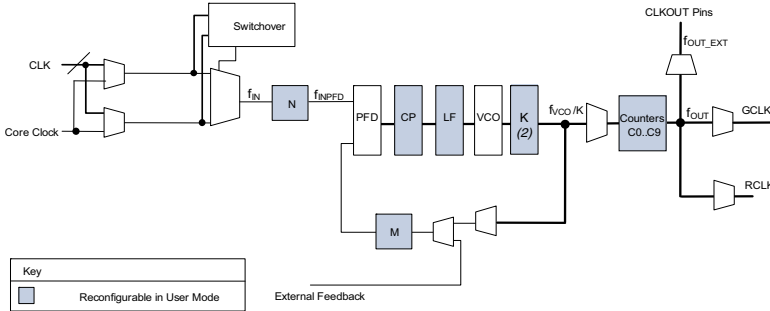
Letter	Subject	Definitions
A, B, C, D	Differential I/O Standards	<i>Receiver Input Waveforms</i> Single-Ended Waveform  Positive Channel (p) = V_{IH} Negative Channel (n) = V_{IL} Ground Differential Waveform  <i>Transmitter Output Waveforms</i> Single-Ended Waveform  Positive Channel (p) = V_{OH} Negative Channel (n) = V_{OL} Ground Differential Waveform 
E, F	f_{HSCLK}	Left/Right PLL input clock frequency.
	f_{HSDR}	High-speed I/O block: Maximum/minimum LVDS data transfer rate ($f_{HSDR} = 1/TUI$), non-DPA.
	f_{HSRDPA}	High-speed I/O block: Maximum/minimum LVDS data transfer rate ($f_{HSRDPA} = 1/TUI$), DPA.

Table 1-68. Glossary (Part 2 of 4)

Letter	Subject	Definitions
G, H, I, J	J	High-speed I/O block: Deserialization factor (width of parallel data bus).
	JTAG Timing Specifications	JTAG Timing Specifications: 
K, L, M, N, O, P	PLL Specifications	PLL Specification parameters: Diagram of PLL Specifications (1)  Notes: (1) CoreClock can only be fed by dedicated clock input pins or PLL outputs. (2) This is the VCO post-scale counter K.
Q, R	R _L	Receiver differential input discrete resistor (external to the Arria II device).