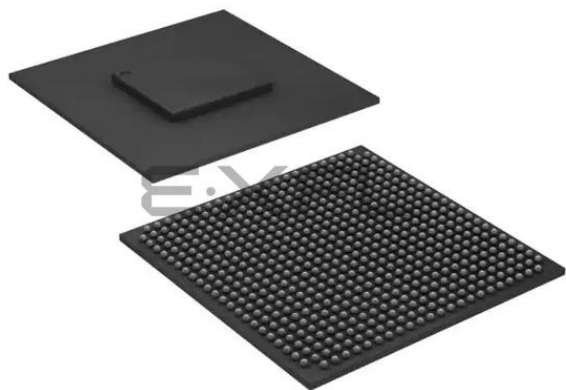




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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	4964
Number of Logic Elements/Cells	118143
Total RAM Bits	8315904
Number of I/O	260
Number of Gates	-
Voltage - Supply	0.87V ~ 0.93V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	572-BGA, FCBGA
Supplier Device Package	572-FBGA, FC (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2agx125df25i5n

Recommended Operating Conditions

This section lists the functional operation limits for AC and DC parameters for Arria II GX and GZ devices. All supplies are required to monotonically reach their full-rail values without plateaus within t_{RAMP} .

Table 1–5 lists the recommended operating conditions for Arria II GX devices.

Table 1–5. Recommended Operating Conditions for Arria II GX Devices (Note 1) (Part 1 of 2)

Symbol	Description	Condition	Minimum	Typical	Maximum	Unit
V_{CC}	Supplies power to the core, periphery, I/O registers, PCIe HIP block, and transceiver PCS	—	0.87	0.90	0.93	V
V_{CCCB}	Supplies power to the configuration RAM bits	—	1.425	1.50	1.575	V
V_{CCBAT} (2)	Battery back-up power supply for design security volatile key registers	—	1.2	—	3.3	V
V_{CCPD} (3)	Supplies power to the I/O pre-drivers, differential input buffers, and MSEL circuitry	—	3.135	3.3	3.465	V
		—	2.85	3.0	3.15	V
		—	2.375	2.5	2.625	V
V_{CCIO}	Supplies power to the I/O banks (4)	—	3.135	3.3	3.465	V
		—	2.85	3.0	3.15	V
		—	2.375	2.5	2.625	V
		—	1.71	1.8	1.89	V
		—	1.425	1.5	1.575	V
		—	1.14	1.2	1.26	V
V_{CCD_PLL}	Supplies power to the digital portions of the PLL	—	0.87	0.90	0.93	V
V_{CCA_PLL}	Supplies power to the analog portions of the PLL and device-wide power management circuitry	—	2.375	2.5	2.625	V
V_I	DC Input voltage	—	–0.5	—	3.6	V
V_O	Output voltage	—	0	—	V_{CCIO}	V
V_{CCA}	Supplies power to the transceiver PMA regulator	—	2.375	2.5	2.625	V
V_{CCL_GXB}	Supplies power to the transceiver PMA TX, PMA RX, and clocking	—	1.045	1.1	1.155	V
V_{CCH_GXB}	Supplies power to the transceiver PMA output (TX) buffer	—	1.425	1.5	1.575	V
T_J	Operating junction temperature	Commercial	0	—	85	°C
		Industrial	–40	—	100	°C

Table 1–5. Recommended Operating Conditions for Arria II GX Devices (Note 1) (Part 2 of 2)

Symbol	Description	Condition	Minimum	Typical	Maximum	Unit
t_{RAMP}	Power Supply Ramp time	Normal POR	0.05	—	100	ms
		Fast POR	0.05	—	4	ms

Notes to Table 1–5:

- (1) For more information about supply pin connections, refer to the *Arria II Device Family Pin Connection Guidelines*.
- (2) Altera recommends a 3.0-V nominal battery voltage when connecting V_{CCBAT} to a battery for volatile key backup. If you do not use the volatile security key, you may connect the V_{CCBAT} to either GND or a 3.0-V power supply.
- (3) V_{CCPD} must be 2.5-V for I/O banks with 2.5-V and lower V_{CCIO} , 3.0-V for 3.0-V V_{CCIO} , and 3.3-V for 3.3-V V_{CCIO} .
- (4) V_{CCIO} for 3C and 8C I/O banks where the configuration pins reside only supports 3.3-, 3.0-, 2.5-, or 1.8-V voltage levels.

Table 1–6 lists the recommended operating conditions for Arria II GZ devices.

Table 1–6. Recommended Operating Conditions for Arria II GZ Devices (Note 6) (Part 1 of 2)

Symbol	Description	Condition	Minimum	Typical	Maximum	Unit
V_{CC}	Core voltage and periphery circuitry power supply	—	0.87	0.90	0.93	V
V_{CCCB}	Supplies power for the configuration RAM bits	—	1.45	1.50	1.55	V
V_{CCAUX}	Auxiliary supply	—	2.375	2.5	2.625	V
V_{CCPD} (2)	I/O pre-driver (3.0 V) power supply	—	2.85	3.0	3.15	V
	I/O pre-driver (2.5 V) power supply	—	2.375	2.5	2.625	V
V_{CCIO}	I/O buffers (3.0 V) power supply	—	2.85	3.0	3.15	V
	I/O buffers (2.5 V) power supply	—	2.375	2.5	2.625	V
	I/O buffers (1.8 V) power supply	—	1.71	1.8	1.89	V
	I/O buffers (1.5 V) power supply	—	1.425	1.5	1.575	V
	I/O buffers (1.2 V) power supply	—	1.14	1.2	1.26	V
V_{CCPGM}	Configuration pins (3.0 V) power supply	—	2.85	3.0	3.15	V
	Configuration pins (2.5 V) power supply	—	2.375	2.5	2.625	V
	Configuration pins (1.8 V) power supply	—	1.71	1.8	1.89	V
$V_{\text{CCA_PLL}}$	PLL analog voltage regulator power supply	—	2.375	2.5	2.625	V
$V_{\text{CCD_PLL}}$	PLL digital voltage regulator power supply	—	0.87	0.90	0.93	V
$V_{\text{CC_CLKIN}}$	Differential clock input power supply	—	2.375	2.5	2.625	V
V_{CCBAT} (1)	Battery back-up power supply (For design security volatile key register)	—	1.2	—	3.3	V
V_{I}	DC input voltage	—	–0.5	—	3.6	V
V_{O}	Output voltage	—	0	—	V_{CCIO}	V
$V_{\text{CCA_L}}$	Transceiver high voltage power (left side)	—	2.85/2.375	3.0/2.5 (4)	3.15/2.625	V
$V_{\text{CCA_R}}$	Transceiver high voltage power (right side)	—				
$V_{\text{CCHIP_L}}$	Transceiver HIP digital power (left side)	—	0.87	0.9	0.93	V
$V_{\text{CCR_L}}$	Receiver power (left side)	—	1.05	1.1	1.15	V
$V_{\text{CCR_R}}$	Receiver power (right side)	—	1.05	1.1	1.15	V
$V_{\text{CCT_L}}$	Transmitter power (left side)	—	1.05	1.1	1.15	V
$V_{\text{CCT_R}}$	Transmitter power (right side)	—	1.05	1.1	1.15	V

I/O Pin Leakage Current

Table 1-7 lists the Arria II GX I/O pin leakage current specifications.

Table 1-7. I/O Pin Leakage Current for Arria II GX Devices

Symbol	Description	Conditions	Min	Typ	Max	Unit
I_I	Input pin	$V_I = 0\text{ V to }V_{CCIOMAX}$	-10	—	10	μA
I_{OZ}	Tri-stated I/O pin	$V_O = 0\text{ V to }V_{CCIOMAX}$	-10	—	10	μA

Table 1-8 lists the Arria II GZ I/O pin leakage current specifications.

Table 1-8. I/O Pin Leakage Current for Arria II GZ Devices

Symbol	Description	Conditions	Min	Typ	Max	Unit
I_I	Input pin	$V_I = 0\text{ V to }V_{CCIOMAX}$	-20	—	20	μA
I_{OZ}	Tri-stated I/O pin	$V_O = 0\text{ V to }V_{CCIOMAX}$	-20	—	20	μA

Bus Hold

Bus hold retains the last valid logic state after the source driving it either enters the high impedance state or is removed. Each I/O pin has an option to enable bus hold in user mode. Bus hold is always disabled in configuration mode.

Table 1-9 lists bus hold specifications for Arria II GX devices.

Table 1-9. Bus Hold Parameters for Arria II GX Devices (Note 1)

Parameter	Symbol	Cond.	V _{CCIO} (V)												Unit
			1.2		1.5		1.8		2.5		3.0		3.3		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus-hold low, sustaining current	I _{SUSL}	V _{IN} > V _{IL} (max.)	8	—	12	—	30	—	50	—	70	—	70	—	μA
Bus-hold high, sustaining current	I _{SUSH}	V _{IN} < V _{IL} (min.)	−8	—	−12	—	−30	—	−50	—	−70	—	−70	—	μA
Bus-hold low, overdrive current	I _{ODL}	0 V < V _{IN} < V _{CCIO}	—	125	—	175	—	200	—	300	—	500	—	500	μA
Bus-hold high, overdrive current	I _{ODH}	0 V < V _{IN} < V _{CCIO}	—	−125	—	−175	—	−200	—	−300	—	−500	—	−500	μA
Bus-hold trip point	V _{TRIP}	—	0.3	0.9	0.375	1.125	0.68	1.07	0.7	1.7	0.8	2	0.8	2	V

Note to Table 1-9:

(1) The bus-hold trip points are based on calculated input voltages from the JEDEC standard.

The calibration accuracy for calibrated series and parallel OCTs are applicable at the moment of calibration. When process, voltage, and temperature (PVT) conditions change after calibration, the tolerance may change.

Table 1-13 lists the Arria II GZ OCT without calibration resistance tolerance to PVT changes.

Table 1-13. OCT Without Calibration Resistance Tolerance Specifications for Arria II GZ Devices

Symbol	Description	Conditions (V)	Resistance Tolerance		Unit
			C3,I3	C4,I4	
25-Ω R _S 3.0 and 2.5	25-Ω internal series OCT without calibration	V _{CCIO} = 3.0, 2.5	± 40	± 40	%
25-Ω R _S 1.8 and 1.5	25-Ω internal series OCT without calibration	V _{CCIO} = 1.8, 1.5	± 40	± 40	%
25-Ω R _S 1.2	25-Ω internal series OCT without calibration	V _{CCIO} = 1.2	± 50	± 50	%
50-Ω R _S 3.0 and 2.5	50-Ω internal series OCT without calibration	V _{CCIO} = 3.0, 2.5	± 40	± 40	%
50-Ω R _S 1.8 and 1.5	50-Ω internal series OCT without calibration	V _{CCIO} = 1.8, 1.5	± 40	± 40	%
50-Ω R _S 1.2	50-Ω internal series OCT without calibration	V _{CCIO} = 1.2	± 50	± 50	%
100-Ω R _D 2.5	100-Ω internal differential OCT	V _{CCIO} = 2.5	± 25	± 25	%

OCT calibration is automatically performed at power up for OCT-enabled I/Os. When voltage and temperature conditions change after calibration, the resistance may change. Use Equation 1-1 and Table 1-14 to determine the OCT variation when voltage and temperature vary after power-up calibration for Arria II GX and GZ devices.

Equation 1-1. OCT Variation (Note 1)

$$R_{OCT} = R_{SCAL} \left(1 + \left\langle \frac{dR}{dT} \times \Delta T \right\rangle \pm \left\langle \frac{dR}{dV} \times \Delta V \right\rangle \right)$$

Notes to Equation 1-1:

- (1) R_{OCT} value calculated from Equation 1-1 shows the range of OCT resistance with the variation of temperature and V_{CCIO}.

I/O Standard Specifications

Table 1-22 through Table 1-35 list input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards supported by the Arria II device family. They also show the Arria II device family I/O standard specifications. V_{OL} and V_{OH} values are valid at the corresponding I_{OH} and I_{OL} , respectively.



For an explanation of terms used in Table 1-22 through Table 1-35, refer to “Glossary” on page 1-74.

Table 1-22 lists the single-ended I/O standards for Arria II GX devices.

Table 1-22. Single-Ended I/O Standards for Arria II GX Devices

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
3.3 V LVTTTL	3.135	3.3	3.465	-0.3	0.8	1.7	3.6	0.45	2.4	4	-4
3.3 V LVCMOS	3.135	3.3	3.465	-0.3	0.8	1.7	3.6	0.2	$V_{CCIO} - 0.2$	2	-2
3.0 V LVTTTL	2.85	3	3.15	-0.3	0.8	1.7	$V_{CCIO} + 0.3$	0.45	2.4	4	-4
3.0 V LVCMOS	2.85	3	3.15	-0.3	0.8	1.7	$V_{CCIO} + 0.3$	0.2	$V_{CCIO} - 0.2$	0.1	-0.1
2.5 V LVCMOS	2.375	2.5	2.625	-0.3	0.7	1.7	$V_{CCIO} + 0.3$	0.4	2	1	-1
1.8 V LVCMOS	1.71	1.8	1.89	-0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	0.45	$V_{CCIO} - 0.45$	2	-2
1.5 V LVCMOS	1.425	1.5	1.575	-0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	2	-2
1.2 V LVCMOS	1.14	1.2	1.26	-0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	2	-2
3.0-V PCI	2.85	3	3.15	—	$0.3 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.1 \times V_{CCIO}$	$0.9 \times V_{CCIO}$	1.5	-0.5
3.0-V PCI-X	2.85	3	3.15	—	$0.35 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.1 \times V_{CCIO}$	$0.9 \times V_{CCIO}$	1.5	-0.5

Table 1-23 lists the single-ended I/O standards for Arria II GZ devices.

Table 1-23. Single-Ended I/O Standards for Arria II GZ Devices (Part 1 of 2)

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
LVTTTL	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.4	2.4	2	-2
LVCMOS	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.2	$V_{CCIO} - 0.2$	0.1	-0.1
2.5 V	2.375	2.5	2.625	-0.3	0.7	1.7	3.6	0.4	2	1	-1
1.8 V	1.71	1.8	1.89	-0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	0.45	$V_{CCIO} - 0.45$	2	-2
1.5 V	1.425	1.5	1.575	-0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	2	-2

Table 1–23. Single-Ended I/O Standards for Arria II GZ Devices (Part 2 of 2)

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
1.2 V	1.14	1.2	1.26	-0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	2	-2
3.0-V PCI	2.85	3	3.15	—	$0.3 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	3.6	$0.1 \times V_{CCIO}$	$0.9 \times V_{CCIO}$	1.5	-0.5
3.0-V PCI-X	2.85	3	3.15	—	$0.35 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	—	$0.1 \times V_{CCIO}$	$0.9 \times V_{CCIO}$	1.5	-0.5

Table 1–24 lists the single-ended SSTL and HSTL I/O reference voltage specifications for Arria II GX devices.

Table 1–24. Single-Ended SSTL and HSTL I/O Reference Voltage Specifications for Arria II GX Devices

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$	$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$
SSTL-15 Class I, II	1.425	1.5	1.575	$0.47 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.53 \times V_{CCIO}$	$0.47 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.53 \times V_{CCIO}$
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	0.85	0.9	0.95
HSTL-15 Class I, II	1.425	1.5	1.575	0.71	0.75	0.79	0.71	0.75	0.79
HSTL-12 Class I, II	1.14	1.2	1.26	$0.48 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.52 \times V_{CCIO}$	—	$V_{CCIO}/2$	—

Table 1–25 lists the single-ended SSTL and HSTL I/O reference voltage specifications for Arria II GZ devices.

Table 1–25. Single-Ended SSTL and HSTL I/O Reference Voltage Specifications for Arria II GZ Devices

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$	$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$
SSTL-15 Class I, II	1.425	1.5	1.575	$0.47 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.53 \times V_{CCIO}$	$0.47 \times V_{CCIO}$	V_{REF}	$0.53 \times V_{CCIO}$
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	—	$V_{CCIO}/2$	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.68	0.75	0.9	—	$V_{CCIO}/2$	—
HSTL-12 Class I, II	1.14	1.2	1.26	$0.47 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.53 \times V_{CCIO}$	—	$V_{CCIO}/2$	—

Table 1–34. Transceiver Specifications for Arria II GX Devices (Note 1) (Part 5 of 7)

Symbol/ Description	Condition	I3			C4			C5 and I5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
LTD lock time (11)	—	0	100	4000	0	100	4000	0	100	4000	0	100	4000	ns
Data lock time from rx_ freqlocked (12)	—	—	—	4000	—	—	4000	—	—	4000	—	—	4000	ns
Programmable DC gain	DC Gain Setting = 0	—	0	—	—	0	—	—	0	—	—	0	—	dB
	DC Gain Setting = 1	—	3	—	—	3	—	—	3	—	—	3	—	dB
	DC Gain Setting = 2	—	6	—	—	6	—	—	6	—	—	6	—	dB
Transmitter														
Supported I/O Standards	1.5-V PCML													
Data rate	—	600	—	6375	600	—	3750	600	—	3750	600	—	3125	Mbps
V _{OCM}	0.65 V setting	—	650	—	—	650	—	—	650	—	—	650	—	mV
Differential on-chip termination resistors	100-Ω setting	—	100	—	—	100	—	—	100	—	—	100	—	Ω
Return loss differential mode	PCIe	50 MHz to 1.25 GHz: –10dB												
	XAUI	312 MHz to 625 MHz: –10dB 625 MHz to 3.125 GHz: –10dB/decade slope												
Return loss common mode	PCIe	50 MHz to 1.25 GHz: –6dB												
Rise time (2)	—	50	—	200	50	—	200	50	—	200	50	—	200	ps
Fall time	—	50	—	200	50	—	200	50	—	200	50	—	200	ps

Table 1–34. Transceiver Specifications for Arria II GX Devices (Note 1) (Part 7 of 7)

Symbol/ Description	Condition	I3			C4			C5 and I5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Digital reset pulse width	—	Minimum is 2 parallel clock cycles												

Notes to Table 1–34:

- (1) For AC-coupled links, the on-chip biasing circuit is switched off before and during configuration. Ensure that input specifications are not violated during this period.
- (2) The rise/fall time is specified from 20% to 80%.
- (3) To calculate the REFCLK rms phase jitter requirement at reference clock frequencies other than 100 MHz, use the following formula:
REFCLK rms phase jitter at f (MHz) = REFCLK rms phase jitter at 100 MHz * 100/f.
- (4) The minimum `reconfig_clk` frequency is 2.5 MHz if the transceiver channel is configured in **Transmitter only** mode. The minimum `reconfig_clk` frequency is 37.5 MHz if the transceiver channel is configured in **Receiver only** or **Receiver and Transmitter** mode. For more information, refer to [AN 558: Implementing Dynamic Reconfiguration in Arria II Devices](#).
- (5) If your design uses more than one dynamic reconfiguration controller instances (`altgx_reconfig`) to control the transceiver channels (`altgx`) physically located on the same side of the device, and if you use different `reconfig_clk` sources for these `altgx_reconfig` instances, the delta time between any two of these `reconfig_clk` sources becoming stable must not exceed the maximum specification listed.
- (6) The device cannot tolerate prolonged operation at this absolute maximum.
- (7) You must use the 1.1-V RX V_{ICM} setting if the input serial data standard is LVDS and the link is DC-coupled.
- (8) The rate matcher supports only up to ± 300 parts per million (ppm).
- (9) Time taken to `rx_pll_locked` goes high from `rx_analogreset` de-assertion. Refer to [Figure 1–1](#).
- (10) The time in which the CDR must be kept in lock-to-reference mode after `rx_pll_locked` goes high and before `rx_locktodata` is asserted in manual mode. Refer to [Figure 1–1](#).
- (11) The time taken to recover valid data after the `rx_locktodata` signal is asserted in manual mode. Refer to [Figure 1–1](#).
- (12) The time taken to recover valid data after the `rx_freqlocked` signal goes high in automatic mode. Refer to [Figure 1–2](#).
- (13) To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.

Table 1–35 lists the transceiver specifications for Arria II GZ devices.

Table 1–35. Transceiver Specifications for Arria II GZ Devices (Part 1 of 5)

Symbol/ Description	Conditions	–C3 and –I3 (1)			–C4 and –I4			Unit
		Min	Typ	Max	Min	Typ	Max	
Reference Clock								
Supported I/O Standards	1.2-V PCML, 1.5-V PCML, 2.5-V PCML, Differential LVPECL, LVDS, and HCSL							
Input frequency from REFCLK input pins	—	50	—	697	50	—	637.5	MHz
Phase frequency detector (CMU PLL and receiver CDR)	—	50	—	325	50	—	325	MHz
Absolute V _{MAX} for a REFCLK pin	—	—	—	1.6	—	—	1.6	V
Operational V _{MAX} for a REFCLK pin	—	—	—	1.5	—	—	1.5	V
Absolute V _{MIN} for a REFCLK pin	—	-0.4	—	—	-0.4	—	—	V
Rise/fall time (2)	—	—	—	0.2	—	—	0.2	UI
Duty cycle	—	45	—	55	45	—	55	%
Peak-to-peak differential input voltage	—	200	—	1600	200	—	1600	mV
Spread-spectrum modulating clock frequency	PCIe	30	—	33	30	—	33	kHz
Spread-spectrum downspread	PCIe	—	0 to -0.5%	—	—	0 to -0.5%	—	—
On-chip termination resistors	—	—	100	—	—	100	—	Ω
V _{ICM} (AC coupled)	—	1100 ± 10%			1100 ± 10%			mV
V _{ICM} (DC coupled)	HCSL I/O standard for PCIe reference clock	250	—	550	250	—	550	mV
Transmitter REFCLK Phase Noise	10 Hz	—	—	-50	—	—	-50	dBc/Hz
	100 Hz	—	—	-80	—	—	-80	dBc/Hz
	1 KHz	—	—	-110	—	—	-110	dBc/Hz
	10 KHz	—	—	-120	—	—	-120	dBc/Hz
	100 KHz	—	—	-120	—	—	-120	dBc/Hz
	≥ 1 MHz	—	—	-130	—	—	-130	dBc/Hz
Transmitter REFCLK Phase Jitter (rms) for 100 MHz REFCLK (3)	10 KHz to 20 MHz	—	—	3	—	—	3	ps
R _{REF}	—	—	2000 ± 1%	—	—	2000 ± 1%	—	Ω

Table 1-35. Transceiver Specifications for Arria II GZ Devices (Part 3 of 5)

Symbol/ Description	Conditions	–C3 and –I3 (1)			–C4 and –I4			Unit
		Min	Typ	Max	Min	Typ	Max	
Receiver DC Coupling Support	—	For more information about receiver DC coupling support, refer to the “DC-Coupled Links” section in the <i>Transceiver Architecture for Arria II Devices</i> chapter.						
Differential on-chip termination resistors	85–Ω setting	85 ± 20%			85 ± 20%			Ω
	100–Ω setting	100 ± 20%			100 ± 20%			Ω
	120–Ω setting	120 ± 20%			120 ± 20%			Ω
	150–Ω setting	150 ± 20%			150 ± 20%			Ω
Differential and common mode return loss	PCIe (Gen 1 and Gen 2), XAUI, HiGig+, CEI SR/LR, SRIO SR/LR, CPRI LV/HV, OBSAI, SATA	Compliant						—
Programmable PPM detector (9)	—	± 62.5, 100, 125, 200, 250, 300, 500, 1,000						ppm
Run length	—	—	—	200	—	—	200	UI
Programmable equalization	—	—	—	16	—	—	16	dB
t _{LTR} (10)	—	—	—	75	—	—	75	μs
t _{LTR_LTD_Manual} (11)	—	15	—	—	15	—	—	μs
t _{LTD_Manual} (12)	—	—	—	4000	—	—	4000	ns
t _{LTD_Auto} (13)	—	—	—	4000	—	—	4000	ns
Receiver CDR 3 dB Bandwidth in lock-to-data (LTD) mode	PCIe Gen1	2.0 - 3.5						MHz
	PCIe Gen2	40 - 65						MHz
	(OIF) CEI PHY at 6.375 Gbps	20 - 35						MHz
	XAUI	10 - 18						MHz
	SRIO 1.25 Gbps	10 - 18						MHz
	SRIO 2.5 Gbps	10 - 18						MHz
	SRIO 3.125 Gbps	6 - 10						MHz
	GIGE	6 - 10						MHz
	SONET OC12	3 - 6						MHz
	SONET OC48	14 - 19						MHz
Receiver buffer and CDR offset cancellation time (per channel)	—	—	—	17000	—	—	17000	recon fig_ clk cycles
Programmable DC gain	DC Gain Setting = 0	—	0	—	—	0	—	dB
	DC Gain Setting = 1	—	3	—	—	3	—	dB
	DC Gain Setting = 2	—	6	—	—	6	—	dB

Table 1–39. Transmitter Pre-Emphasis Levels for Arria II GZ Devices (Part 2 of 2)

Pre-Emphasis 1st Post-Tap Setting	V _{OD} Setting							
	0	1	2	3	4	5	6	7
29	N/A	N/A	N/A	12.5	9.6	7.7	6.3	4.3
30	N/A	N/A	N/A	N/A	11.4	9	7.4	N/A
31	N/A	N/A	N/A	N/A	12.9	10	8.2	N/A

Table 1–40 lists the transceiver jitter specifications for all supported protocols for Arria II GX devices.

Table 1–40. Transceiver Block Jitter Specifications for Arria II GX Devices (Note 1) (Part 1 of 10)

Symbol/ Description	Conditions	I3			C4			C5, I5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SONET/SDH Transmit Jitter Generation (2)														
Peak-to-peak jitter at 622.08 Mbps	Pattern = PRBS15	—	—	0.1	—	—	0.1	—	—	0.1	—	—	0.1	UI
RMS jitter at 622.08 Mbps	Pattern = PRBS15	—	—	0.01	—	—	0.01	—	—	0.01	—	—	0.01	UI
Peak-to-peak jitter at 2488.32 Mbps	Pattern = PRBS15	—	—	0.1	—	—	0.1	—	—	0.1	—	—	0.1	UI
RMS jitter at 2488.32 Mbps	Pattern = PRBS15	—	—	0.01	—	—	0.01	—	—	0.01	—	—	0.01	UI
SONET/SDH Receiver Jitter Tolerance (2)														
Jitter tolerance at 622.08 Mbps	Jitter frequency = 0.03 KHz Pattern = PRBS15	> 15			> 15			> 15			> 15			UI
	Jitter frequency = 25 KHZ Pattern = PRBS15	> 1.5			> 1.5			> 1.5			> 1.5			UI
	Jitter frequency = 250 KHz Pattern = PRBS15	> 0.15			> 0.15			> 0.15			> 0.15			UI

Table 1–40. Transceiver Block Jitter Specifications for Arria II GX Devices (Note 1) (Part 5 of 10)

Symbol/ Description	Conditions	I3			C4			C5, I5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SDI Transmitter Jitter Generation (8)														
Alignment jitter (peak-to-peak)	Data rate = 1.485 Gbps (HD) pattern = Color Bar Low- frequency Roll-off = 100 KHz	0.2	—	—	0.2	—	—	0.2	—	—	0.2	—	—	UI
	Data rate = 2.97 Gbps (3G) pattern = Color bar Low- frequency Roll-off = 100 KHz	0.3	—	—	0.3	—	—	0.3	—	—	0.3	—	—	UI
SDI Receiver Jitter Tolerance (8)														
Sinusoidal jitter tolerance (peak-to-peak)	Jitter frequency = 15 KHz Data rate = 2.97 Gbps (3G) Pattern = single line scramble color bar	> 2			> 2			> 2			> 2			UI
	Jitter frequency = 100 KHz Data rate = 2.97 Gbps (3G) Pattern = single line scramble color bar	> 0.3			> 0.3			> 0.3			> 0.3			UI
	Jitter frequency = 148.5 MHz Data rate = 2.97 Gbps (3G) Pattern = single line scramble color bar	> 0.3			> 0.3			> 0.3			> 0.3			UI

Table 1–41. Transceiver Block Jitter Specifications for Arria II GZ Devices (Note 1), (2) (Part 2 of 7)

Symbol/ Description	Conditions	–C3 and –I3			–C4 and –I4			Unit
		Min	Typ	Max	Min	Typ	Max	
Jitter tolerance at 2488.32 Mbps	Jitter frequency = 0.06 KHz Pattern = PRBS15	> 15			> 15			UI
	Jitter frequency = 100 KHZ Pattern = PRBS15	> 1.5			> 1.5			UI
	Jitter frequency = 1 MHz Pattern = PRBS15	> 0.15			> 0.15			UI
	Jitter frequency = 10 MHz Pattern = PRBS15	> 0.15			> 0.15			UI
Fibre Channel Transmit Jitter Generation (4), (5)								
Total jitter FC-1	Pattern = CRPAT	—	—	0.23	—	—	0.23	UI
Deterministic jitter FC-1	Pattern = CRPAT	—	—	0.11	—	—	0.11	UI
Total jitter FC-2	Pattern = CRPAT	—	—	0.33	—	—	0.33	UI
Deterministic jitter FC-2	Pattern = CRPAT	—	—	0.2	—	—	0.2	UI
Total jitter FC-4	Pattern = CRPAT	—	—	0.52	—	—	0.52	UI
Deterministic jitter FC-4	Pattern = CRPAT	—	—	0.33	—	—	0.33	UI
Fibre Channel Receiver Jitter Tolerance (4), (6)								
Deterministic jitter FC-1	Pattern = CJTPAT	> 0.37			> 0.37			UI
Random jitter FC-1	Pattern = CJTPAT	> 0.31			> 0.31			UI
Sinusoidal jitter FC-1	Fc/25000	> 1.5			> 1.5			UI
	Fc/1667	> 0.1			> 0.1			UI
Deterministic jitter FC-2	Pattern = CJTPAT	> 0.33			> 0.33			UI
Random jitter FC-2	Pattern = CJTPAT	> 0.29			> 0.29			UI
Sinusoidal jitter FC-2	Fc/25000	> 1.5			> 1.5			UI
	Fc/1667	> 0.1			> 0.1			UI
Deterministic jitter FC-4	Pattern = CJTPAT	> 0.33			> 0.33			UI
Random jitter FC-4	Pattern = CJTPAT	> 0.29			> 0.29			UI
Sinusoidal jitter FC-4	Fc/25000	> 1.5			> 1.5			UI
	Fc/1667	> 0.1			> 0.1			UI
XAUI Transmit Jitter Generation (7)								
Total jitter at 3.125 Gbps	Pattern = CJPAT	—	—	0.3	—	—	0.3	UI
Deterministic jitter at 3.125 Gbps	Pattern = CJPAT	—	—	0.17	—	—	0.17	UI
XAUI Receiver Jitter Tolerance (7)								
Total jitter	—	> 0.65			> 0.65			UI
Deterministic jitter	—	> 0.37			> 0.37			UI

Table 1-44. PLL Specifications for Arria II GX Devices (Part 3 of 3)

Symbol	Description	Min	Typ	Max	Unit
$t_{CASC_OUTJITTER_PERIOD_DEDCLK}$ (6), (7)	Period jitter for dedicated clock output in cascaded PLLs ($F_{OUT} \geq 100$ MHz)	—	—	425	ps (p-p)
	Period jitter for dedicated clock output in cascaded PLLs ($F_{OUT} \leq 100$ MHz)	—	—	42.5	mUI (p-p)

Notes to Table 1-44:

- (1) f_{IN} is limited by the I/O f_{MAX} .
- (2) The VCO frequency reported by the Quartus II software in the PLL summary section of the compilation report takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f_{VCO} specification.
- (3) A high-input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean-clock source, which is less than 200 ps.
- (4) F_{REF} is f_{IN}/N when $N = 1$.
- (5) This specification is limited by the lower of the two: I/O f_{MAX} or f_{OUT} of the PLL.
- (6) Peak-to-peak jitter with a probability level of 10^{-12} (14 sigma, 99.999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in Table 1-62 on page 1-70.
- (7) The cascaded PLL specification is only applicable with the following condition:
 - a. Upstream PLL: $0.59 \text{ MHz} \leq \text{Upstream PLL BW} < 1 \text{ MHz}$
 - b. Downstream PLL: $\text{Downstream PLL BW} > 2 \text{ MHz}$

Table 1-45 lists the PLL specifications for Arria II GZ devices when operating in both the commercial junction temperature range (0° to 85°C) and the industrial junction temperature range (-40° to 100°C).

Table 1-45. PLL Specifications for Arria II GZ Devices (Part 1 of 2)

Symbol	Parameter	Min	Typ	Max	Unit
f_{IN}	Input clock frequency (-3 speed grade)	5	—	717 (1)	MHz
	Input clock frequency (-4 speed grade)	5	—	717 (1)	MHz
f_{INPFD}	Input frequency to the PFD	5	—	325	MHz
f_{VCO}	PLL VCO operating range (-3 speed grade)	600	—	1,300	MHz
	PLL VCO operating range (-4 speed grade)	600	—	1,300	MHz
$t_{EINDUTY}$	Input clock or external feedback clock input duty cycle	40	—	60	%
f_{OUT}	Output frequency for internal global or regional clock (-3 speed grade)	—	—	700 (2)	MHz
	Output frequency for internal global or regional clock (-4 speed grade)	—	—	500 (2)	MHz
f_{OUT_EXT}	Output frequency for external clock output (-3 speed grade)	—	—	717 (2)	MHz
	Output frequency for external clock output (-4 speed grade)	—	—	717 (2)	MHz
$t_{OUTDUTY}$	Duty cycle for external clock output (when set to 50%)	45	50	55	%
t_{FCOMP}	External feedback clock compensation time	—	—	10	ns
$t_{CONFIGPLL}$	Time required to reconfigure scan chain	—	3.5	—	scanclk cycles
$t_{CONFIGPHASE}$	Time required to reconfigure phase shift	—	1	—	scanclk cycles
$f_{SCANCLK}$	scanclk frequency	—	—	100	MHz
t_{LOCK}	Time required to lock from end-of-device configuration or de-assertion of areset	—	—	1	ms

Table 1-45. PLL Specifications for Arria II GZ Devices (Part 2 of 2)

Symbol	Parameter	Min	Typ	Max	Unit
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	1	ms
f_{CLBW}	PLL closed-loop low bandwidth	—	0.3	—	MHz
	PLL closed-loop medium bandwidth	—	1.5	—	MHz
	PLL closed-loop high bandwidth (7)	—	4	—	MHz
$t_{\text{PLL_PSERR}}$	Accuracy of PLL phase shift	—	—	±50	ps
t_{ARESET}	Minimum pulse width on the areset signal	10	—	—	ns
t_{INCCJ} (3), (4)	Input clock cycle to cycle jitter ($F_{\text{REF}} \geq 100$ MHz)	—	—	0.15	UI (p-p)
	Input clock cycle to cycle jitter ($F_{\text{REF}} < 100$ MHz)	—	—	±750	ps (p-p)
$t_{\text{OUTPJ_DC}}$ (5)	Period Jitter for dedicated clock output ($F_{\text{OUT}} \geq 100$ MHz)	—	—	175	ps (p-p)
	Period Jitter for dedicated clock output ($F_{\text{OUT}} < 100$ MHz)	—	—	17.5	mUI (p-p)
$t_{\text{OUTCCJ_DC}}$ (5)	Cycle to Cycle Jitter for dedicated clock output ($F_{\text{OUT}} \geq 100$ MHz)	—	—	175	ps (p-p)
	Cycle to Cycle Jitter for dedicated clock output ($F_{\text{OUT}} < 100$ MHz)	—	—	17.5	mUI (p-p)
$t_{\text{OUTPJ_IO}}$ (5), (8)	Period Jitter for clock output on regular I/O ($F_{\text{OUT}} \geq 100$ MHz)	—	—	600	ps (p-p)
	Period Jitter for clock output on regular I/O ($F_{\text{OUT}} < 100$ MHz)	—	—	60	mUI (p-p)
$t_{\text{OUTCCJ_IO}}$ (5), (8)	Cycle to Cycle Jitter for clock output on regular I/O ($F_{\text{OUT}} \geq 100$ MHz)	—	—	600	ps (p-p)
	Cycle to Cycle Jitter for clock output on regular I/O ($F_{\text{OUT}} < 100$ MHz)	—	—	60	mUI (p-p)
$t_{\text{CASC_OUTPJ_DC}}$ (5), (6)	Period Jitter for dedicated clock output in cascaded PLLs ($F_{\text{OUT}} \geq 100$ MHz)	—	—	250	ps (p-p)
	Period Jitter for dedicated clock output in cascaded PLLs ($F_{\text{OUT}} < 100$ MHz)	—	—	25	mUI (p-p)
f_{DRIFT}	Frequency drift after PFDENA is disabled for duration of 100 μ s	—	—	±10	%

Notes to Table 1-45:

- (1) This specification is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.
- (2) This specification is limited by the lower of the two: I/O F_{MAX} or F_{OUT} of the PLL.
- (3) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source that is less than 120 ps.
- (4) F_{REF} is f_{IN}/N when $N = 1$.
- (5) Peak-to-peak jitter with a probability level of 10^{-12} (14 sigma, 99.9999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in [Table 1-64 on page 1-71](#).
- (6) The cascaded PLL specification is only applicable with the following condition:
 - a. Upstream PLL: $0.59 \text{ MHz} \leq \text{Upstream PLL BW} < 1 \text{ MHz}$
 - b. Downstream PLL: $\text{Downstream PLL BW} > 2 \text{ MHz}$
- (7) High bandwidth PLL settings are not supported in external feedback mode.
- (8) External memory interface clock output jitter specifications use a different measurement method, which is available in [Table 1-63 on page 1-71](#).

DSP Block Specifications

Table 1-46 lists the DSP block performance specifications for Arria II GX devices.

Table 1-46. DSP Block Performance Specifications for Arria II GX Devices (Note 1)

Mode	Resources Used	Performance				Unit
	Number of Multipliers	C4	I3	C5,I5	C6	
9 × 9-bit multiplier	1	380	310	300	250	MHz
12 × 12-bit multiplier	1	380	310	300	250	MHz
18 × 18-bit multiplier	1	380	310	300	250	MHz
36 × 36-bit multiplier	1	350	270	270	220	MHz
18 × 36-bit high-precision multiplier adder mode	1	350	270	270	220	MHz
18 × 18-bit multiply accumulator	4	380	310	300	250	MHz
18 × 18-bit multiply adder	4	380	310	300	250	MHz
18 × 18-bit multiply adder-signed full precision	2	380	310	300	250	MHz
18 × 18-bit multiply adder with loopback (2)	2	275	220	220	180	MHz
36-bit shift (32-bit data)	1	350	270	270	220	MHz
Double mode	1	350	270	270	220	MHz

Notes to Table 1-46:

- (1) Maximum is for a fully-pipelined block with **Round** and **Saturation** disabled.
- (2) Maximum is for loopback input registers disabled, **Round** and **Saturation** disabled, pipeline and output registers enabled.

Table 1-47 lists the DSP block performance specifications for Arria II GZ devices.

Table 1-47. DSP Block Performance Specifications for Arria II GZ Devices (Note 1) (Part 1 of 2)

Mode	Resources Used	Performance		Unit
	Number of Multipliers	-3	-4	
9 × 9-bit multiplier	1	460	400	MHz
12 × 12-bit multiplier	1	500	440	MHz
18 × 18-bit multiplier	1	550	480	MHz
36 × 36-bit multiplier	1	440	380	MHz
18 × 18-bit multiply accumulator	4	440	380	MHz
18 × 18-bit multiply adder	4	470	410	MHz
18 × 18-bit multiply adder-signed full precision	2	450	390	MHz
18 × 18-bit multiply adder with loopback (2)	2	350	310	MHz
36-bit shift (32-bit data)	1	440	380	MHz

Periphery Performance

This section describes periphery performance, including high-speed I/O, external memory interface, and IOE programmable delay.

I/O performance supports several system interfaces, for example the high-speed I/O interface, external memory interface, and the PCI/PCI-X bus interface. I/O using SSTL-18 Class I termination standard can achieve up to the stated DDR2 SDRAM interfacing speed with typical DDR2 SDRAM memory interface setup. I/O using general purpose I/O (GPIO) standards such as 3.0, 2.5, 1.8, or 1.5 LVTTTL/LVCMOS are capable of typical 200 MHz interfacing frequency with 10pF load.



Actual achievable frequency depends on design- and system-specific factors. You should perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

High-Speed I/O Specification

Table 1-53 lists the high-speed I/O timing for Arria II GX devices.

Table 1-53. High-Speed I/O Specifications for Arria II GX Devices (Part 1 of 4)

Symbol	Conditions	I3		C4		C5,I5		C6		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Clock										
f _{HCLK_IN} (input clock frequency)–Row I/O	Clock boost factor, W = 1 to 40 (1)	5	670	5	670	5	622	5	500	MHz
f _{HCLK_IN} (input clock frequency)–Column I/O	Clock boost factor, W = 1 to 40 (1)	5	500	5	500	5	472.5	5	472.5	MHz
f _{HCLK_OUT} (output clock frequency)–Row I/O	—	5	670	5	670	5	622	5	500	MHz
f _{HCLK_OUT} (output clock frequency)–Column I/O	—	5	500	5	500	5	472.5	5	472.5	MHz

Table 1–53. High-Speed I/O Specifications for Arria II GX Devices (Part 4 of 4)

Symbol	Conditions	I3		C4		C5,I5		C6		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
f_{HSDR} (data rate)	SERDES factor J = 3 to 10	(3)	945 (7)	(3)	945 (7)	(3)	740 (7)	(3)	640 (7)	Mbps
	SERDES factor J = 2 (using DDR registers)	(3)	(7)	(3)	(7)	(3)	(7)	(3)	(7)	Mbps
	SERDES factor J = 1 (using SDR registers)	(3)	(7)	(3)	(7)	(3)	(7)	(3)	(7)	Mbps
Soft-CDR PPM tolerance	Soft-CDR mode	—	300	—	300	—	300	—	300	±PPM
DPA run length	DPA mode	—	10,000	—	10,000	—	10,000	—	10,000	UI
Sampling window (SW)	Non-DPA mode (5)	—	300	—	300	—	350	—	400	ps

Notes to Table 1–53:

- (1) $f_{\text{HCLK_IN}} = f_{\text{HSDR}} / W$. Use W to determine the supported selection of input reference clock frequencies for the desired data rate.
- (2) Applicable for interfacing with DPA receivers only. For interfacing with non-DPA receivers, you must calculate the leftover timing margin in the receiver by performing link timing closure analysis. For Arria II GX transmitter to Arria II GX non-DPA receiver, the maximum supported data rate is 945 Mbps. For data rates above 840 Mbps, perform PCB trace compensation by adjusting the PCB trace length for LVDS channels to improve channel-to-channel skews.
- (3) The minimum and maximum specification depends on the clock source (for example, PLL and clock pin) and the clock routing resource you use (global, regional, or local). The I/O differential buffer and input register do not have a minimum toggle rate.
- (4) The specification is only applicable under the influence of core noise.
- (5) Applicable for true LVDS using dedicated SERDES only.
- (6) Dedicated SERDES and DPA features are only available on the right banks.
- (7) You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and the receiver sampling margin to determine the leftover timing margin.

Table 1–54 lists the high-speed I/O timing for Arria II GZ devices.

Table 1–54. High-Speed I/O Specifications for Arria II GZ Devices (Note 1), (2), (10) (Part 1 of 3)

Symbol	Conditions	C3, I3			C4, I4			Unit
		Min	Typ	Max	Min	Typ	Max	
Clock								
f _{HCLK_in} (input clock frequency) true differential I/O standards	Clock boost factor W = 1 to 40 (3)	5	—	717	5	—	717	MHz
f _{HCLK_in} (input clock frequency) single ended I/O standards (9)	Clock boost factor W = 1 to 40 (3)	5	—	717	5	—	717	MHz
f _{HCLK_in} (input clock frequency) single ended I/O standards (10)	Clock boost factor W = 1 to 40 (3)	5	—	420	5	—	420	MHz

Table 1-54. High-Speed I/O Specifications for Arria II GZ Devices (Note 1), (2), (10) (Part 2 of 3)

Symbol	Conditions	C3, I3			C4, I4			Unit
		Min	Typ	Max	Min	Typ	Max	
$f_{\text{HCLK_OUT}}$ (output clock frequency)	—	5	—	717 (7)	5	—	717 (7)	MHz
Transmitter								
f_{HSDR} (true LVDS output data rate)	SERDES factor, J = 3 to 10 (using dedicated SERDES) (8)	(4)	—	1250	(4)	—	1250	Mbps
	SERDES factor J = 2, (using DDR registers)	(4)	—	(5)	(4)	—	(5)	Mbps
	SERDES factor J = 1, (uses an SDR register)	(4)	—	(5)	(4)	—	(5)	Mbps
f_{HSDR} (emulated LVDS_E_3R output data rate) (5)	SERDES factor J = 4 to 10	(4)	—	1152	(4)	—	800	Mbps
f_{HSDR} (emulated LVDS_E_1R output data rate)		(4)	—	200	(4)	—	200	Mbps
$t_{\text{x Jitter}}$	Total jitter for data rate, 600 Mbps to 1.6 Gbps	—	—	160	—	—	160	ps
	Total jitter for data rate, < 600 Mbps	—	—	0.1	—	—	0.1	UI
$t_{\text{x Jitter}}$ - emulated differential I/O standards with three external output resistor network	Total jitter for data rate, 600 Mbps to 1.25 Gbps	—	—	300	—	—	325	ps
	Total jitter for data rate < 600 Mbps	—	—	0.2	—	—	0.25	UI
$t_{\text{x Jitter}}$ - emulated differential I/O standards with one external output resistor network	—	—	—	0.15	—	—	0.15	UI
t_{DUTY}	TX output clock duty cycle for both True and emulated differential I/O standards	45	50	55	45	50	55	%

IOE Programmable Delay

Table 1–66 lists the delay associated with each supported IOE programmable delay chain for Arria II GX devices.

Table 1–66. IOE Programmable Delay for Arria II GX Devices

Parameter	Available Settings <i>(1)</i>	Minimum Offset <i>(2)</i>	Maximum Offset								Unit
			Fast Model			Slow Model					
			I3	C4	I5	I3	C4	C5	I5	C6	
Output enable pin delay	7	0	0.413	0.442	0.413	0.814	0.713	0.796	0.801	0.873	ns
Delay from output register to output pin	7	0	0.339	0.362	0.339	0.671	0.585	0.654	0.661	0.722	ns
Input delay from pin to internal cell	52	0	1.494	1.607	1.494	2.895	2.520	2.733	2.775	2.944	ns
Input delay from pin to input register	52	0	1.493	1.607	1.493	2.896	2.503	2.732	2.774	2.944	ns
DQS bus to input register delay	4	0	0.074	0.076	0.074	0.140	0.124	0.147	0.147	0.167	ns

Notes to Table 1–66:

- (1) The available setting for every delay chain starts with zero and ends with the specified maximum number of settings.
- (2) The minimum offset represented in the table does not include intrinsic delay.

Table 1–67 lists the IOE programmable delay settings for Arria II GZ devices.

Table 1–67. IOE Programmable Delay for Arria II GZ Devices

Parameter	Available Settings <i>(1)</i>	Minimum Offset <i>(2)</i>	Maximum Offset						Unit
			Fast Model		Slow Model				
			Industrial	Commercial	C3	I3	C4	I4	
D1	15	0	0.462	0.505	0.795	0.801	0.857	0.864	ns
D2	7	0	0.234	0.232	0.372	0.371	0.407	0.405	ns
D3	7	0	1.700	1.769	2.927	2.948	3.157	3.178	ns
D4	15	0	0.508	0.554	0.882	0.889	0.952	0.959	ns
D5	15	0	0.472	0.500	0.799	0.817	0.875	0.882	ns
D6	6	0	0.186	0.195	0.319	0.321	0.345	0.347	ns

Notes to Table 1–67:

- (1) You can set this value in the Quartus II software by selecting **D1**, **D2**, **D3**, **D4**, **D5**, and **D6** in the **Assignment Name** column.
- (2) Minimum offset does not include the intrinsic delay.